Todo list

MicroSys
Creating Embedded Systems

CRX-IMX95

User Manual (HW Revision 2)

V0.1

Table of Contents

1 Document Information

	Name	Role	Signature
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Reviewed by			
Approved by			

2 Document history

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Date	Version	Change description
2024-12-19	V0.1	Draft Hardware Revision 1
2025-07-14	V0.1	Draft Hardware Revision 2

Table 1: *List of changes*

3 General notes

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3.5 Errata handling

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It is the user’s responsibility to make sure all errata published by the manufacturer of each component are taken note of.

The manufacturer’s advice should be followed.

If desired, MicroSys Electronics GmbH can support you with your lifecycle management regarding chip errata. Please ask your sales representative or send an email inquiry to support@microsys.de .

3.6 Definitions

Information marked with this symbol `MUST` be obeyed to avoid the risk of material damage to the equipment and/or injury to the involved personnel.

Information marked with this symbol `MUST` be obeyed to avoid the risk of material damage to the equipment.

Additional information, not binding.

3.7 Safety and Handling Precautions

You `MUST NOT` exceed the rated maximum values for the device! This may result in severe permanent damage to the unit, as well as possible serious injury.
ALWAYS keep the unit dry, clean and free of foreign objects. Otherwise, irreparable damage may occur.

Parts of the unit may become hot during operation. Take care not to touch any parts of the circuitry during operation to avoid burns and operate the unit in a well-ventilated location. Provide an appropriate cooling solution as required.

Electrostatic discharge (ESD) can damage the unit. Always take the necessary ESD precautions.
Many pins on the module connector are directly connected to the SOC or other ESD sensitive devices.
Make or break ANY connection ONLY while the unit is switched OFF.
Otherwise, permanent damage to the unit may occur, which is not covered by warranty.

3.8 Conventions

There are several naming conventions used throughout this document. They can be found in the following table:

Symbol	Explanation
name# / name_B	Denotes a low active signal
name- / name_N	Denotes the negative signal of a differential pair
name+ / name_P	Denotes the positive signal of a differential pair
←	Denotes the signal flow in the direction shown
→	Denotes the signal flow in the direction shown
↔	Denotes the signal flow in both directions
I/O / INOUT	Denotes a bidirectional pin
IN	Denotes an input pin. Signal flow is *from* carrier board *to* SoM
OUT	Denotes an output pin. Signal flow is *from* SoM *to* carrier board
matched	Denotes the according signal to be routed impedance controlled and length matched
Pin 1	Refers to the numeric pin of a component package
Pin a1	Refers to the array position of a pin within a component package

Table 2: *Conventions*

3.9 Climatic Conditions

The relative humidity during operation or storage of the module may not exceed 10% to 90%, non-condensing.

3.10 RoHS

All components on the CRX-IMX95 are RoHS compliant, also a RoHS compliant soldering process is used for manufacturing.

3.11 Storage Temperature

The storage temperature is -40℃ - +85℃.

Storage Temperatur lässt sich nicht exakt klären

4 Short Description

The SBC-IMX95 is a small computer system consisting of

- the MPX-IMX95 module, based on NXP's IMX95 CPU
- CRX-IMX95 carrier board

It targets both

- evaluation of the respective MPX-IMX95 SoM
- direct usage as an industrial computing solution

This document gives you an overview on the board's hardware features and capabilities and how to take the first steps on the initial setup.

5 Quick Start Guide

This quick start guide describes the first steps to operate the evaluation board consisting of CRX-IMX95 and MPX-IMX95 SoM.

5.1 Prerequisites

5.1.1 Unpacking

Before using the setup for the first time, unpack the unit and make sure that it is clean and free of foreign objects. Please exclude visible transport damage.

Always make sure to handle the evaluation board unit ESD-safe! Otherwise, the unit may suffer permanent damage.
However, do not place the unit directly flat on a metal surface, as this may result in short circuits and damage to the board.

5.1.2 System Setup

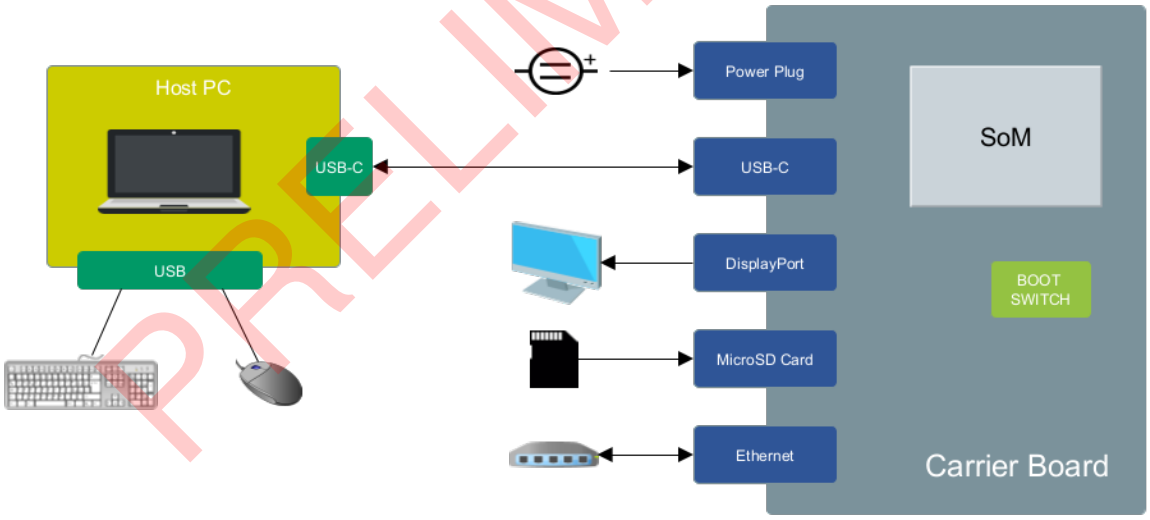


Figure 1: *Evaluation board system setup*

The evaluation kit usually arrives fully mounted including SoM and heatspreader (with thermal pad). If this is not the case, take a look at chapter Mounting / Unmounting. Optional adapter boards can be connected via ST19.

An overview of all connectors and switches can be found in chapter Connector Overview.

5.1.3 Host Computer

Host computer and evaluation board establish a connection by USB cable. The host PC is running a terminal software (e.g. TeraTerm, HyperTerminal, putty, Kermit...) with the following parameters:

- 115200 Baud
- 8 data bits
- no parity
- 1 stop bit

USB connection is converted to UART on the carrierboard. Therefore, there will be three console windows, one for each UART and core, respectively (see table 21). Choose UART1 for A55 cores.

5.2 Board Preparation and Power Up

After mounting, please follow the next steps:

1. Insert a MicroSD card in ST4.
2. Set boot selection switch to boot from MicroSD card.
3. Connect a USB-C cable to ST22 in order to establish a debug connection.
4. *Optionally* connect a monitor to DisplayPort connector ST3.
5. *Optionally* connect a CAT5e cable to either RJ45 connector ST11 or ST12.
6. Connect a power cable to ST13.
7. Connect a power supply (9-24V) that is capable of providing enough electrical power for all peripheral consumer devices (USB-C, M.2 cards, LVDS displays, ...)
8. The system will start automatically.

5.3 Operation

When the evaluation kit is powered, several green LEDs are illuminated. The red LED must be off.

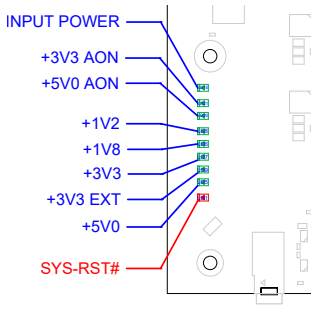


Figure 2: *Minimum numbers of LEDs*

The console window shows U-boot and Linux starting. When finished, the user has to enter ***root*** after the prompt, no password is required.

For detailed setup instructions, refer to the readme document delivered along with the unit!

5.4 Accessories

Interface	Type	Order Code	Specification
Main Power Supply	Power connector	Phoenix Contact FKCN 2,5/ 3-ST-5,08	2 out of 3 pins used, additional cables required
LVDS	Display with touch	Newhaven NHD-10.1-1024600BF-LSXP-CTP	10.1 inch, 1024 x 600, Capacitive Touch Panel
	LVDS display FFC cable	Würth 687740200002	40pin, 20cm, opposite side contacts
	Touch cable extension (optional)	Consumer product	6pin, 20cm
MIPI-CSI	Camera	Vision Components VC MIPI IMX415C	1/2.8" Sony IMX415C, color, 8.3 Mpixel, 4 lanes, 4k, 60FPS, 10bit
	Camera FFC cable	Vision Components MIPI FPC cable 200/22-22	22pin, 20cm, same side contacts

Table 3: *MicroSys' test setup*

6 System Description

6.1 Block Diagram

The system architecture is displayed in Figure 3:

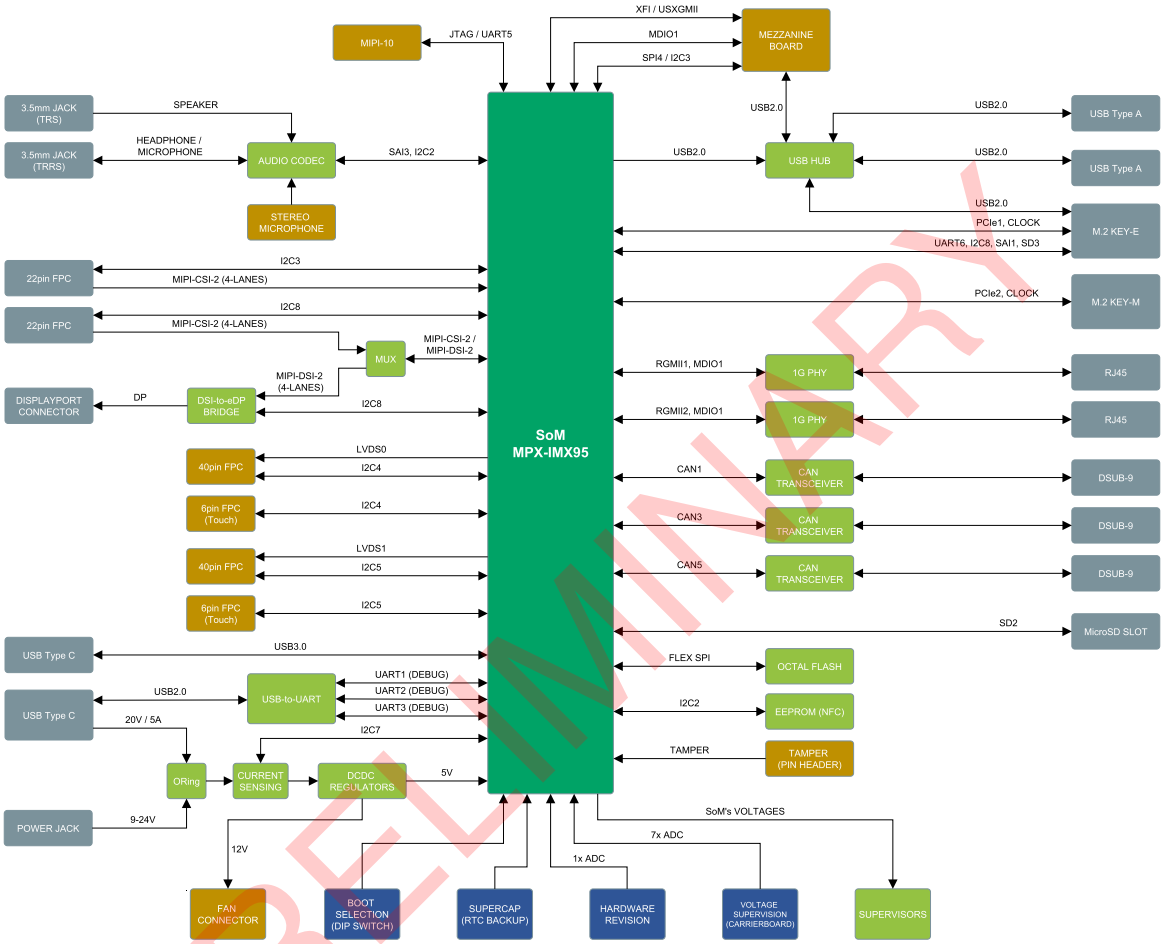


Figure 3: *Block diagram CRX-IMX95*

6.2 Feature Overview

The SBC-IMX95 offers the features listed in table 5.

Feature	Interface	Description
Processor	NXP i.MX95 on MPX-IMX95 SoM	■ up to 2GHz ■ 6x Arm Cortex-A55 ■ 1x Cortex-M33 ■ 1x Cortex-M7
DRAM	LPDDR5 interface	■ up to 16 GBytes ■ max. 6400 MT/s ■ 32-bit
Boot Devices	Selectable via DIP switch	■ eMMC ■ MicroSD card ■ Octal Flash
Ethernet	RGMII, XFI/USXGMII	■ 2x 10/100/1000 Mbps on RJ-45 ■ 1G ports with Wake-on-LAN support ■ 1x 10G via adapterboard
Extension Board	Mezzanine connector	use with adapterboards
JTAG	JTAG interface	10-pin MIPI header
I²C	I²C interface	■ 1x EEPROM (with NFC) ■ 2x Touch Controller ■ 2x Camera ■ 1x M.2 Key-E ■ 1x Mezzanine board ■ GPIO Expanders
CAN	CAN FD interface	■ 3x CAN-FD on DSUB-9 connectors ■ Wake-on-CAN support
MIPI-CSI	MIPI-CSI interface	up to 2x MIPI-CSI with 4 lanes each
MIPI-DSI	MIPI-DSI interface	up to 1x MIPI-DSI with 4 lanes
LVDS	LVDS interface	2x LVDS interface with 4 lanes each and touch interface
Audio	I²S interface	■ Stereo microphone input ■ 1x Line Out ■ 1x Headphone Out with microphone
USB	USB2.0 / 3.0	■ 1x USB3.0 on Type C connector ■ 2x USB2.0 on Type A connectors ■ 1x USB2.0 on M.2 Key-M ■ 1x USB2.0 on adapterboard (mezzanine connector)

Voltage Supervision	ADC & supervisor circuit	■ ADC monitors carrier board voltages ■ supervisors monitor SoM's voltages
Debug Port	UART debug ports (converted to USB)	Separate UARTs for: ■ Cortex-A55 ■ Cortex-M33 ■ Cortex-M7
Tamper Detection	Tamper pins	Tamper detection pins on pin header
Power Management	Primary supply	Input: 9-24V DC via power jack
	Secondary supply	Input: 20V DC via USB-C
	Backup supply RTC	Supercap

Table 5: *Feature overview*

6.3 Ordering Information

Ordering information can be found on the following website
https://microsys.de/products/crx-i-mx95/
or contact your local sales representative.

6.4 Power Consumption

The use case plays an important role for power consumption measurements, as well as ambient and operating temperature. Therefore, the numbers in table 6 are to be seen as an approximation only.

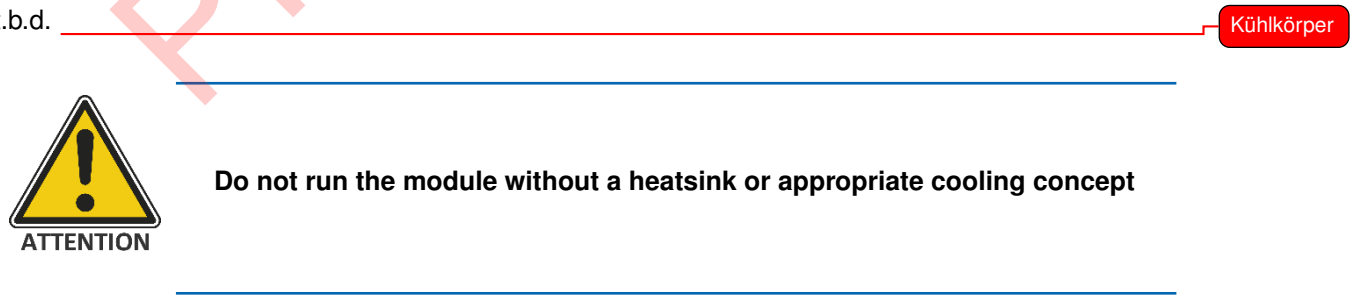
Typical power consumption values for the CRX-IMX95 module are determined on a CRX-IMX95 carrier board running Linux. Measurements are taken with the power sensor MAX9611 (12V input voltage) at room temperature. All cores are active, but power management has not been optimised yet. Take into account, that parts of the CPU are consuming power even if not actively used.

Use Case	Total Power Consumption including SoM
Uboot, prompt	≈ 4,9 W
Linux, idle	≈ 4,4 W
Linux, stressapptest	≈ 8,0 W
Linux, urandom generator	≈ 6,4 W
Linux, 2x 1 GBit Ethernet connection	≈ 5,3 W
Linux, 2x 1 GBit Ethernet connection with 1x 1 GBit iperf3	≈ 5,9 W
Linux, Displayport & 1x LVDS display	≈ 7,8 W

Table 6: *Power consumption at room temperature*

6.5 Cooling

t.b.d.



7 Technical Description

7.1 Connector Overview

The CRX-IMX95 has connectors on top and bottom side. They are listed in the following table 7 along with their designators which are printed on PCB.

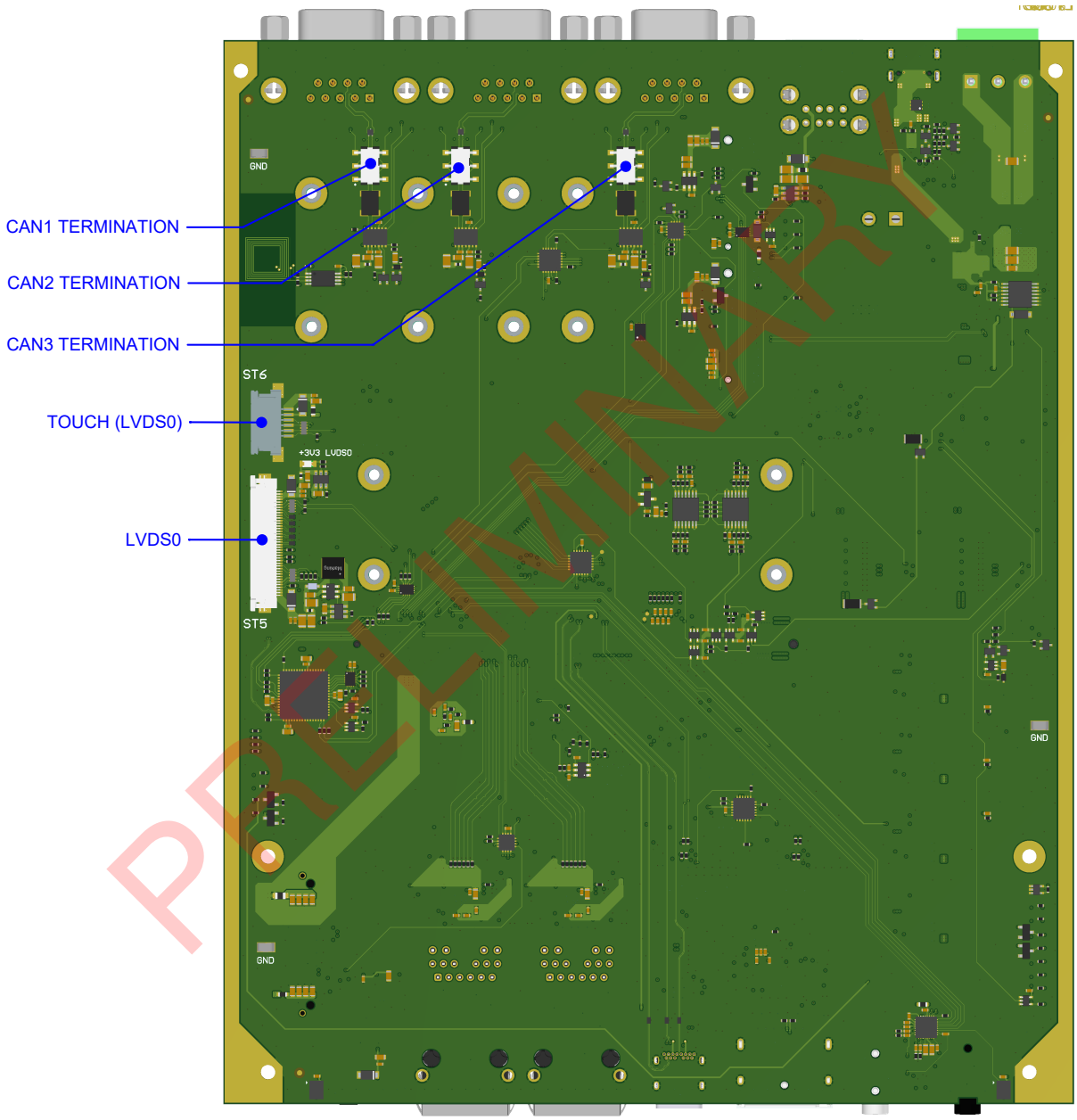


Figure 4: *Bottom side connectors*

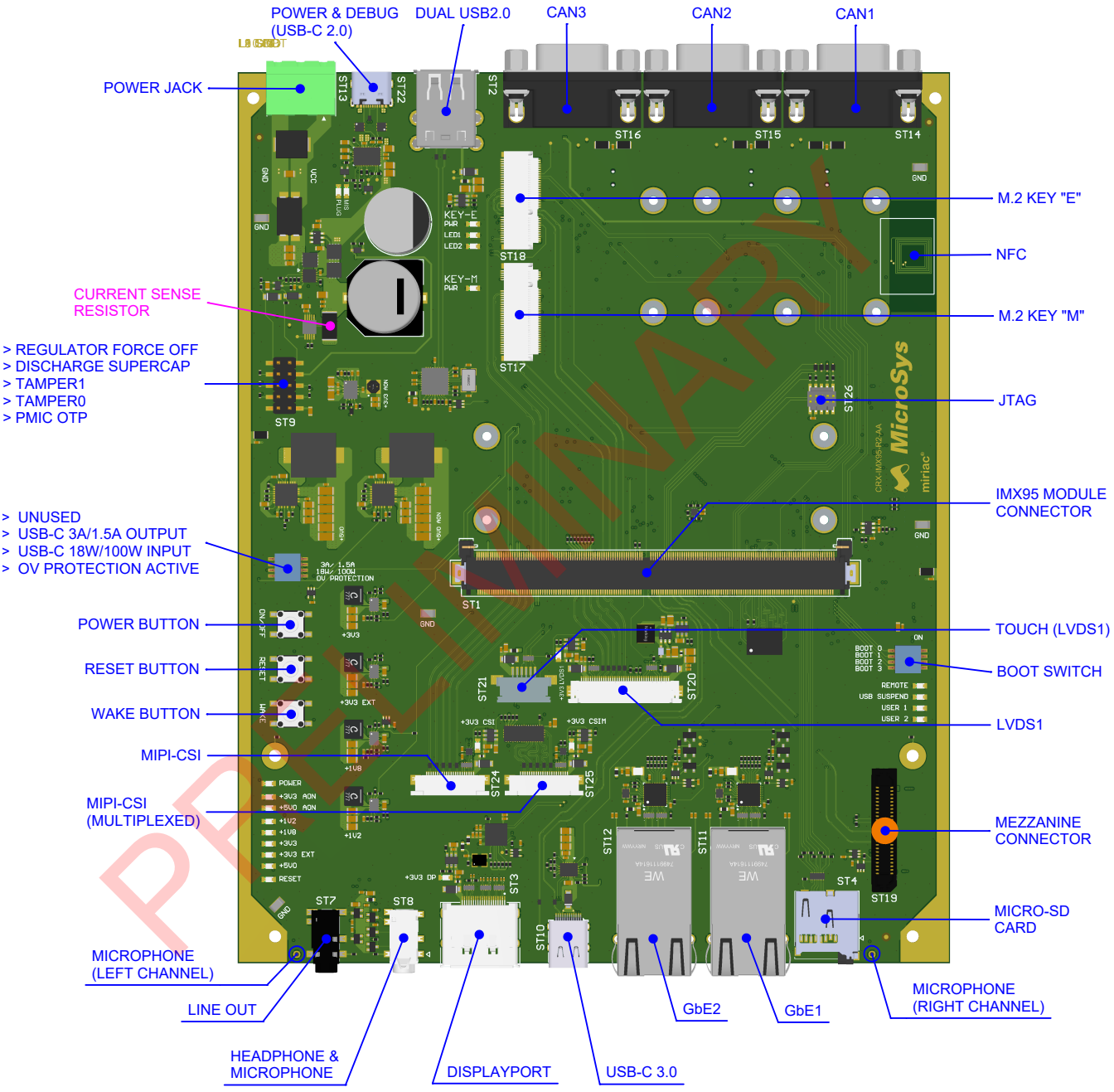


Figure 5: *Top side connectors*

Designator	PCB Side	Interface	Connector Type	Mates with
ST1	Top	IMX95 Module	MM70-314B1-2-R300	MicroSys MPX-IMX95 module
ST2	Top	USB2.0	Dual USB Type A	USB Type A cables
ST3	Top	Displayport	Displayport	Displayport cables
ST4	Top	SD Card	microSD card slot	microSD cards
ST5	Bottom	LVDS Display	54104-4031	Newhaven NHD-10.1-1024600BF-LSXP-CTP display
ST6	Bottom	I^2C Touch	522070685	Newhaven NHD-10.1-1024600BF-LSXP-CTP display
ST7	Top	Line Out	3.5mm Audio Jack (TRS)	Three contact (TRS) audio jacks
ST8	Top	Headphone Out	3.5mm Audio Jack (TRRS)	Four contact (TRRS) audio jacks
ST9	Top	Custom Pinout	2.54mm 4-pin header	Cables, jumpers, ...
ST10	Top	USB 3.0 / USB2.0	USB-C	USB-C cables
ST11	Top	Gigabit Ethernet	RJ45 with LEDs	Ethernet cables, e.g. CAT5e
ST12	Top	Gigabit Ethernet	RJ45 with LEDs	Ethernet cables, e.g. CAT5e
ST13	Top	Main Power Supply	Phoenix Contact 1759020	different options, for example FKCN 2,5/ 3-ST-5,08 or IC 2,5/ 3-ST-5,08 . . .
ST14	Top	CAN bus	DSUB-9 socket	CAN header (pinout CiA® 106)
ST15	Top	CAN bus	DSUB-9 socket	CAN header (pinout CiA® 106)
ST16	Top	CAN bus	DSUB-9 socket	CAN header (pinout CiA® 106)
ST17	Bottom	M.2 Key M	M.2 Key M socket	M.2 Key M cards
ST18	Bottom	M.2 Key E	M.2 Key E socket	M.2 Key E cards
ST19	Top	Custom Pinout	Samtec ERF8-025-09.0-L-DV-K-TR	adapter designed by MicroSys
ST20	Top	LVDS Display	54104-4031	Newhaven NHD-10.1-1024600BF-LSXP-CTP display
ST21	Top	I^2C Touch	522070685	Newhaven NHD-10.1-1024600BF-LSXP-CTP display
ST22	Top	USB-C 2.0 sink only	USB-C 2.0 connector	USB-C cables
ST24	Top	MIPI-CSI	5051102296	Cameras connected via 22-pin FFC cable (e.g. Vision Components)
ST25	Top	MIPI-CSI	5051102296	Cameras connected via 22-pin FFC cable (e.g. Vision Components)
ST26	Top	JTAG	FTSH-105-01-L-DV-K	Connectors with MIPI-10 pinout

Table 7: *Connector overview*

7.2 Module Connector (Top Pinout)

Pin	Primary Name	Pin Usage	Usage	CPU Ball	GPIO	Supply Voltage
T1	I2C1-SCL	I2C1-SCL	I2C	D48	—	+3V3
T2	I2C1-SDA	I2C1-SDA	I2C	D52	—	+3V3
T3	I2C2-SCL	I2C2-SCL	I2C	E43	gpio1.IO[2]	+3V3
T4	I2C2-SDA	I2C2-SDA	I2C	E45	gpio1.IO[3]	+3V3
T5	GND	GND				
T6	PDM-CLK/CAN1-TX	CAN1-TX	CAN	F46	gpio1.IO[8]	+3V3
T7	PDM-BS0/CAN1-RX	CAN1-RX	CAN	G45	gpio1.IO[9]	+3V3
T8	AON-IRQ#	AON-IRQ#	IRQ	—	—	+3V3
T9	GND	GND				
T10	SDHC2-D2	SDHC2-D2	MICRO SD	AA51	gpio3.IO[5]	+1V8/3V3
T11	SDHC2-D3	SDHC2-D3	MICRO SD	AA49	gpio3.IO[6]	+1V8/3V3
T12	SDHC2-CMD	SDHC2-CMD	MICRO SD	AB52	gpio3.IO[2]	+1V8/3V3
T13	SDHC2-CLK	SDHC2-CLK	MICRO SD	AB48	gpio3.IO[1]	+1V8/3V3
T14	GND	GND				
T15	SDHC2-D0	SDHC2-D0	MICRO SD	AC51	gpio3.IO[3]	+1V8/3V3
T16	SDHC2-D1	SDHC2-D1	MICRO SD	AC49	gpio3.IO[4]	+1V8/3V3
T17	SDHC2-CD#	SDHC2-CD#	MICRO SD	AD48	gpio3.IO[0]	+1V8/3V3
T18	SDHC2-RST#	SDHC2-RST#	MICRO SD	AD52	gpio3.IO[7]	+1V8/3V3
T19	GND	GND				
T20	SDHC3-D0	SDHC3-D0	M.2 KEY-E	AG49	gpio3.IO[22]	+1V8
T21	SDHC3-D1	SDHC3-D1	M.2 KEY-E	AH52	gpio3.IO[23]	+1V8
T22	SDHC3-D2	SDHC3-D2	M.2 KEY-E	AE49	gpio3.IO[24]	+1V8
T23	SDHC3-D3	SDHC3-D3	M.2 KEY-E	AF52	gpio3.IO[25]	+1V8
T24	GND	GND				
T25	SDHC3-CLK	SDHC3-CLK	M.2 KEY-E	AG51	gpio3.IO[20]	+1V8
T26	SDHC3-CMD	SDHC3-CMD	M.2 KEY-E	AF48	gpio3.IO[21]	+1V8
T27	GND	GND				
T28	XSPI-DATA7	XSPI-DATA7	OCTAL FLASH	AH50	gpio5.IO[7]	+1V8
T29	XSPI-DATA6	XSPI-DATA6	OCTAL FLASH	AJ51	gpio5.IO[6]	+1V8
T30	XSPI-DATA5	XSPI-DATA5	OCTAL FLASH	AK50	gpio5.IO[5]	+1V8
T31	XSPI-DATA4	XSPI-DATA4	OCTAL FLASH	AJ49	gpio5.IO[4]	+1V8

T32	XSPI-DATA3	XSPI-DATA3	OCTAL FLASH	AK48	gpio5.IO[3]	+1V8
T33	XSPI-DATA2	XSPI-DATA2	OCTAL FLASH	AJ47	gpio5.IO[2]	+1V8
T34	XSPI-DATA1	XSPI-DATA1	OCTAL FLASH	AH46	gpio5.IO[1]	+1V8
T35	XSPI-DATA0	XSPI-DATA0	OCTAL FLASH	AJ45	gpio5.IO[0]	+1V8
T36	GND	GND				
T37	XSPI-DQS	XSPI-DQS	OCTAL FLASH	AK44	gpio5.IO[8]	+1V8
T38	XSPI-CLK	XSPI-CLK	OCTAL FLASH	AJ43	gpio5.IO[9]	+1V8
T39	XSPI-SS1#	XSPI-SS1#	OCTAL FLASH	AH42	gpio5.IO[11]	+1V8
T40	XSPI-SS0#	XSPI-SS0#	OCTAL FLASH	AJ41	gpio5.IO[10]	+1V8
T41	GND	GND				
T42	GPIO4-IO0	unused	unused	AK40	gpio4.IO[0]	+1V8
T43	GPIO4-IO1	unused	unused	AJ39	gpio4.IO[1]	+1V8
T44	GND	GND				
T45	RGMII1-RX-D3	RGMII1-RX-D3	ETHERNET	AH38	gpio4.IO[13]	+1V8
T46	RGMII1-RX-D2	RGMII1-RX-D2	ETHERNET	AJ37	gpio4.IO[12]	+1V8
T47	RGMII1-RX-D1	RGMII1-RX-D1	ETHERNET	AK36	gpio4.IO[11]	+1V8
T48	RGMII1-RX-D0	RGMII1-RX-D0	ETHERNET	AJ35	gpio4.IO[10]	+1V8
T49	GND	GND				
T50	RGMII1-RX-CTL	RGMII1-RX-CTL	ETHERNET	AH34	gpio4.IO[8]	+1V8
T51	RGMII1-RX-CLK	RGMII1-RX-CLK	ETHERNET	AJ33	gpio4.IO[9]	+1V8
T52	GND	GND				
T53	MDC	MDC	ETHERNET	AK32	gpio4.IO[14]	+1V8
T54	MDIO	MDIO	ETHERNET	AJ31	gpio4.IO[15]	+1V8
T55	GND	GND				
T56	RGMII2-RX-D3	RGMII2-RX-D3	ETHERNET	AH30	gpio4.IO[27]	+1V8
T57	RGMII2-RX-D2	RGMII2-RX-D2	ETHERNET	AJ29	gpio4.IO[26]	+1V8
T58	RGMII2-RX-D1	RGMII2-RX-D1	ETHERNET	AK28	gpio4.IO[25]	+1V8
T59	RGMII2-RX-D0	RGMII2-RX-D0	ETHERNET	AJ27	gpio4.IO[24]	+1V8
T60	GND	GND				
T61	RGMII2-RX-CTL	RGMII2-RX-CTL	ETHERNET	AH26	gpio4.IO[20]	+1V8
T62	RGMII2-RX-CLK	RGMII2-RX-CLK	ETHERNET	AJ25	gpio4.IO[21]	+1V8
T63	GND	GND				
T64	CCM-CLKO4	CCM-CLKO4	M.2 KEY-E SUSCLK	AJ21	gpio4.IO[29]	+1V8
T65	CCM-CLKO3	unused	unused	AK20	gpio4.IO[28]	+1V8
T66	CCM-CLKO2	unused	unused	AF20	gpio4.IO[27]	+1V8
T67	CCM-CLKO1	unused	unused	AH20	gpio4.IO[26]	+1V8

T68	GND	GND				
T69	ETH-TX0_P	ETH-TX0_P	MEZZANINE (ETHERNET)	AJ17	—	+0V8
T70	ETH-TX0_N	ETH-TX0_N	MEZZANINE (ETHERNET)	AK16	—	+0V8
T71	GND	GND				
T72	ETH-RX0_P	ETH-RX0_P	MEZZANINE (ETHERNET)	AJ13	—	+0V8
T73	ETH-RX0_N	ETH-RX0_N	MEZZANINE (ETHERNET)	AK12	—	+0V8
T74	GND	GND				
T75	USB1-SSRX0_N	USB1-SSRX0_N	USB-C 3.0	D26	—	+0V8
T76	USB1-SSRX0_P	USB1-SSRX0_P	USB-C 3.0	E25	—	+0V8
T77	GND	GND				
T78	USB1-SSTX0_N	USB1-SSTX0_N	USB-C 3.0	A21	—	+0V8
T79	USB1-SSTX0_P	USB1-SSTX0_P	USB-C 3.0	B20	—	+0V8
T80	GND	GND				
T81	USB1-D_P	USB1-D_P	USB-C 3.0	C19	—	+3V3
T82	USB1-D_N	USB1-D_N	USB-C 3.0	B18	—	+3V3
T83	GND	GND				
T84	LVDS0-D3_P	LVDS0-D3_P	LVDS DISPLAY 1	D8	—	+1V8
T85	LVDS0-D3_N	LVDS0-D3_N	LVDS DISPLAY 1	E9	—	+1V8
T86	GND	GND				
T87	LVDS0-CLK_P	LVDS0-CLK_P	LVDS DISPLAY 1	B4	—	+1V8
T88	LVDS0-CLK_N	LVDS0-CLK_N	LVDS DISPLAY 1	A5	—	+1V8
T89	GND	GND				
T90	LVDS0-D2_P	LVDS0-D2_P	LVDS DISPLAY 1	D6	—	+1V8
T91	LVDS0-D2_N	LVDS0-D2_N	LVDS DISPLAY 1	E7	—	+1V8
T92	GND	GND				
T93	LVDS0-D1_P	LVDS0-D1_P	LVDS DISPLAY 1	F6	—	+1V8
T94	LVDS0-D1_N	LVDS0-D1_N	LVDS DISPLAY 1	F8	—	+1V8
T95	GND	GND				
T96	LVDS0-D0_P	LVDS0-D0_P	LVDS DISPLAY 1	G7	—	+1V8
T97	LVDS0-D0_N	LVDS0-D0_N	LVDS DISPLAY 1	G9	—	+1V8
T98	GND	GND				
T99	LVDS1-D3_P	LVDS1-D3_P	LVDS DISPLAY 2	F2	—	+1V8
T100	LVDS1-D3_N	LVDS1-D3_N	LVDS DISPLAY 2	F4	—	+1V8
T101	GND	GND				
T102	LVDS1-CLK_P	LVDS1-CLK_P	LVDS DISPLAY 2	D2	—	+1V8
T103	LVDS1-CLK_N	LVDS1-CLK_N	LVDS DISPLAY 2	D4	—	+1V8

T104	GND	GND				
T105	LVDS1-D2_P	LVDS1-D2_P	LVDS DISPLAY 2	E1	—	+1V8
T106	LVDS1-D2_N	LVDS1-D2_N	LVDS DISPLAY 2	E3	—	+1V8
T107	GND	GND				
T108	LVDS1-D1_P	LVDS1-D1_P	LVDS DISPLAY 2	C1	—	+1V8
T109	LVDS1-D1_N	LVDS1-D1_N	LVDS DISPLAY 2	C3	—	+1V8
T110	GND	GND				
T111	LVDS1-D0_P	LVDS1-D0_P	LVDS DISPLAY 2	B2	—	+1V8
T112	LVDS1-D0_N	LVDS1-D0_N	LVDS DISPLAY 2	A3	—	+1V8
T113	GND	GND				
T114	MIPI-DSI-CSI-D3_P	MIPI-DSI-CSI-D3_P	MIPI-CSI / DISPLAYPORT	B6	—	+1V8
T115	MIPI-DSI-CSI-D3_N	MIPI-DSI-CSI-D3_N	MIPI-CSI / DISPLAYPORT	C7	—	+1V8
T116	GND	GND				
T117	MIPI-DSI-CSI-D2_P	MIPI-DSI-CSI-D2_P	MIPI-CSI / DISPLAYPORT	B8	—	+1V8
T118	MIPI-DSI-CSI-D2_N	MIPI-DSI-CSI-D2_N	MIPI-CSI / DISPLAYPORT	A9	—	+1V8
T119	GND	GND				
T120	MIPI-DSI-CSI-CLK_P	MIPI-DSI-CSI-CLK_P	MIPI-CSI / DISPLAYPORT	B10	—	+1V8
T121	MIPI-DSI-CSI-CLK_N	MIPI-DSI-CSI-CLK_N	MIPI-CSI / DISPLAYPORT	C11	—	+1V8
T122	GND	GND				
T123	MIPI-DSI-CSI-D1_P	MIPI-DSI-CSI-D1_P	MIPI-CSI / DISPLAYPORT	B12	—	+1V8
T124	MIPI-DSI-CSI-D1_N	MIPI-DSI-CSI-D1_N	MIPI-CSI / DISPLAYPORT	A13	—	+1V8
T125	GND	GND				
T126	MIPI-DSI-CSI-D0_P	MIPI-DSI-CSI-D0_P	MIPI-CSI / DISPLAYPORT	B14	—	+1V8
T127	MIPI-DSI-CSI-D0_N	MIPI-DSI-CSI-D0_N	MIPI-CSI / DISPLAYPORT	C15	—	+1V8
T128	GND	GND				
T129	+1V8/3V3-SD2	+1V8/3V3-SD2	MICRO SD			+1V8/3V3
T130	+3V3-SD2	+3V3-SD2	MICRO SD			+3V3
T131	MIPI-CSI-D3_P	MIPI-CSI-D3_P	MIPI-CSI	E11	—	+1V8
T132	MIPI-CSI-D3_N	MIPI-CSI-D3_N	MIPI-CSI	F12	—	+1V8
T133	GND	GND				
T134	MIPI-CSI-D2_P	MIPI-CSI-D2_P	MIPI-CSI	E13	—	+1V8
T135	MIPI-CSI-D2_N	MIPI-CSI-D2_N	MIPI-CSI	D14	—	+1V8
T136	GND	GND				
T137	MIPI-CSI-CLK_P	MIPI-CSI-CLK_P	MIPI-CSI	E15	—	+1V8
T138	MIPI-CSI-CLK_N	MIPI-CSI-CLK_N	MIPI-CSI	F16	—	+1V8
T139	GND	GND				

T140	MIPI-CSI-D1_P	MIPI-CSI-D1_P	MIPI-CSI	E17	—	+1V8
T141	MIPI-CSI-D1_N	MIPI-CSI-D1_N	MIPI-CSI	D18	—	+1V8
T142	GND	GND				
T143	MIPI-CSI-D0_P	MIPI-CSI-D0_P	MIPI-CSI	E19	—	+1V8
T144	MIPI-CSI-D0_N	MIPI-CSI-D0_N	MIPI-CSI	F20	—	+1V8
T145	GND	GND				
T146	GND	GND				
T147	GND	GND				
T148	GND	GND				
T149	GND	GND				
T150	GND	GND				
T151	+5V0-AON	+5V0-AON				+5V0
T152	+5V0-AON	+5V0-AON				+5V0
T153	+5V0-AON	+5V0-AON				+5V0
T154	+5V0-AON	+5V0-AON				+5V0
T155	+5V0-AON	+5V0-AON				+5V0
T156	+5V0-AON	+5V0-AON				+5V0

Table 8: *Module connector: top pinout*

7.3 Module Connector (Bottom Pinout)

Pin	Primary Name	Pin Usage	Usage	CPU Ball	GPIO	Supply Voltage
B1	+VCC-BAT	+VCC-BAT	RTC BACKUP	—		+5V0
B2	UART1-RXD	UART1-RXD	UART: DEBUG	E49	gpio1.IO[4]	+3V3
B3	UART1-TXD/BOOT0	UART1-TXD/BOOT0	UART: DEBUG & BOOT PIN	F52	gpio1.IO[5]	+3V3
B4	UART2-RXD	UART2-RXD	UART: DEBUG	E51	gpio1.IO[6]	+3V3
B5	UART2-TXD/BOOT1	UART2-TXD/BOOT1	UART: DEBUG & BOOT PIN	F48	gpio1.IO[7]	+3V3
B6	GND	GND				
B7	SAI1-TXC	SAI1-TXC	M.2 KEY-E	G51	gpio1.IO[12]	+3V3
B8	SAI1-TXFS/BOOT2	SAI1-TXFS/BOOT2	M.2 KEY-E & BOOT PIN	G49	gpio1.IO[11]	+3V3
B9	SAI1-TXD0/BOOT3	SAI1-TXD0/BOOT3	M.2 KEY-E	H48	gpio1.IO[13]	+3V3
B10	SAI1-RXD0	SAI1-RXD0	M.2 KEY-E & BOOT PIN	H52	gpio1.IO[14]	+3V3
B11	GND	GND				
B12	GPIO-IO00	GPIO-IO00	I2C3	J49	gpio2.IO[0]	+3V3
B13	GPIO-IO01	GPIO-IO01	I2C3	J51	gpio2.IO[1]	+3V3
B14	GPIO-IO02	GPIO-IO02	I2C4	K48	gpio2.IO[2]	+3V3
B15	GPIO-IO03	GPIO-IO03	I2C4	K52	gpio2.IO[3]	+3V3
B16	GPIO-IO04	GPIO-IO04	UART6	K46	gpio2.IO[4]	+3V3
B17	GPIO-IO05	GPIO-IO05	UART6	L45	gpio2.IO[5]	+3V3
B18	GPIO-IO06	GPIO-IO06	UART6	L49	gpio2.IO[6]	+3V3
B19	GPIO-IO07	GPIO-IO07	UART6	L51	gpio2.IO[7]	+3V3
B20	GPIO-IO08	GPIO-IO08	I2C7	M44	gpio2.IO[8]	+3V3
B21	GND	GND				
B22	GPIO-IO09	GPIO-IO09	I2C7	M46	gpio2.IO[9]	+3V3
B23	GPIO-IO10	GPIO-IO10	I2C8	M48	gpio2.IO[10]	+3V3
B24	GPIO-IO11	GPIO-IO11	I2C8	M52	gpio2.IO[11]	+3V3
B25	GPIO-IO12	GPIO-IO12	TOUCH0 IRQ	N45	gpio2.IO[12]	+3V3
B26	GPIO-IO13	GPIO-IO13	TOUCH1 IRQ	N49	gpio2.IO[13]	+3V3
B27	GPIO-IO14	GPIO-IO14	UART3	N51	gpio2.IO[14]	+3V3
B28	GPIO-IO15	GPIO-IO15	UART3	P44	gpio2.IO[15]	+3V3
B29	GPIO-IO16	GPIO-IO16	AUDIO CODEC	P46	gpio2.IO[16]	+3V3
B30	GPIO-IO17	GPIO-IO17	AUDIO CODEC	P48	gpio2.IO[17]	+3V3
B31	GND	GND				
B32	GPIO-IO18	GPIO-IO18	DISPLAY1 PWM	P52	gpio2.IO[18]	+3V3
B33	GPIO-IO19	GPIO-IO19	DISPLAY2 PWM	R45	gpio2.IO[19]	+3V3

B34	GPIO-IO20	GPIO-IO20	AUDIO CODEC	R49	gpio2.IO[20]	+3V3
B35	GPIO-IO21	GPIO-IO21	AUDIO CODEC	R51	gpio2.IO[21]	+3V3
B36	GPIO-IO22	GPIO-IO22	I2C5	T44	gpio2.IO[22]	+3V3
B37	GPIO-IO23	GPIO-IO23	I2C5	T46	gpio2.IO[23]	+3V3
B38	GPIO-IO24	GPIO-IO24	GPIO EXPANDER IRQ	T48	gpio2.IO[24]	+3V3
B39	GPIO-IO25	GPIO-IO25	unused	T52	gpio2.IO[25]	+3V3
B40	GPIO-IO26	GPIO-IO26	AUDIO CODEC	U45	gpio2.IO[26]	+3V3
B41	GPIO-IO27	GPIO-IO27	GPIO	U49	gpio2.IO[27]	+3V3
B42	GND	GND				
B43	GPIO-IO28	GPIO-IO28	CAN3	U51	gpio2.IO[28]	+3V3
B44	GPIO-IO29	GPIO-IO29	CAN3	V44	gpio2.IO[29]	+3V3
B45	GPIO-IO30	GPIO-IO30	CAN5	V46	gpio2.IO[30]	+3V3
B46	GPIO-IO31	GPIO-IO31	CAN5	V48	gpio2.IO[31]	+3V3
B47	GPIO-IO32	GPIO-IO32	MEZZANINE (SPI4)	V52	gpio5.IO[12]	+3V3
B48	GPIO-IO33	GPIO-IO33	MEZZANINE (SPI4)	W45	gpio5.IO[13]	+3V3
B49	GPIO-IO34	GPIO-IO34	MEZZANINE (SPI4)	W49	gpio5.IO[14]	+3V3
B50	GPIO-IO35	GPIO-IO35	MEZZANINE (SPI4)	W51	gpio5.IO[15]	+3V3
B51	GPIO-IO36	GPIO-IO36	MEZZANINE (SPI4)	Y48	gpio5.IO[16]	+3V3
B52	GPIO-IO37	GPIO-IO37	MEZZANINE (SPI4)	Y52	gpio5.IO[17]	+3V3
B53	GND	GND				
B54	AUD-N-HPD	unused	unused	Y46	—	+1V8
B55	AUD-AUX	unused	unused	AA45	—	+1V8
B56	AUD-P-UTIL	unused	unused	Y44	—	+1V8
B57	GND	GND				
B58	RGMII1-TX-D3	RGMII1-TX-D3	ETHERNET	AG37	gpio4.IO[2]	+1V8
B59	RGMII1-TX-D2	RGMII1-TX-D2	ETHERNET	AF36	gpio4.IO[3]	+1V8
B60	RGMII1-TX-D1	RGMII1-TX-D1	ETHERNET	AG35	gpio4.IO[4]	+1V8
B61	RGMII1-TX-D0	RGMII1-TX-D0	ETHERNET	AG33	gpio4.IO[5]	+1V8
B62	GND	GND				
B63	RGMII1-TX-CTL	RGMII1-TX-CTL	ETHERNET	AF32	gpio4.IO[6]	+1V8
B64	RGMII1-TX-CLK	RGMII1-TX-CLK	ETHERNET	AG31	gpio4.IO[7]	+1V8
B65	GND	GND				
B66	RGMII2-TX-D3	RGMII2-TX-D3	ETHERNET	AG29	gpio4.IO[16]	+1V8
B67	RGMII2-TX-D2	RGMII2-TX-D2	ETHERNET	AF28	gpio4.IO[17]	+1V8
B68	RGMII2-TX-D1	RGMII2-TX-D1	ETHERNET	AG27	gpio4.IO[18]	+1V8
B69	RGMII2-TX-D0	RGMII2-TX-D0	ETHERNET	AG25	gpio4.IO[19]	+1V8

B70	GND	GND				
B71	RGMII2-TX-CTL	RGMII2-TX-CTL	ETHERNET	AF24	gpio4.IO[20]	+1V8
B72	RGMII2-TX-CLK	RGMII2-TX-CLK	ETHERNET	AG23	gpio4.IO[21]	+1V8
B73	GND	GND				
B74	JTAG-TDI	JTAG-TDI	JTAG	AK24	gpio3.IO[28]	+1V8
B75	JTAG-TDO	JTAG-TDO	JTAG	AJ23	gpio3.IO[31]	+1V8
B76	JTAG-TMS	JTAG-TMS	JTAG	AH22	gpio3.IO[29]	+1V8
B77	JTAG-TCK	JTAG-TCK	JTAG	AG21	gpio3.IO[30]	+1V8
B78	GND	GND				
B79	USB1-SSTX1_P	USB1-SSTX1_P	USB-C 3.0	E21	—	+0V8
B80	USB1-SSTX1_N	USB1-SSTX1_N	USB-C 3.0	D22	—	+0V8
B81	GND	GND				
B82	USB1-SSRX1_P	USB1-SSRX1_P	USB-C 3.0	B16	—	+0V8
B83	USB1-SSRX1_N	USB1-SSRX1_N	USB-C 3.0	A17	—	+0V8
B84	RESERVED_B84	unused	unused			
B85	USB2-ID	USB2-ID	USB	F24	—	+1V8
B86	USB1-VBUS	USB1-VBUS	USB	E23	—	+3V3
B87	USB2-VBUS	USB2-VBUS	USB	E27	—	+3V3
B88	GND	GND				
B89	USB2-D_P	USB2-D_P	USB	B24	—	+3V3
B90	USB2-D_N	USB2-D_N	USB	A25	—	+3V3
B91	GND	GND				
B92	PCIE1-TX0_P	PCIE1-TX0_P	M.2 KEY-E	E29	—	+1V8
B93	PCIE1-TX0_N	PCIE1-TX0_N	M.2 KEY-E	D30	—	+1V8
B94	GND	GND				
B95	PCIE1-RX0_P	PCIE1-RX0_P	M.2 KEY-E	B28	—	+1V8
B96	PCIE1-RX0_N	PCIE1-RX0_N	M.2 KEY-E	A29	—	+1V8
B97	GND	GND				
B98	PCIE2-TX0_P	PCIE2-TX0_P	M.2 KEY-M	E31	—	+1V8
B99	PCIE2-TX0_N	PCIE2-TX0_N	M.2 KEY-M	F32	—	+1V8
B100	GND	GND				
B101	PCIE2-RX0_P	PCIE2-RX0_P	M.2 KEY-M	B34	—	+1V8
B102	PCIE2-RX0_N	PCIE2-RX0_N	M.2 KEY-M	C35	—	+1V8
B103	GND	GND				
B104	PCIE-CLKO_P	unused	unused	B26	—	+1V8
B105	PCIE-CLKO_N	unused	unused	C27	—	+1V8

B106	GND	GND				
B107	ADC-IN0	ADC-IN0	ADC	A37	—	+1V8
B108	ADC-IN1	ADC-IN1	ADC	B38	—	+1V8
B109	ADC-IN2	ADC-IN2	ADC	C39	—	+1V8
B110	ADC-IN3	ADC-IN3	ADC	B40	—	+1V8
B111	ADC-IN4	ADC-IN4	ADC	A41	—	+1V8
B112	ADC-IN5	ADC-IN5	ADC	B42	—	+1V8
B113	ADC-IN6	ADC-IN6	ADC	B44	—	+1V8
B114	ADC-IN7	ADC-IN7	ADC	A45	—	+1V8
B115	GND	GND				
B116	TAMPER0	TAMPER0	TAMPER	F36	—	+1V8-BBSM
B117	TAMPER1	TAMPER1	TAMPER	D38	—	+1V8-BBSM
B118	OV-ALRT#	OV-ALRT#	CONTROL	—	—	+3V3
B119	ONOFF	ONOFF	CONTROL	F40	—	+1V8-BBSM
B120	PON-RST#	PON-RST#	CONTROL	D42	—	+1V8-BBSM
B121	PWRON	PWRON	CONTROL	D44	—	+1V8-BBSM
B122	STBY	STBY	CONTROL	C43	—	+1V8-BBSM
B123	RESERVED_B123	unused	unused			
B124	RESERVED_B124	unused	unused			
B125	RESERVED_B125	unused	unused			
B126	PCIE2-CLKREQ#	PCIE2-CLKREQ#	M.2 KEY-M	—	—	+3V3
B127	PCIE1-CLKREQ#	PCIE1-CLKREQ#	M.2 KEY-E	—	—	+3V3
B128	GND	GND				
B129	PCIE2-CLKO_N	PCIE2-CLKO_N	M.2 KEY-M	—	—	+1V8
B130	PCIE2-CLKO_P	PCIE2-CLKO_P	M.2 KEY-M	—	—	+1V8
B131	GND	GND				
B132	PCIE1-CLKO_N	PCIE1-CLKO_N	M.2 KEY-E	—	—	+1V8
B133	PCIE1-CLKO_P	PCIE1-CLKO_P	M.2 KEY-E	—	—	+1V8
B134	GND	GND				
B135	SYS-RST#	SYS-RST#	CONTROL	—	—	+1V8
B136	SOC-STBY#	SOC-STBY#	CONTROL	—	—	+3V3
B137	ARM-STBY#	ARM-STBY#	CONTROL	—	—	+3V3
B138	+VCC-OTP-PF9	+VCC-OTP-PF9				t.b.d
B139	+VCC-ARM	+VCC-ARM				internal voltage
B140	+VCC-SOC	+VCC-SOC				internal voltage
B141	+1V8-PMIC-BBSM	+1V8-PMIC-BBSM				+1V8-BBSM

B142	+3V3-PF09	+3V3-PF09				+3V3
B143	+1V8-PF09	+1V8-PF09				+1V8
B144	+0V8-PF09	+0V8-PF09				internal voltage
B145	+0V5-PF09	+0V5-PF09				internal voltage
B146	+1V05-PF09	+1V05-PF09				internal voltage
B147	GND	GND				
B148	GND	GND				
B149	GND	GND				
B150	GND	GND				
B151	GND	GND				
B152	GND	GND				
B153	+5V0-AON	+5V0-AON				+5V0
B154	+5V0-AON	+5V0-AON				+5V0
B155	+5V0-AON	+5V0-AON				+5V0
B156	+5V0-AON	+5V0-AON				+5V0
B157	+5V0-AON	+5V0-AON				+5V0
B158	+5V0-AON	+5V0-AON				+5V0

Table 9: *Module connector: bottom pinout*

7.4 Miscellaneous Switch

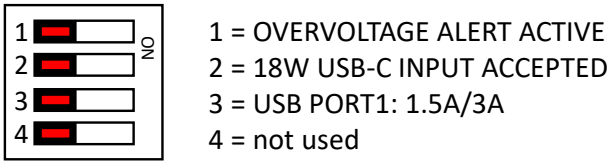


Figure 6: *DIP switch settings*

Signal	OFF (Default)	ON
Overvoltage	Overvoltage triggers an interrupt on the SoM. Power is not switched off.	Supply voltage is immediately switched off
18W USB-C mode	Power supply on USB-C input must provide at least 20V and 2A.	Power supply on USB-C input must provide at least 9V and 2A.
USB-C 3A output	USB-C output provides 5V and 1.5A	USB-C output provides 5V and 3A
not connected	—	—

Table 10: *DIP switch with different configuration settings*

7.5 Boot Switch

The SoC has four boot pins to choose boot device and the boot core.

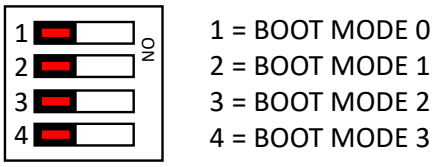


Figure 7: *DIP switch: boot selection*

BOOT3 basically selects which core to boot from. Booting from Serial NAND is not supported as there's no Serial NAND available on the CRX-IMX95 or on the SoM.

BOOT[3:0]	Boot Core	Boot Device	Description
0000	Cortex A55	Internal Fuses	
0001	Cortex A55	Serial Downloader	USB1 2.0 only, available on ST27
0010	Cortex A55	USDHC1 8-bit eMMC 5.1	eMMC on SoM
0011	Cortex A55	USDHC2 4-bit SD3.0	microSD Card (ST4)
0100	Cortex A55	FlexSPI Serial NOR	Octal Flash (see 7.14)
0101	Cortex A55	*Not supported on CRX-IMX95*	
0110	Cortex A55	*Reserved*	
0111	Cortex A55	*Reserved*	
1000	Cortex M33	Internal Fuses	
1001	Cortex M33	Serial Downloader	USB1 2.0 only, available on ST27
1010	Cortex M33	USDHC1 8-bit eMMC 5.1	eMMC on SoM
1011	Cortex M33	USDHC2 4-bit SD3.0	microSD Card (ST4)
1100	Cortex M33	FlexSPI Serial NOR	Octal Flash (see 7.14)
1101	Cortex M33	*Not supported on CRX-IMX95*	
1110	Cortex M33	*Reserved*	
1111	Cortex M33	*Reserved*	

Table 11: *Boot options*

7.6 LEDs

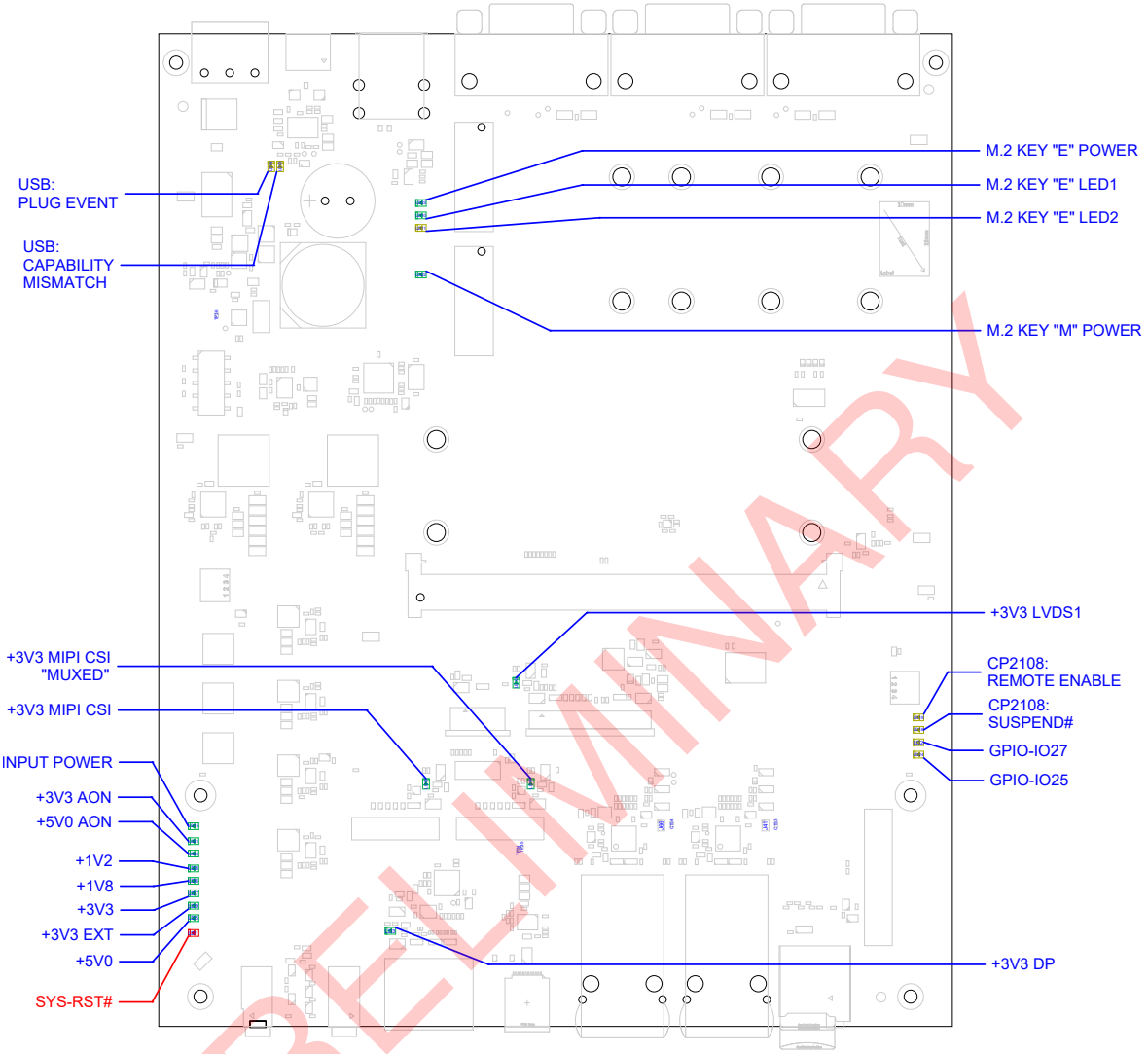


Figure 8: *Top side LEDs*

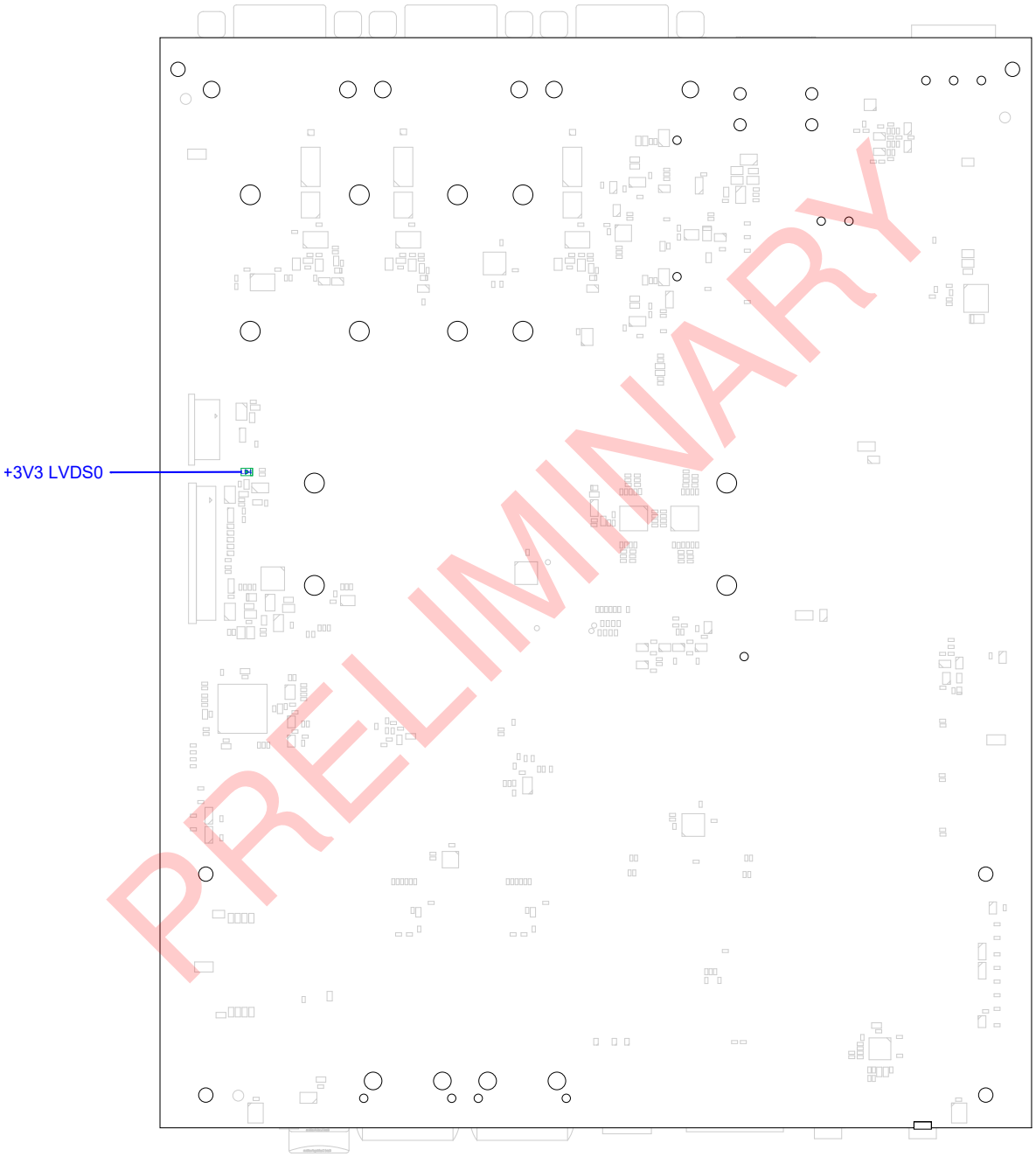


Figure 9: *Bottom side LEDs*

7.7 Testpoints

Several signals are available on test points. The complete list can be found in table 12:

Testpoint	Signal	Top	Bottom
TP1	+VBUS-USB-P1-CON	✓	
TP2	RESERVED_B84		✓
TP3	+VBUS-USB-P2-CON	✓	
TP4	USB-P3-EN	✓	
TP5	USB-P4-EN	✓	
TP6	DP-GPIO4	✓	
TP7	ETH1-CLKOUT	✓	
TP8	ETH2-CLKOUT	✓	
TP9	SDHC2-RST#	✓	
TP10	CAN1-ERR#	✓	
TP11	CAN2-ERR#	✓	
TP12	CAN3-ERR#	✓	
TP13	M2-KYE-ALERT#	✓	
TP14	FORCE-OFF#	✓	
TP15	TYPEC-SINK-EN#	✓	
TP16	TYPEC-FAULTIN#	✓	
TP17	CRNT-SENSE-OUT	✓	
TP18	CAN1-WAKE	✓	
TP19	CAN2-WAKE	✓	
TP20	CAN3-WAKE	✓	
TP21	PCIE-CLKO_P		✓
TP22	PCIE-CLKO_N		✓
TP23	GND		✓
TP24	GND	✓	
TP25	GND	✓	
TP26	GND	✓	
TP27	GND	✓	

TP28	GND	✓	
TP29	GND	✓	
TP30	GND		✓
TP31	GPX-0X76-P17		✓
TP32	GPX-0X22-P05	✓	
TP33	GPX-0X22-P06	✓	
TP34	I2C8-SCL-1V8	✓	
TP35	I2C8-SDA-1V8	✓	
TP36	DISCHARGE	✓	

Table 12: *Testpoints*

7.8 Power Rails

A few power rails are generated on the CRX-IMX95 and some of the rails of the SoM are also used, for example for voltage tracking or signal buffering. Table 13 gives an overview.

Power Rail	Nominal Voltage Range	Description
+VIN	9-24V (Power Jack) / 20V (USB-C)	Carrier board input supply voltage
+12V0	11.4V - 12.6V	Display supply voltage
+5V0	4.75V - 5.25V	USB, CAN supply voltage
+5V0-AON	4.75V - 5.25V	i.MX95 supply voltage
+3V3-AON	3.13V - 3.47V	Ethernet supply voltage
+3V3	3.13V - 3.47V	USB, Display, MIPI, Touch, DisplayPort, Camera, Audio, Clock, CAN supply voltage
+3V3-EXT	3.13V - 3.47V	M.2, Mezzanine board supply voltage
+1V8	1.71V - 1.89V	Audio, Octal Flash, MIPI, Mezzanine board supply voltage
+1V2	1.14V - 1.26V	MIPI supply voltage

Table 13: *Power rails*

7.9 ON / OFF

The system can be turned on an off after power has been applied to the CRX-IMX95. CRX-IMX95 and SoM will be controlled by means of the ONOFF button, which has several functions.

Here's a summary of the pin function:

- A brief connection to GND (while OFF) enables the CRX-IMX95 and SoM
- A long connection to GND (while ON) for $\geq$ 5s causes a forced off
- A short connection to GND (while ON) generates an interrupt

7.9.1 Power-up Sequence

Figure 10 represents the voltage start-up sequence of the CRX-IMX95 in the correct order, not depicting voltage ramps, voltage levels or exact timing between the slots. The power-up sequence finishes within ???ms.

Voltage with trailing "-MDL" are voltages that are generated on the SoM and used on the carrier board.

Startup Zeit anpassen nach Messung

stimmt die Spannungsreihenfolge im Bild?

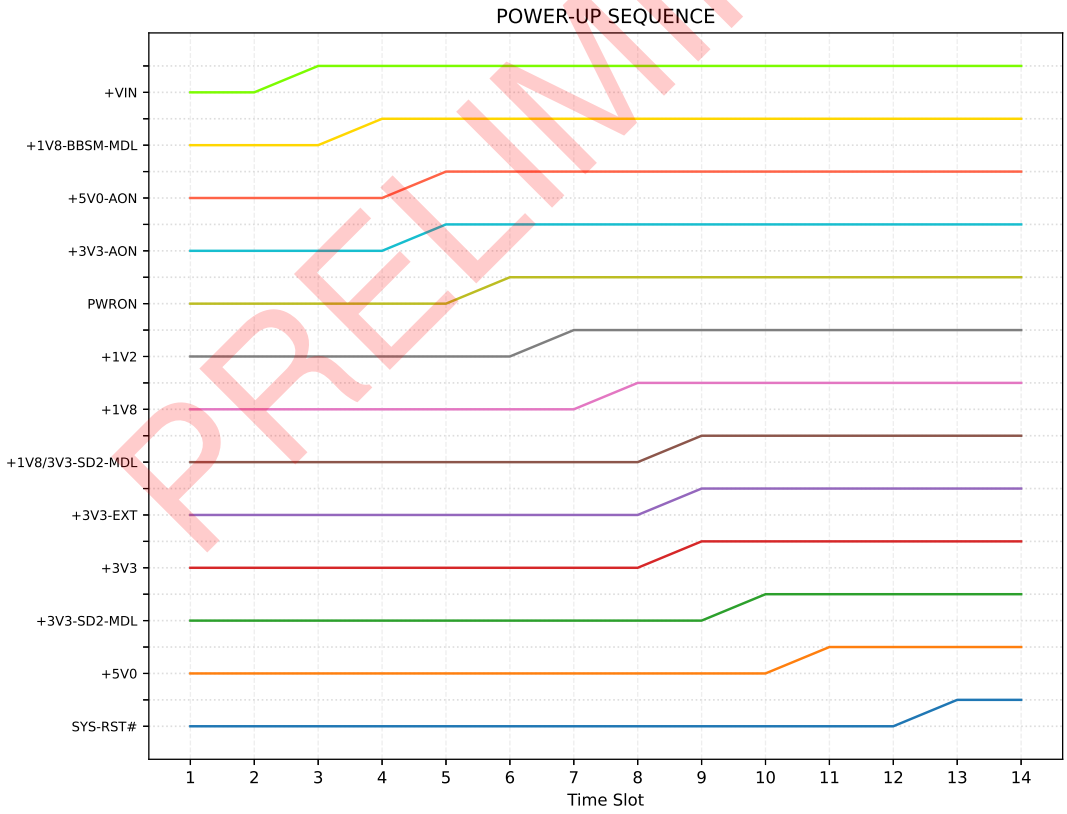


Figure 10: *Power-up sequence*

Reset is applied before any voltage is ramped. When the PMIC on the SoM is requested to start, several power supplies are ramped up in a fixed order. The CRX-IMX95 tracks these voltages and ramps up as shown in figure 10. After all rails are up, the reset is released.

7.9.2 Startup Sequence

First, power is supplied to both carrier board and SoM via Power Jack or USB-C. The system starts automatically. The ONOFF pin is only used after the board has initially started. During startup, the PMIC defines the reset pulse. When the reset event is finally cleared, the SoM is fully running.

Nevertheless, the SoM cannot be permanently held in reset. SYS-RST# is edge triggered and the PMIC creates a fixed reset pulse of $500\,\mathrm{ms}$. During this pulse, the power LEDs toggle off and on.

It is possible, that the reset states of carrier board and SoM differ after $500\,\mathrm{ms}$.

7.10 Reset

Figure 11 gives an overview of the reset structure on the CRX-IMX95. Most resets can be individually controlled by GPIO expanders (see chapter 7.17.9).

Flash reset (chapter 7.14) is controlled by GPIO from the SoM.

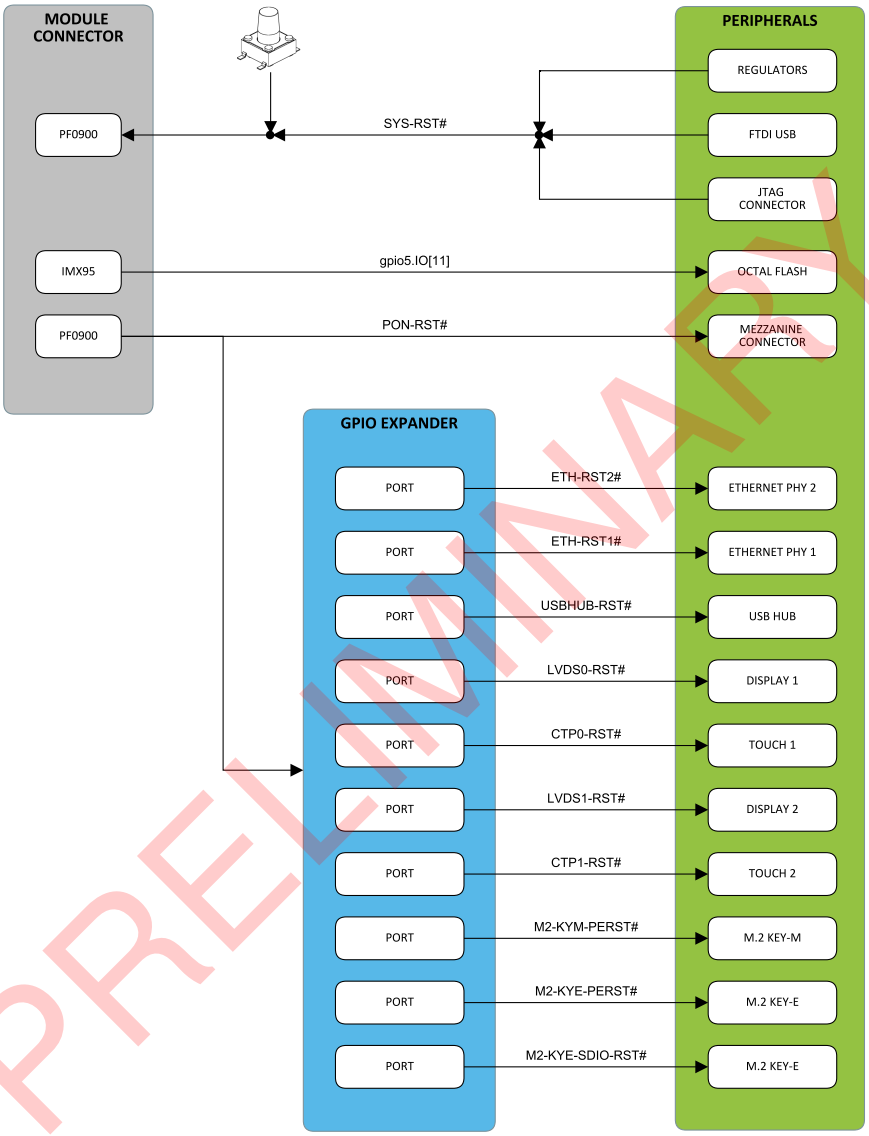


Figure 11: *Reset structure*

Reset	Direction	Description
SYS-RST#	Module Input	System reset created on CRX-IMX95. It controls the SoM both during power-up and asynchronously by Reset Button.
PON-RST#	Module Output	Power-on reset output from the SoM. When active, the SoM is in reset state. Used to control peripheral devices on the carrier board including GPIO expanders which return to default state. Maximum reset pulse is $500\,\mathrm{ms}$.

Table 14: *General resets*

7.11 JTAG

JTAG can be accessed either via MIPI-10 connector (see table 7).

The MIPI-10 pinout is depicted in table 15.

Pin	Signal	Description	Voltage Level
1	+1.8V	Reference Voltage	1.8V
2	TMS		1.8V
3	GND		
4	TCK		1.8V
5	GND		
6	TDO		1.8V
7	n.c. (KEY)		
8	TDI		1.8V
9	GND		
10	TRST#		1.8V

Table 15: *MIPI-10 JTAG connector pinout*

UART5 of the SoM can also be chosen as multiplexing option instead of JTAG on MIPI-10 connector. Please change pin definition in software accordingly.

See chapter 7.24 for details.

7.12 Miscellaneous

Table 16 lists the pinout of a $2.54\,\mathrm{mm}$ pitch pin header (ST9, table 7 and figure 5). By shorting pairs of adjacent pins, several functions can be tested. They can be found in the following sections.

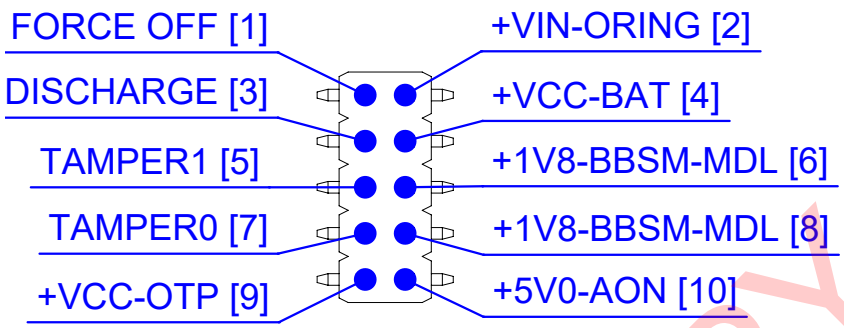


Figure 12: $2.54\,\mathrm{mm}$ *pin header*

Pin	Signal	Description	Signal	Pin
1	FORCE-OFF	1-2: disable all regulators	+VIN-ORING	2
3	RTC-DISCHARGE	3-4: discharge RTC supercap	+VCC-BAT	4
5	TAMPER1	5-6: simulate tamper detection	+1V8-BBSM-MDL	6
7	TAMPER0	7-8: simulate tamper detection	+1V8-BBSM-MDL	8
9	+VCC-OTP	9-10: power OTP voltage on SoM	+5V0-AON	10

Table 16: *Miscellaneous interfaces connector pinout*

7.12.1 Force Off

"Force Off" disables all power paths to the regulators by shorting pins 1 & 2.
If shorted, the ON/OFF button has no effect. The regulators will only restart, if the jumper is removed again.

7.12.2 Discharging RTC

The supercap powering the RTC on the SoM can be discharged by shorting pins 3 & 4.

Please remove power supplies connected to Power Jack and USB-C before discharging the supercap.

7.12.3 Tamper Detection

There are two tamper detection signals on ST9. Either pins 5 & 6 or 7 & 8 have to be shorted to simulate a detection.

7.12.4 OTP

For debugging the PMIC on the SoM there's another voltage required: +VCC-OTP. It can be provided by connecting pins 9 & 10 on ST9 (table 16). Users have to apply a voltage to a special pin in order to enter debug mode. For details refer to NXP's PF0900 datasheet.

Be careful when using this feature as you may create unwanted behaviour or inhibit the board from starting. Make sure to follow the proper sequence described in NXP's datasheet.

7.13 MicroSD Card

The CRX-IMX95 offers a microSD card slot with card detection. It is a push-push type.

The interface can also be configured as boot device (USDHC2 4-bit).

7.14 Octal Flash

There's an octal flash populated on the CRX-IMX95. Is uses XSPI1 and Slave Select SS0 with gpio5.IO[11] of the SoM as dedicated reset.

7.15 Power Supply

The CRX-IMX95 has two redundant power supply inputs:

- main supply is connected via Power Jack ST13
- alternate supply is via USB-C ST22, see also 7.16.1

When either voltage is present, power LED "Input Power" is illuminated green.

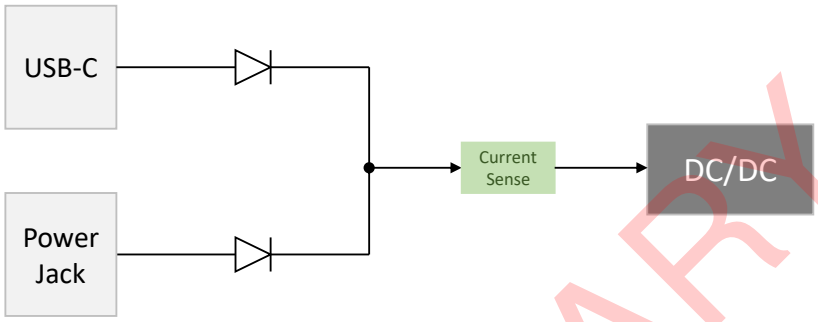


Figure 13: *Redundant power supply inputs*

7.15.1 Power Jack

Power Jack ST13 is considered the main supply with a wide nominal input voltage range from 9V to 24V. Overvoltage and undervoltage lockout limit the actual range to either ≈8.8V-25.3V (rising voltage) or ≈8.1V-25.3V (falling voltage).

7.15.2 Power via USB-C

USB-C on ST22 is another option to power the CRX-IMX95. Depending on the peripherals used, power consumption can be demanding. Therefore, the following settings are supported only:

USB-C Voltage	Supported?
9V	✗
12V	✗
15V	✗
20V	✓

Table 17: *Supported USB-C Power Delivery Sink capabilities*

Minimum accepted current is 2A. If the power supplied via USB-C is not sufficient, capability mismatch LED will be illuminated.

The CRX-IMX95 can also be evaluated with limited peripheral devices. In that case, it may be desirable to use a USB supply with reduced power. Via DIP switch (table 10) an 18W mode as minimum capability can be chosen. The accepted minimum current is also 2A.

USB-C Voltage	Supported?
9V	✓
12V	✓
15V	✓
20V	✓

Table 18: *Supported USB-C Power Delivery Sink capabilities in reduced mode*

7.15.3 RTC Backup

The RTC is powered in conjunction with the SoM or separately from optional RTC backup voltage (+VCC-BAT on ST1, pin B1).

For RTC backup, there's a supercap with $470\,\mathrm{mF}$ on the CRX-IMX95 that is charged as soon as power is supplied either via Power Jack or USB-C. It can also supply the RTC when both CRX-IMX95 and SoM are switched off. When fully charged ($\approx$ 4.4V), the RTC can be backed up for at least a month.

The supercap can be discharged. See chapter 7.12.2 for details.

7.15.4 Current Monitoring

As shown in figure 13, the input voltage path has a current sensor MAX9611AUB. It is accessible via I^2C7 (table 32).

The position of the $10\,\mathrm{m\Omega}$ sense resistor is marked in figure 5 if manual measurements are preferred.

7.15.5 Voltage Monitoring

SoM

The voltages of the SoM are provided on the module connector and monitored for overvoltage on the CRX-IMX95; undervoltage is **not** monitored. Overvoltage events trigger an alert, which is communicated to the SoM.

If activated by DIP switch (table 10), overvoltage events could alternatively switch off the power supply to the SoM.

Overvoltage limits are listed in table 19.

Voltage Rail	Overvoltage Range Limits
+1V8-MDL	2.08V ... 2.10V
+1V8-BBSM-MDL	2.08V ... 2.10V
+0V8-MDL	0.92V ... 0.93V
+3V3-MDL	3.90V ... 3.94V
+VCC-SOC-MDL	1.04V ... 1.05V
+VCC-ARM-MDL	1.04V ... 1.05V
+0V5-MDL	0.66V ... 0.67V
+1V05-MDL	1.24V ... 1.26V

Table 19: *Voltage monitoring limits for SoM's power rails*

Carrier Board

Carrier board voltages are monitored by the SoM's A/D converter channels 0-6.

Voltage Rail	ADC Channel	Voltage Divider Ratio
+5V0-AON	0	1 : 3.128
+5V0	1	1 : 3.128
+3V3-AON	2	1 : 2
+3V3-EXT	3	1 : 2
+3V3	4	1 : 2
+1V8	5	1 : 2
+1V2	6	1 : 1

Table 20: *Voltage monitoring on CRX-IMX95*

For example, voltages measured on channel 5 have to be multiplied by 2 to get the real values, whereas voltages on channel 6 correspond to real voltages.

7.16 USB

The carrier board CRX-IMX95 features three USB connectors and USB support for M.2 Key-E.

7.16.1 USB Type C (Power & Debug)

Power

ST22 (see table 7) is the alternative power supply input via USB-C connector. It requires a USB power source with 9V or 20V and minimum 2A current (see chapter 7.15.2). In case there's a mismatch regarding the minimum capability of the USB-C power source, the capability mismatch LED labeled "MIS" is illuminated. Depending on the peripherals used on the carrier board, 40W (or 18W, respectively) may not be sufficient and a more powerful supply unit must be used.

Debug

ST22 also carries the USB 2.0 debug port for quad UARTs. See chapter USB to UART for details.

7.16.2 USB to UART

Silicon Lab's CP2108 is the control unit on the CRX-IMX95. It has the following tasks:

1. convert USB to UART
2. remote control for
   - power on/off
   - system reset
   - boot selection

CP2108 converts one USB 2.0 port on USB-C connector (see connector in chapter 7.16.1) to quad UARTs. Three out of four ports are actually used.

UART Instance	Core Usage
UART1	Cortex A55
UART2	Cortex M33
UART3	Cortex M7

Table 21: *UART debug ports*

Enabling remote control also enables remote control for boot pins!

The following pins are used on channel 0:

Port	Direction	Function
TX0	Out (OD)	UART1-TXD
RX0	In	UART1-RXD
RTS0	—	—
CTS0	—	—
DTR0	—	—
DSR0	—	—
DCD0	—	—
RI0	—	—

Table 22: *CP2108 channel 0 pinout*

Channel 1:

Port	Direction	Function
TX1	Out (OD)	UART2-TXD
RX1	In	UART2-RXD
RTS1	—	—
CTS1	—	—
DTR1	—	—
DSR1	—	—
DCD1	—	—
RI1	—	—

Table 23: *CP2108 channel 1 pinout*

Channel 2:

Port	Direction	Function
TX2	Out (OD)	UART3-TXD
RX2	In	UART3-RXD
RTS2	—	—
CTS2	—	—
DTR2	—	—
DSR2	—	—
DCD2	—	—
RI2	—	—

Table 24: *CP2108 channel 2 pinout*

Channel 3:

Port	Direction	Function
TX3	—	—
RX3	—	—
RTS3	—	—
CTS3	—	—
DTR3	—	—
DSR3	—	—
DCD3	—	—
RI3	—	—

Table 25: *CP2108 channel 3 pinout*

CP2108 can set the boot pins by means of software.

1. configure boot mode to write mode
2. set boot mode pins according to the desired boot device
3. enable remote control
4. trigger a system reset

Those pins are controlled by CP2108's GPIOs according to table 26. "PP" stands for push-pull, whereas "OD" defines open-drain outputs.

Port	Direction	Function
GPIO0	—	—
GPIO1	—	—
GPIO2	—	—
GPIO3	—	—
GPIO4	—	—
GPIO5	—	—
GPIO6	—	—
GPIO7	—	—
GPIO8	Out (PP)	Boot Mode 0
GPIO9	Out (PP)	Boot Mode 1
GPIO10	Out (PP)	Boot Mode 2
GPIO11	Out (PP)	Boot Mode 3
GPIO12	Out (OD)	Read/ Write Boot mode pins: ■ High: write mode ■ Low: read mode (default)
GPIO13	Out (OD)	Remote control enable (low active)
GPIO14	Out (OD)	ON/OFF (high active)
GPIO15	Out (OD)	System reset (high active)

Table 26: *GPIO pinout*

7.16.3 USB Type A

The CRX-IMX95 features a stacked dual USB Type A connector (table 7 and figure 5). Both USB host ports support High Speed USB 2.0 mode with 500mA nominal current each. An overcurrent situation (≈650mA) is detected by the USB hub and the corresponding VBUS port power is turned off. In order to turn the port power on again, USB reset must be toggled via GPIO Expander (table 37).

7.16.4 USB Type C

The CRX-IMX95 also has an USB-C 3.0 Super Speed connector with 1.5A nominal current capability. This limit can be extended to 3A via DIP switch (see table 6). The port uses native USB lanes of the SoM and it can be controlled and monitored by GPIO Expander (see table 36) including fault, plugging and polarity information. Exceeding the chosen current limit or temperature limit of $135\,^{\circ}\mathrm{C}$ will trigger the USB1-FAULT# signal. It remains active until the fault condition is removed. Temperatures above $155\,^{\circ}\mathrm{C}$ will finally disable the USB-C controller on the CRX-IMX95. It will attempt to power-up again when die temperature decreases by 20℃.

Serial Download is available through this connector. It uses High Speed 2.0 signals of the USB-C connector only.

7.17 I²C

The CRX-IMX95 connects 7 out of 8 I²C ports. Port 7 is also used on the SoM, whereas I²C6 is not used at all. Please note that port 8 is 1.8V.

The following tables list all available devices. The maximum speed each chip is capable of is shown in the tables, but the minimum speed defines the speed of the I²C bus in the end.

7.17.1 Bus 1

Device	Part Number	A6	A5	A4	A3	A2	A1	A0	R/W	Addr (7bit)	Speed [kHz]	VCC
GPIO Expander	MCP23009	0	1	0	0	1	1	1	1/0	0x27	3400	3.3V
NXP's FuSa EEPROM	M24128-DRMF3TG/K	1	0	1	0	0	0	0	1/0	0x50	1000	3.3V

Table 27: *I²C1 address map*

7.17.2 Bus 2

Device	Part Number	A6	A5	A4	A3	A2	A1	A0	R/W	Addr (7bit)	Speed [kHz]	VCC
Audio Codec	WM8904	0	0	1	1	0	1	0	1/0	0x1A	400	3.3V
EEPROM (NFC)	ST25DV64KC	1	0	1	0	0	0	1	1/0	0x51	1000	3.3V
		1	0	1	0	0	1	1	1/0	0x53	1000	3.3V
		1	0	1	0	1	0	1	1/0	0x55	1000	3.3V
		1	0	1	0	1	1	1	1/0	0x57	1000	3.3V

Table 28: *I²C2 address map*

7.17.3 Bus 3

Device	Part Number	A6	A5	A4	A3	A2	A1	A0	R/W	Addr (7bit)	Speed [kHz]	VCC
MIPI-CSI Connector	Vision Components Power Chip	0	0	1	0	0	0	0	1/0	0x10	400	3.3V
MIPI-CSI Connector	Sony IMX415	0	0	1	1	0	1	0	1/0	0x1A	400	3.3V
Mezzanine Connector	t.b.d.	?	?	?	?	?	?	?	1/0	?	?	3.3V

Table 29: *I²C3 address map*

7.17.4 Bus 4

Device	Part Number	A6	A5	A4	A3	A2	A1	A0	R/W	Addr (7bit)	Speed [kHz]	VCC
LVDS0 Touch	FT5526EEZ	0	1	1	1	0	0	0	1/0	0x38	400	3.3V
LVDS0 EDID		1	0	1	0	0	0	0	1/0	0x50	?	3.3V

Table 30: *I²C4 address map*

7.17.5 Bus 5

Device	Part Number	A6	A5	A4	A3	A2	A1	A0	R/W	Addr (7bit)	Speed [kHz]	VCC
LVDS1 Touch	FT5526EEZ	0	1	1	1	0	0	0	1/0	0x38	400	3.3V
LVDS1 EDID		1	0	1	0	0	0	0	1/0	0x50	?	3.3V

Table 31: *I²C5 address map*

7.17.6 Bus 6

I²C Bus 6 is not available on CRX-IMX95. Those pins are used for other interfaces.

7.17.7 Bus 7

Device	Part Number	A6	A5	A4	A3	A2	A1	A0	R/W	Addr (7bit)	Speed [kHz]	VCC
USB Power Sink	TPS25730D	0	1	0	0	0	0	0	1/0	0x20	400	3.3V
GPIO Expander	MCP23009	0	1	0	0	0	1	0	1/0	0x22	3400	3.3V
Current Sensor	MAX9611AUB	1	1	1	0	0	0	0	1/0	0x70	400	3.3V
GPIO Expander	TCAL9539	1	1	1	0	1	0	0	1/0	0x74	1000	3.3V
GPIO Expander	TCAL9539	1	1	1	0	1	0	1	1/0	0x75	1000	3.3V
GPIO Expander	TCAL9539	1	1	1	0	1	1	0	1/0	0x76	1000	3.3V

Table 32: *I^2C7 address map*

7.17.8 Bus 8

Device	Part Number	A6	A5	A4	A3	A2	A1	A0	R/W	Addr (7bit)	Speed [kHz]	VCC
MIPI-CSI Connector	Vision Components Power Chip	0	0	1	0	0	0	0	1/0	0x10	400	3.3V
MIPI-CSI-MUX Connector	Sony IMX415	0	0	1	1	0	1	0	1/0	0x1A	400	3.3V
M.2 Connector Key E	???											1.8V
MIPI-to-DP Bridge	SN65DSI86ZXHR	0	1	0	1	1	0	1	1/0	0x2D	400	1.8V

Table 33: *I^2C8 address map*

7.17.9 GPIO Expander

Tables 27 and 32 list four GPIO expanders which control the main board functions like multiplexing, power enable and fault detection, resets, interrupts and board management.

I²C1

The GPIO Expander MCP23009 from Microchip on I²C1 bus is in the always-on domain. It provides an interrupt that is available on the module connector to notify the SoM of any changes.

Port	Direction	Signal	Active State	Pullup (SW configured)	Pulldown (SW configured)	OD / PP	Signal Description
GP0	Input	M2-KYE-PEWAKE#	Low	yes	—	—	PCIe PME wake from M.2 Key E socket
GP1	Input	M2-KYE-SDIO-WAKE#	Low	yes	—	—	SDIO sideband wake from M.2 Key E socket
GP2	Input	M2-KYE-UART-WAKE#	Low	—	—	—	UART sideband wake from M.2 Key E socket
GP3	Input	M2-KYE-PEWAKE#	Low	yes	—	—	PCIe PME wake from M.2 Key E socket
GP4	Output	CAN1-EN#	Low	—	—	OD	Enable signal for CAN transceiver (CAN1 / ST14)
GP5	Output	CAN1-STBY-EN	High	—	—	OD	Standby signal for CAN transceiver (CAN1 / ST14)
GP6	Input	ETH-WAKE#	Low	yes	—	—	Shared interrupt from both Ethernet PHYs
GP7	Input	BTN-WAKE#	Low	—	—	—	Interrupt from WAKE button to wake-up the whole system
INT#	Output	AON-IRQ#	Low	—	—	—	Interrupt output connected to Module Connector Pin T8

Table 34: *GPIO expander pin description (I²C1) on address 0x27*

I²C7

The CRX-IMX95 is furthermore controlled by three GPIO Expanders TCAL9539 from Texas Instruments and one MCP23009. They share one interrupt pin that is available on the module connector to notify the SoM of any changes.

Port	Direction	Signal	Active State	Pullup (SW configured)	Pulldown (SW configured)	OD / PP	Signal Description
GP0	Input	ETH1-IRQ#	Low	yes	—	—	Interrupt from Ethernet 1 PHY
GP1	Output	ETH1-RST#	Low	—	—	OD	Low active reset for Ethernet 1 PHY
GP2	Input	ETH2-RST#	Low	—	—	OD	Low active reset for Ethernet 2 PHY
GP3	Input	ETH2-IRQ#	Low	yes	—	—	Interrupt from Ethernet 2 PHY
GP4	Input	MEZZ-LAN-IRQ#	Low	yes	—	—	LAN interrupt from adapter on mezzanine board
GP5	—	GPX-0X22-P05	—	—	—	—	unused pin available on testpoint
GP6	—	GPX-0X22-P06	—	—	—	—	unused pin available on testpoint
GP7	Output	USBHUB-RST#	Low	—	—	OD	Dedicated reset for USB Hub. Reset pulse width >100µs
INT#	Output	GPX-IRQ#	Low	—	—	—	Interrupt output connected to Module Connector Pin B38

Table 35: *GPIO expander pin description (I²C7) on address 0x22*

Port	Direction	Signal	Active State	Pullup (SW configured)	Pulldown (SW configured)	OD / PP	Signal Description
P00	Output	M2-KYE-3V3-EN	High	—	—	OD	Enable 3.3V on M.2 Key E connector
P01	Input	M2-KYM-3V3-FLT#	Low	yes	—	—	Overcurrent flag for 3.3V on M.2 Key M connector
P02	Output	M2-KYM-PERST#	Low	—	—	OD	PCIe Reset (PERST#) to M.2 Key M connector
P03	Output	M2-KYE-SDIO-RST#	Low	—	—	OD	SDIO sideband GPIO pin to enable/disable (reset) the WiFi function on M.2 Key E connector
P04	Output	M2-KYE-PERST#	Low	—	—	OD	PCIe Reset (PERST#) to M.2 Key E connector
P05	Output	M2-KEYE-WDIS1#	Low	—	—	OD	Wireless disable signal 1 on M.2 Key E connector
P06	Output	M2-KYM-3V3-EN	High	—	—	OD	Enable 3.3V on M.2 Key M connector
P07	Input	M2-KYE-3V3-FLT#	Low	yes	—	—	Overcurrent flag for 3.3V on M.2 Key E connector
P10	Output	CAN3-EN	High	—	—	PP	Enable CAN-FD transceiver TJA1463 on CAN bus 3
P11	Output	CAN3-STBY-EN#	Low	—	—	PP	Control standby input of CAN-FD transceiver TJA1463 on CAN bus 3
P12	Output	CAN2-STBY-EN#	Low	—	—	PP	Control standby input of CAN-FD transceiver TJA1463 on CAN bus 2
P13	Output	CAN2-EN	High	—	—	PP	Enable CAN-FD transceiver TJA1463 on CAN bus 2
P14	Input	USB1-FAULT#	Low	yes	—	—	USB-C controller indicates current limit or thermal shutdown event due to over temperature
P15	Input	USB1-UFP#	Low	yes	—	—	Upstream facing port is identified on the CC via USB-C controller on USB1 port
P16	Input	USB1-POL#	Low	yes	—	—	Polarity signal from USB-C controller for USB type C implementation on USB1 port: – HIGH = standard polarity (CC line connected to CC1) – LOW = inverted polarity (CC line connected to CC2)
P17	Output	USB1-EN	High	—	—	PP	Enable USB-C 3.0 DFP controller TPS25810RVC
INT#	Output	GPX-IRQ#	Low	—	—	—	Shared interrupt output connected to Module Connector Pin B38

Table 36: *GPIO expander pin description (I^2C7) on address 0x74*

Port	Direction	Signal	Active State	Pullup (SW configured)	Pulldown (SW configured)	OD / PP	Signal Description
P00	Input	MIPI-CSI-MUX-OC#	Low	yes	—	—	Overcurrent flag for 3.3V on MIPI-CSI connector (multiplexed channel)
P01	Input	MIPI-CSI-MUX-FLASH	High	—	—	—	Flash signal from camera sensor on MIPI-CSI connector (multiplexed channel)
P02	Input	DP-IRQ#	Low	yes	—	—	Interrupt from DisplayPort Bridge SN65DSI86
P03	Output	DP-EN	High	—	—	OD	Enable DisplayPort Bridge SN65DSI86
P04	Input	DP-OC#	Low	yes	—	—	Overcurrent flag for 3.3V on DisplayPort connector
P05	Input	MIPI-CSI-CON-FLASH	High	—	—	—	Flash signal from camera sensor on MIPI-CSI connector
P06	Input	MIPI-CSI-OC#	Low	yes	—	—	Overcurrent flag for 3.3V on MIPI-CSI connector
P07	Output	DSI/CSI#	—	—	—	OD	Configure multiplexer: – HIGH = DSI selected – LOW = CSI selected
P10	Output	DP-PWR-EN	High	—	—	PP	Enable DisplayPort power on DP connector
P11	Output	MIPI-CSI-CON-TRG	High	—	—	PP	Trigger signal to camera sensor on MIPI-CSI connector
P12	Output	MIPI-CSI-PWR-EN	High	—	—	PP	Enable 3.3V on MIPI-CSI connector
P13	Output	MIPI-CSI-MUX-TRG	High	—	—	PP	Trigger signal to camera sensor on MIPI-CSI connector
P14	Output	DSI-CSI-MUX-EN	High	—	—	PP	Enable DSI/CSI multiplexer outputs
P15	Output	MIPI-CSI-MUX-PWR-EN	High	—	—	PP	Enable 3.3V on MIPI-CSI connector (multiplexed channel)
P16	Output	LVDS1-3V3-EN	High	—	—	PP	LVDS1: Enable power for Display and Touch Controller (=deactivate power gating)
P17	Output	LVDS0-3V3-EN	High	—	—	PP	LVDS0: Enable power for Display and Touch Controller (=deactivate power gating)
INT#	Output	GPX-IRQ#	Low	—	—	—	Shared interrupt output connected to Module Connector Pin B38

Table 37: *GPIO expander pin description (I^2C7) on address 0x75*

Port	Direction	Signal	Active State	Pullup (SW configured)	Pulldown (SW configured)	OD / PP	Signal Description
P00	Output	CTP0-RST#	Low	—	—	OD	Trigger reset for Touch Controller on LVDS0 channel
P01	Input	LVDS0-3V3-OC#	Low	yes	—	—	Overcurrent flag for 3.3V for LVDS0 channel
P02	Output	LVDS0-STBY#	Low	—	—	OD	Trigger standby signal on LVDS0 connector
P03	Output	LVDS0-RST#	Low	—	—	OD	Trigger reset on LVDS0 connector
P04	Input	LVDS0-12V0-FLT#	Low	yes	—	—	Overcurrent or undervoltage flag for 12V backlight for LVDS0 channel
P05	Output	LVDS0-LED-EN	High	—	—	OD	Enable Backlight on LVDS0 connector
P06	Output	LVDS0-12V0-EN	High	—	—	OD	LVDS0: Enable power for Backlight Driver (=deactivate power gating)
P07	Output	LVDS1-LED-EN	High	—	—	OD	Enable Backlight on LVDS1 connector
P10	Output	LVDS1-12V0-EN	High	—	—	OD	LVDS1: Enable power for Backlight Driver (=deactivate power gating)
P11	Output	LVDS1-STBY#	Low	—	—	OD	Trigger standby signal on LVDS1 connector
P12	Output	LVDS1-RST#	Low	—	—	OD	Trigger reset on LVDS1 connector
P13	Input	LVDS1-12V0-FLT#	Low	yes	—	—	Overcurrent or undervoltage flag for 12V backlight for LVDS1 channel
P14	—	unused	—	—	—	—	unused pin
P15	Input	LVDS1-3V3-OC#	Low	yes	—	—	Overcurrent flag for 3.3V for LVDS1 channel
P16	Output	CTP1-RST#	Low	—	—	OD	Trigger reset for Touch Controller on LVDS1 channel
P17	—	GPX-0X76-P17	—	—	—	—	unused pin available on testpoint
INT#	Output	GPX-IRQ#	Low	—	—	OD	Shared interrupt output connected to Module Connector Pin B38

Table 38: *GPIO expander pin description (I^2C7) on address 0x76*

7.17.10 EEPROM with NFC

There's an onboard EEPROM which can be accessed via I^2C (see table 28) and NFC. It contains board information like serial number and both board revision and version.

The location of the passive NFC antenna can be found in figure 5.

7.18 Ethernet

The CRX-IMX95 offers two Gigabit Ethernet ports and one 10 Gigabit Ethernet port.

- the 1 Gigabit ports are available on two separate RJ45 connectors.
- the 10 Gigabit port is available on the mezzanine connector.

The RJ45 connectors have two LEDs:

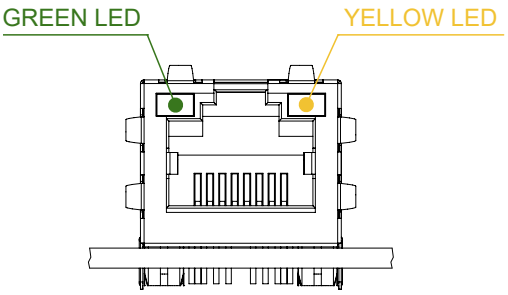


Figure 14: *Ethernet LEDs*

LED	Function
Green (PHY LED1)	1000 Mbps Link & Activity
Yellow (PHY LED2)	100 Mbps Link & Activity

Table 39: *Ethernet LEDs*

7.18.1 Gigabit Ethernet

Both Gigabit RGMII PHYs share MDIO1 bus. See table 40 for PHY addresses:

Port	PHY Address	Connector
RGMII 1	0x01	ST28
RGMII 2	0x02	ST29

Table 40: *PHY addresses on MDIO1 bus*

Both Gigabit ports support Wake-on-LAN, which is the default setting in software.

7.18.2 10 Gigabit Ethernet

10 Gigabit Ethernet can only be used on the CRX-IMX95 by means of additional boards plugged into the mezzanine connector. See chapter Mezzanine Connector for details.

PHYs on the mezzanine board use MDIO1 bus, too. Please check for address conflicts when designing custom adapter boards.

7.19 LVDS Displays

There are two LVDS displays supported on the CRX-IMX95. The connectors are located on top and bottom side of the board (see figure 4 and figure 5).

Each display has the following features which can mostly be controlled by GPIO expander (see tables 36 and 38)

- separate I²C ports
- I²C touch
- separate power gating for 12V and 3.3V supplies
- overcurrent control for 12V and 3.3V supplies
- PWM support for backlight control
- configurable reset and standby modes for the display

The carrier board CRX-IMX95 has been designed to support Newhaven NHD-10.1-1024600BF-LSXP-CTP displays.

The Newhaven NHD-10.1-1024600BF-LSXP-CTP features:

- 10.1" Diagonal
- 1024 x 600 Pixel RGB
- LVDS Interface
- LED Backlight
- I²C Capacitive Touch

Basically, displays can be adapted that fit the pinout and power limits for each power rail.

Port	Connector	Power Rail	Maximum Current
LVDS0	ST5	+12V	≈1200mA
LVDS0	ST5 & ST6	+3.3V	≈500mA
LVDS1	ST20	+12V	≈1200mA
LVDS1	ST20 & ST21	+3.3V	≈500mA

Table 41: *LVDS display power limits*

LVDS displays including touch interface do not support hot plugging! Disconnect power supply before wiring.

7.19.1 LVDS 0

The LVDS connector (see table 7) has 40 pins and the pinout is listed in table 42.

Pin	Signal	Description
1	GND	
2	+3.3V	■ enable: LVDS0-3V3-EN ■ overcurrent: LVDS0-3V3-OC# ■ LED: LD4
3	+3.3V	
4	+3.3V	
5	GND	
6	SCL	I2C4
7	SDA	
8	LVDS-CH0-	
9	LVDS-CH0+	
10	GND	
11	LVDS-CH1-	
12	LVDS-CH1+	
13	GND	
14	LVDS-CH2-	
15	LVDS-CH2+	
16	GND	
17	LVDS-CLKIN-	
18	LVDS-CLKIN+	
19	GND	
20	LVDS-CH3-	
21	LVDS-CH3+	
22	GND	
23	INSEL	strap: 8 bit
24	GND	
25	GND	
26	UPDN	strap: normal scan
27	SHLR	strap: normal scan
28	GND	

29	RESET#	reset: LVDS0-RST#
30	STBY#	standby: LVDS0-STBY
31	GND	
32	GND	
33	GND	
34	GND	
35	LED-PWM	tpm5.CH2 (gpio2.IO[18])
36	LED-EN	enable: LVDS0-LED-EN
37	LED-BIST	strap: normal scan
38	+12V	■ enable: LVDS0-12V0-EN ■ overcurrent: LVDS0-12V0-FLT# ■ LED: none
39	+12V	
40	+12V	

Table 42: *LVDS0 display connector pinout*

There's a separate connector for the capacitive touch interface (table 7). The pinout can be found in table 43.

Pin	Signal	Description
1	+3.3V	■ enable: LVDS0-3V3-EN ■ overcurrent: LVDS0-3V3-OC# ■ LED: LD4
2	GND	
3	I2C-SCL	I2C4
4	I2C-SDA	
5	IRQ#	interrupt: CTP0-RST#
6	RESET#	reset: CTP0-RST#

Table 43: *LVDS0 touch connector pinout*

7.19.2 LVDS 1

The LVDS connector (see table 7) has 40 pins and the pinout is listed in table 44.

Pin	Signal	Description
1	GND	
2	+3.3V	■ enable: LVDS1-3V3-EN ■ overcurrent: LVDS1-3V3-OC# ■ LED: LD12
3	+3.3V	
4	+3.3V	
5	GND	
6	SCL	I2C5
7	SDA	
8	LVDS-CH0-	
9	LVDS-CH0+	
10	GND	
11	LVDS-CH1-	
12	LVDS-CH1+	
13	GND	
14	LVDS-CH2-	
15	LVDS-CH2+	
16	GND	
17	LVDS-CLKIN-	
18	LVDS-CLKIN+	
19	GND	
20	LVDS-CH3-	
21	LVDS-CH3+	
22	GND	
23	INSEL	strap: 8 bit
24	GND	
25	GND	
26	UPDN	strap: normal scan
27	SHLR	strap: normal scan
28	GND	

29	RESET#	reset: LVDS1-RST#
30	STBY#	standby: LVDS1-STBY
31	GND	
32	GND	
33	GND	
34	GND	
35	LED-PWM	tpm6.CH2 (gpio2.IO[19])
36	LED-EN	enable: LVDS1-LED-EN
37	LED-BIST	strap: normal scan
38	+12V	■ enable: LVDS1-12V0-EN ■ overcurrent: LVDS1-12V0-FLT# ■ LED: none
39	+12V	
40	+12V	

Table 44: *LVDS1 display connector pinout*

There's a separate connector for the capacitive touch interface (table 7). The pinout can be found in table 45.

Pin	Signal	Description
1	+3.3V	■ enable: LVDS1-3V3-EN ■ overcurrent: LVDS1-3V3-OC# ■ LED: LD12
2	GND	
3	I2C-SCL	I2C5
4	I2C-SDA	
5	IRQ#	interrupt: CTP1-RST#
6	RESET#	reset: CTP1-RST#

Table 45: *LVDS1 touch connector pinout*

7.20 MIPI-CSI / -DSI

The SoM provides two MIPI interfaces. On the one hand, there's a MIPI-CSI interface for external cameras. On the other hand, there's a multiplexed MIPI-CSI or MIPI-DSI interface for either cameras or display. Consequently, there are two configuration options:

- 2x MIPI-CSI
- 1x MIPI-CSI + 1x MIPI-DSI (DisplayPort)

MIPI-DSI is converted to DisplayPort on CRX-IMX95.

As the signals are routed to different connectors, there's a multiplexer which has to be configured correctly to use the desired configuration. It is described in the following chapters.

7.20.1 MIPI-CSI (native)

MIPI-CSI can be used on a 22-pin connector listed in table 7, which provides four data lanes. The pinout is common for many camera modules, which can consume 500mA nominal current. An over-current situation (≈650mA) can be monitored via GPIO expander. When power is switched on, LED "+3V3 MIPI CSI" is illuminated (figure 8).

Pin	Signal	Description
1	GND	
2	D0-	data pair 0
3	D0+	
4	GND	
5	D1-	data pair 1
6	D1+	
7	GND	
8	CLK-	clock pair
9	CLK+	
10	GND	
11	D2-	data pair 2
12	D2+	

13	GND	
14	D3-	data pair 3
15	D3+	
16	GND	
17	TRG	trigger to sensor
18	FLASH	flash from sensor
19	GND	
20	SCL	I2C3
21	SDA	
22	+3.3V	supply voltage

Table 46: *MIPI-CSI connector pinout*

The connector has the "inverse" pinout and a "top contact" FPC connector. Please make sure to use the correct FFC cable (see chapter 3)!

MIPI cameras do not support hot plugging! Disconnect power supply before wiring.

7.20.2 MIPI-CSI (multiplexed)

As mentioned in chapter 7.20 the second MIPI-CSI interface and MIPI-DSI are mutually exclusive. In order to use the multiplexed MIPI-CSI port, the driver handles the following steps (in that order):

1. configure the GPIO expander for MIPI-CSI (see table 32)
2. enable the multiplexer via GPIO expander
3. enable MIPI-CSI power for the multiplexed channel via GPIO expander (LED is illuminated)

MIPI-CSI can be used on a 22-pin connector listed in table 7 which provides four data lanes. The pinout is common for many camera modules, which can consume 500mA nominal current. An overcurrent situation (≈650mA) can be monitored via GPIO expander. When power is switched on, LED "+3V3 MIPI CSI (MUXED)" is illuminated (figure 8).

Pin	Signal	Description
1	GND	
2	D0-	data pair 0
3	D0+	
4	GND	
5	D1-	data pair 1
6	D1+	
7	GND	
8	CLK-	clock pair
9	CLK+	
10	GND	
11	D2-	data pair 2
12	D2+	
13	GND	
14	D3-	data pair 3
15	D3+	
16	GND	
17	TRG	trigger to sensor
18	FLASH	flash from sensor

19	GND	
20	SCL	I2C8
21	SDA	
22	+3.3V	supply voltage

Table 47: *MIPI-CSI connector pinout (multiplexed)*

The connector has the "inverse" pinout and a "top contact" FPC connector. Please make sure to use the correct FFC cable (see chapter 3)!

LVDS displays do not support hot plugging! Disconnect power supply before wiring.

7.20.3 MIPI-DSI / DisplayPort

MIPI-DSI is not available as native interface on the CRX-IMX95. It is converted to DisplayPort instead. More information can be found in chapter DisplayPort.

7.21 DisplayPort

DisplayPort is derived from MIPI-DSI interface. Therefore, the second MIPI-CSI interface and DisplayPort are mutually exclusive.

The following steps (in that order) are required to use DisplayPort. This is handled by the driver.

1. configure the GPIO expander for MIPI-DSI (see table 32)
2. enable the multiplexer via GPIO expander
3. enable DisplayPort power via GPIO expander (LED is illuminated)
4. enable DisplayPort bridge via GPIO expander

DisplayPort power is limited to 500mA nominal current. An overcurrent situation (≈650mA) can be monitored via GPIO Expander. Both bridge and interface do not have a dedicated hardware reset, the bridge is reset by the enable pin.

The DisplayPort interface supports hot plugging.

7.22 Audio

The audio section of the CRX-IMX95 comprises stereo microphone input, line output and headphone output with microphone on two connectors (figure 5). The audio Codec WM8904CGE can be accessed by I^2C bus (table 28) and exchanges data via I^2S bus 3. It has no dedicated reset pin.

WM8904CGE	Signal	Direction
MCLK	SAI3-MCLK (ST1: B30)	Codec Input
BCLK	SAI3-TXC (ST1: B29)	Codec Input (Slave mode) / Output (Master mode)
LRCLK	SAI3-TXFS (ST1: B40)	Codec Input (Slave mode) / Output (Master mode)
DACDAT	SAI3-TXD (ST1: B35)	Codec Input
ADCDAT	SAI3-RXD (ST1: B34)	Codec Output

Table 48: *Audio Codec signal description*

7.22.1 Headphone with Microphone

ST8 is an audio jack with four electrical contacts (TRRS / CTIA standard). See figure 15.

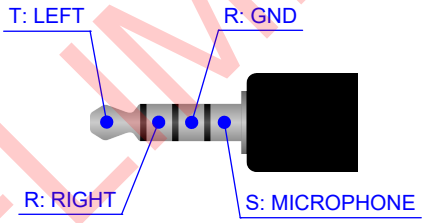


Figure 15: *Headphone connector pinout*

7.22.2 Line-Out

ST7 is an audio jack with three electrical contacts (TRS / CTIA standard). See figure 16.

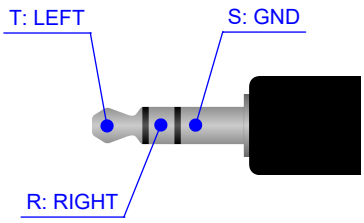


Figure 16: *Line-Out connector pinout*

7.22.3 Microphones

There are two MEMS microphones on the CRX-IMX95 for left and right channel. They use DMICDAT1 channel for data and GPIO1 for DMIC clock output.

7.23 A/D Converter

The SoM provides 8 A/D converter channels (channels 0-7) with 1.8V maximum amplitude. They are used for monitoring the CRX-IMX95's voltages and can not be used for user purposes. See chapter Voltage Monitoring for more information.

The eigth channel (channel 7) is used for hardware identification of the CRX-IMX95 according to table 49.

Hardware Revision	Voltage Range
Revision 1	$U \leq 0.05V$
Revision 2	$0.17V < U < 0.22V$
Revision 3	$0.34V < U < 0.39V$
Revision 4	$0.51V < U < 0.56V$
Revision 5	$0.68V < U < 0.73V$
Revision 6	$0.85V < U < 0.90V$
Revision 7	$1.02V < U < 1.07V$
Revision 8	$1.19V < U < 1.24V$
Revision 9	$1.36V < U < 1.41V$
Revision 10	$1.53V < U < 1.58V$
Revision 11	$1.70V < U < 1.75V$

Table 49: *Hardware revision overview*

7.24 UART

The CRX-IMX95 has three UART ports which are described in the USB section of the document (table 21).

They are used for console outputs of the different cores of the CPU and converted to USB.

7.25 CAN

The CRX-IMX95 has three CAN-FD ports using TJA1463ATK as transceiver. All ports support Wake-on-CAN.

The CAN signals are available on three DSUB9 connectors with identical pinout.

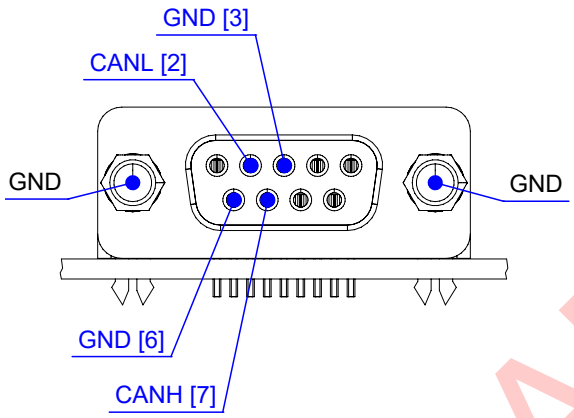


Figure 17: *DSUB-9 CAN pinout*

NOTE

The connector pinout is in accordance with CiA® 106. Optional $120\,\Omega$ (split) termination can be added individually for each port by means of slide switches (see figures 4 and 18).

Pin	Signal	Description
1	—	
2	CANL	CAN LOW signal
3	GND	
4	—	
5	—	
6	GND	
7	CANH	CAN HIGH signal
8	—	
9	—	

Table 50: *DSUB-9 CAN connector pinout*

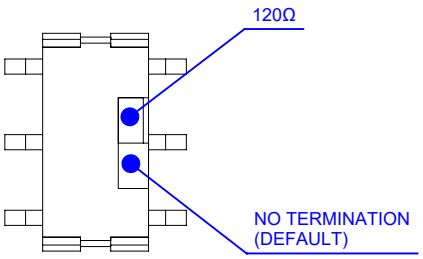


Figure 18: *CAN termination switch*

NXP's TJA1463ATK transceivers support various modes. Starting from power-off, when the CRX-IMX95 is not externally supplied, the transceiver enters *standby* mode as soon as the carrier board is supplied. In order to transition to *normal* mode, *listen-only* or *sleep* mode, control signals are provided via GPIO Expanders (see tables 34 and 36)

Signal	TJA1463ATK Pin
CAN-EN	Pin 6
CAN-STBY-EN#	Pin 14

Table 51: *CAN transceiver control signals*

Those signals can be controlled individually for all three transceivers. On top of that, CANx-WAKE and CANx-ERR# signals are available on testpoints (see table 12).

CAN1 is controlled by M33 core, whereas CAN2 and CAN3 are accessible for A55 cores.

7.26 M.2

There are two M.2 sockets on the CRX-IMX95:

- M.2 socket Key-M
- M.2 socket Key-E

Power for each port must be enabled via GPIO Expander (see table 36). It is limited to $1.9\,\mathrm{A}$ nominal current per port, whereas an overcurrent situation ($\approx 2.05\,\mathrm{A}$) can be also monitored via GPIO Expander.

M.2 slots do not support hot plugging! Disconnect power supply before wiring.

7.26.1 Key-M

Key-M - usually intended for memory extension - offers one PCIe lane with $100\,\mathrm{MHz}$ clock provided by the SoM after a successful request. The card can be reset via GPIO Expander (table 36).

For M.2 cards that support wakeup function, PEWAKE# can also be queried by GPIO Expander (see table 34).

Key-M socket supports M.2 modules with width of $22\,\mathrm{mm}$ and length up to $80\,\mathrm{mm}$

Table 52 lists all available signals on the M.2 socket.

Pin	Signal	Supported?	Supported?	Signal	Pin
1	GND	✓	✓	+3.3V	2
3	GND	✓	✓	+3.3V	4
5	PER3-	✗	✓	n.c.	6
7	PER3+	✗	✓	n.c.	8
9	GND	✓	✗	DAS/DSS#	10
11	PET3-	✗	✓	+3.3V	12
13	PET3+	✗	✓	+3.3V	14
15	GND	✓	✓	+3.3V	16

17	PER2-	✗	✓	+3.3V	18
19	PER2+	✗	✓	n.c.	20
21	GND	✓	✓	n.c.	22
23	PET2-	✗	✓	n.c.	24
25	PET2+	✗	✓	n.c.	26
27	GND	✓	✓	n.c.	28
29	PER1-	✗	✓	n.c.	30
31	PER1+	✗	✓	n.c.	32
33	GND	✓	✓	n.c.	34
35	PET1-	✗	✓	n.c.	36
37	PET1+	✗	✗	DEVSLP	38
39	GND	✓	✓	n.c.	40
41	SATA-B+/PER0-	✓(PCIe)	✓	n.c.	42
43	SATA-B-/PER0+	✓(PCIe)	✓	n.c.	44
45	GND	✓	✓	n.c.	46
47	SATA-A-/PET0-	✓(PCIe)	✓	n.c.	48
49	SATA-A+/PET0+	✓(PCIe)	✓	PERST#	50
51	GND	✓	✓	CLKREQ#	52
53	REFCLK-	✓	✓	PEWAKE#	54
55	REFCLK+	✓	✓	n.c.	56
57	GND	✓	✓	n.c.	58
KEY M					
67	n.c.	✓	✗	SUSCLK	68
69	PEDET	✓	✓	+3.3V	70
71	GND	✓	✓	+3.3V	72
73	GND	✓	✓	+3.3V	74
75	GND	✓			

Table 52: *M.2 Key-M Pinout*

7.26.2 Key-E

Key-E - usually intended for extension cards, e.g. WiFi cards - offers one PCIe lane with 100 MHz clock provided by the SoM after a successful request. The card can be reset via GPIO Expander (table 36).

For M.2 cards that support wakeup function, PEWAKE# can also be queried by GPIO Expander (see table 34).

The following features are supported:

- USB 2.0 port (USB-HUB: port 3) without control signals (not supported by M.2 standard)
- 4-bit SDIO interface with wakeup and reset (via GPIO Expander)
- UART interface with handshake signals and wakeup signal (via GPIO Expander)
- I^2C (bus 8)
- 2 status indicator LEDs
- PCM interface
- W_DISABLE1# to disable wireless communications add-in cards
- SUSCLK provided by SoM (CCM_CLKO4 / gpio4.IO[29] on connector ST1, pin T64)

Key-E socket supports M.2 modules with width of 22 mm and length up to 80 mm

Table 53 lists all available signals on the M.2 socket.

Pin	Signal	Supported?	Supported?	Signal	Pin
1	GND	✓	✓	+3.3V	2
3	USB-D+	✓	✓	+3.3V	4
5	USB-D-	✓	✓	LED1#	6
7	GND	✓	✓	PCM-CLK/I2S-SCK	8
9	SDIO-CLK	✓	✓	PCM-SYNC/I2S-WS	10
11	SDIO-CMD	✓	✓	PCM-IN/I2S-SD-IN	12
13	SDIO-DATA0	✓	✓	PCM-OUT/I2S-SD-OUT	14
15	SDIO-DATA1	✓	✓	LED2#	16
17	SDIO-DATA2	✓	✓	GND	18
19	SDIO-DATA3	✓	✓	UART-WAKE#	20

21	SDIO-WAKE	✓	✓	UART-RXD	22
23	SDIO-RESET#	✓			
KEY E					
			✓	UART-TXD	32
33	GND	✓	✓	UART-CTS	34
35	PET0+	✓	✓	UART-RTS	36
37	PET0-	✓	✗	VENDOR DEFINED	38
39	GND	✓	✗	VENDOR DEFINED	40
41	PER0+	✓	✗	VENDOR DEFINED	42
43	PER0-	✓	✗	COEX3	44
45	GND	✓	✗	COEX2	46
47	REFCLK+	✓	✗	COEX1	48
49	REFCLK-	✓	✓	SUSCLK	50
51	GND	✓	✓	PERST0#	52
53	CLKREQ0#	✓	✗	W-DISABLE2#	54
55	PEWAKE0#	✓	✓	W-DISABLE1#	56
57	GND	✓	✓	I2C-DATA	58
59	PET1+	✗	✓	I2C-CLK	60
61	PET1-	✗	✗	ALERT#	62
63	GND	✓	✗	RESERVED	64
65	PER1+	✗	✗	UIM-SWP/PERST1#	66
67	PER1-	✗	✗	UIM-POWER-SNK/CLKREQ1#	68
69	GND	✓	✗	UIM-POWER-SRC/GPIO1/PEWAKE1#	70
71	REFCLK1+	✗	✓	+3.3V	72
73	REFCLK1-	✗	✓	+3.3V	74
75	GND	✓			

Table 53: *M.2 Key-E Pinout*

7.27 Mezzanine Connector

The mezzanine connector (order code can be found in table 7) with 50 pins allows for additional adapter boards to be used with the CRX-IMX95. MicroSys provides several adapters, for example with SJA1110 providing 6x Ethernet T1. Those adapters can be used on several carrier boards across different SoM families. Therefore, some pins of the adapter(s) may not be supported on the CRX-IMX95 carrier board.

The pinout of the mezzanine connector on the CRX-IMX95 is as follows:

Pin	Signal	Signal Source	Level	Level	Signal Source	Signal	Pin
1	+1.8V					+1.8V	2
3	+1.8V					+1.8V	4
5	GND					GND	6
7	GND			+1.8V	ST1: Pin B120	RESET#	8
9	SPI-MISO	ST1: B50 / CPU: gpio5.IO[15]	+3.3V	+1.8V	GPIO Expander	LAN-IRQ#	10
11	SPI-MOSI	ST1: B51 / CPU: gpio5.IO[16]	+3.3V	+3.3V	ST1: Pin B13	I2C-SCL	12
13	SPI-SCK	ST1: B52 / CPU: gpio5.IO[17]	+3.3V	+3.3V	ST1: Pin B12	I2C-SDA	14
15	GND					GND	16
17	SPI-CS0#	ST1: B49 / CPU: gpio5.IO[14]	+3.3V		ST1: Pin T70	SRD-A-TX-	18
19	SPI-CS1#	ST1: B48 / CPU: gpio5.IO[13]	+3.3V		ST1: Pin T69	SRD-A-TX+	20
21	GND					GND	22
23	—				ST1: Pin T73	SRD-A-RX-	24
25	—				ST1: Pin T72	SRD-A-RX+	26
27	GND					GND	28
29	—			+1.8V	ST1: Pin T53	MDC	30
31	—			+1.8V	ST1: Pin T54	MDIO	32
33	GND					GND	34
35	USB-D-	USB-HUB: PORT 4				—	36
37	USB-D+	USB-HUB: PORT 4				—	38
39	GND					GND	40
41	—		+1.8V			—	42

43	GND					—	44
45	GND					GND	46
47	+3.3V					+3.3V	48
49	+3.3V					+3.3V	50

Table 54: *Mezzanine connector pinout*

The power rails are not fused, thus make sure that the CRX-IMX95 is not overloaded. Maximum power which can be provided is:

Power Rail	Maximum Power per Rail
+1.8V	1A
+3.3V	1.5A

Table 55: *Maximum power on mezzanine connector*

All adapters have one size, which is $150 \times 55\,\mathrm{mm}$:

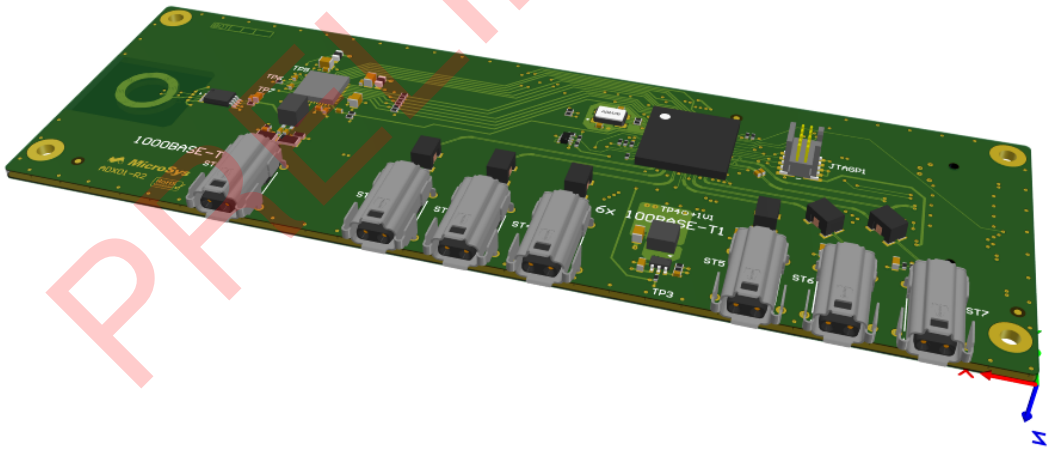


Figure 19: *Adapter ADX01*

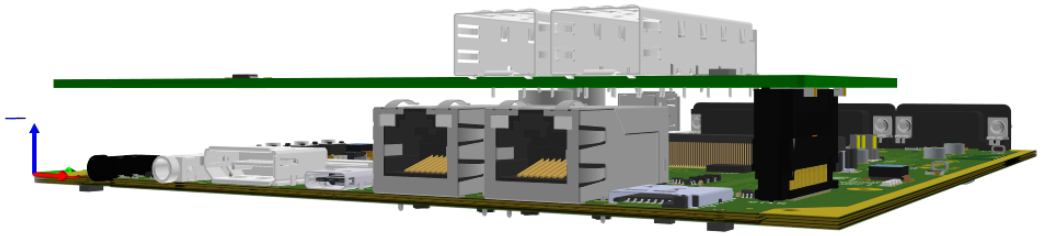


Figure 20: *Adapter board and carrier board (spacers are not shown)*

Adapter boards do not support hot plugging! Disconnect power supply before connecting an additional adapter.

8 Mechanical Description

8.1 Mounting / Unmounting

The mounting or unmounting of the module should only be made in a static free area with full ESD precautions, i.e. as a minimum, a grounded dissipative work surface of sufficient size and a grounded skin contact wrist strap are necessary. Make sure that all parts, the carrier board, the module and the heatsink are placed on the same static free area to avoid any discharges between them during assembly. To mount the SoM, make sure that the CRX-IMX95 is disconnected from any power or other IO interfaces. Both connector surfaces of the module must be clean and as the carrier board connector should be checked for bent or dirty contacts. Check the module and the carrier board for foreign or loose parts, which do not belong to the boards. The screws should have clean threads and should be tightened with a maximum torque of 30Ncm.

Insert or remove the SoM at an angle of about 25° as shown in figure 21.

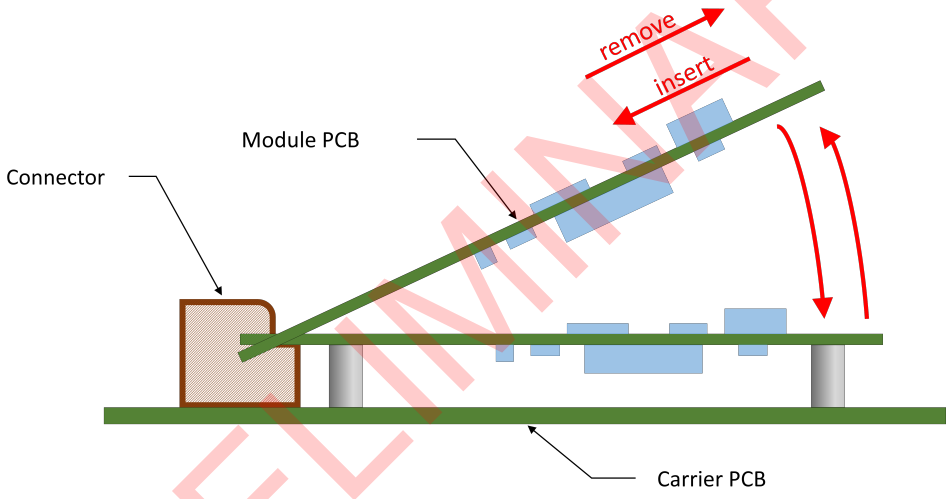


Figure 21: *Module mounting*

The thermal conduction between heatsink and SoC is achieved using a thermal pad. Make sure that this thermal pad has the correct thickness and is placed over the SoC package before mounting the heatsink.

For the removal of the module, first unplug all connections to the system. Remove the inner screws, then the outer ones. The thermal pad may cause the heatsink to stick to the module, so take care when pulling them apart to avoid damaging any part of the module. Lift the module to about 25° and remove it from the connector. Store the parts on a static free area.

8.2 Board Dimensions

The following figure 22 shows the mechanical outline of the CRX-IMX95. The mounting holes require M2.5 screws.

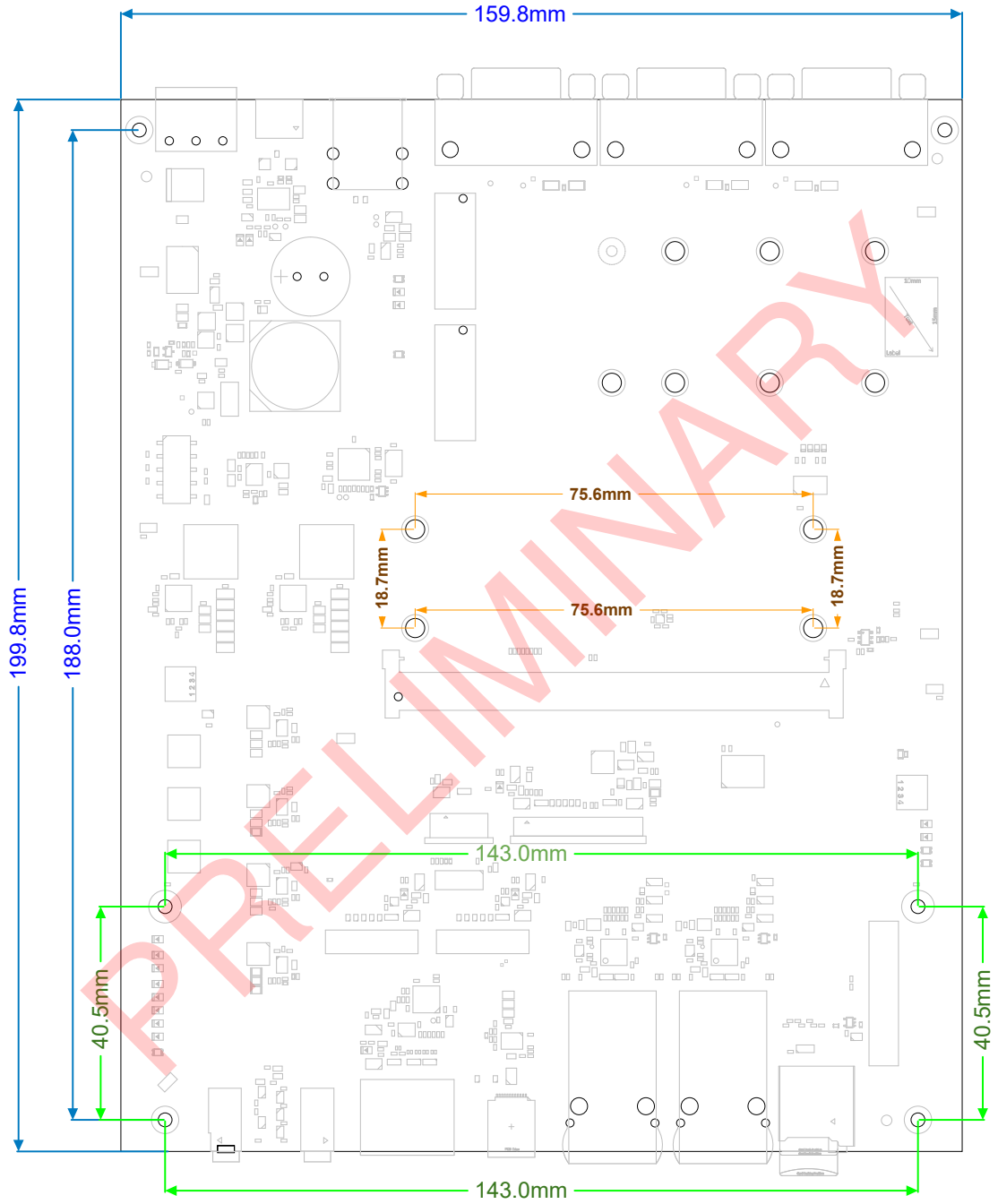


Figure 22: *Board dimensions*

NOTE

For 3D data files please contact MicroSys.

8.3 Thickness

The PCB thickness of the CRX-IMX95 carrier board is 1.69mm ± 10%.

8.4 Height

Board height is shown in figure 23. The values given are without SoM, adapters, cooling solutions and extension cards. The supercap for RTC buffering stands out on top side, whereas an inductor is the highest point on bottom side.

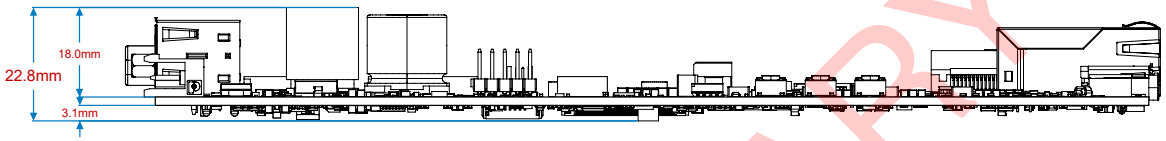


Figure 23: *Board height*

8.5 Weight

The weight is $approx 240\,\mathrm{g}$.

Gewicht fehlt

8.6 Housing

The CRX-IMX95 has been designed to fit in a Fischer housing. It can be found on the Fischer website with the model number AKG 165 46 200.

9 Software

9.1 U-Boot

The CRX-IMX95 uses U-Boot as the standard bootloader. The current version of U-Boot is pre-programmed in the board's eMMC memory.

Additionally, there is a U-Boot version available for SD card if that interface is implemented on the carrier. The standard MicroSys carrier board (CRX-IMX95) has a SD card interface.

Basically, the bootloader carries out the following tasks:

- Pin configuration
- SoC configuration
- Clock configuration
- LPDDR5 configuration and timing

9.2 Operating System

MicroSys Electronics GmbH offers Linux support for the module. Please refer to the MicroSys Software Enablement Guide for more details.

Other Operating Systems are available on request only.

List of Figures

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List of Acronyms

ADC Analogue digital converter. 46

CAN Controller Area Network. 75

Codec *Cod*er / *Dec*oder. 73

FFC Flat Flexible Cable. 69, 71

FPC Flexible Printed Circuits. 69, 71

GPIO General Purpose Input Output. 55, 56

JTAG Joint Test Action Group. 41

MIPI-CSI Mobile Industry Processor Interface Alliance Camera Serial Interface. 68

MIPI-DSI Mobile Industry Processor Interface Alliance Display Serial Interface. 68, 71

PCB Printed Circuit Board. 19

PCIe PCI Express. 77, 80

PCM Pulse Code Modulation. 80

PMIC Power-Management Integrated Circuit. 43

PWM Pulse Width Modulation. 62

RTC Real-time clock. 45

TRRS Audio connector with **T**ip **R**ing **R**ing **S**leeve contacts. 73

TRS Audio connector with **T**ip **R**ing **S**leeve contacts. 73

UART Universal Asynchronous Receiver / Transmitter. 74

USB-C Universal Serial Bus Type C. 47

WiFi Wireless Fidelity. 80