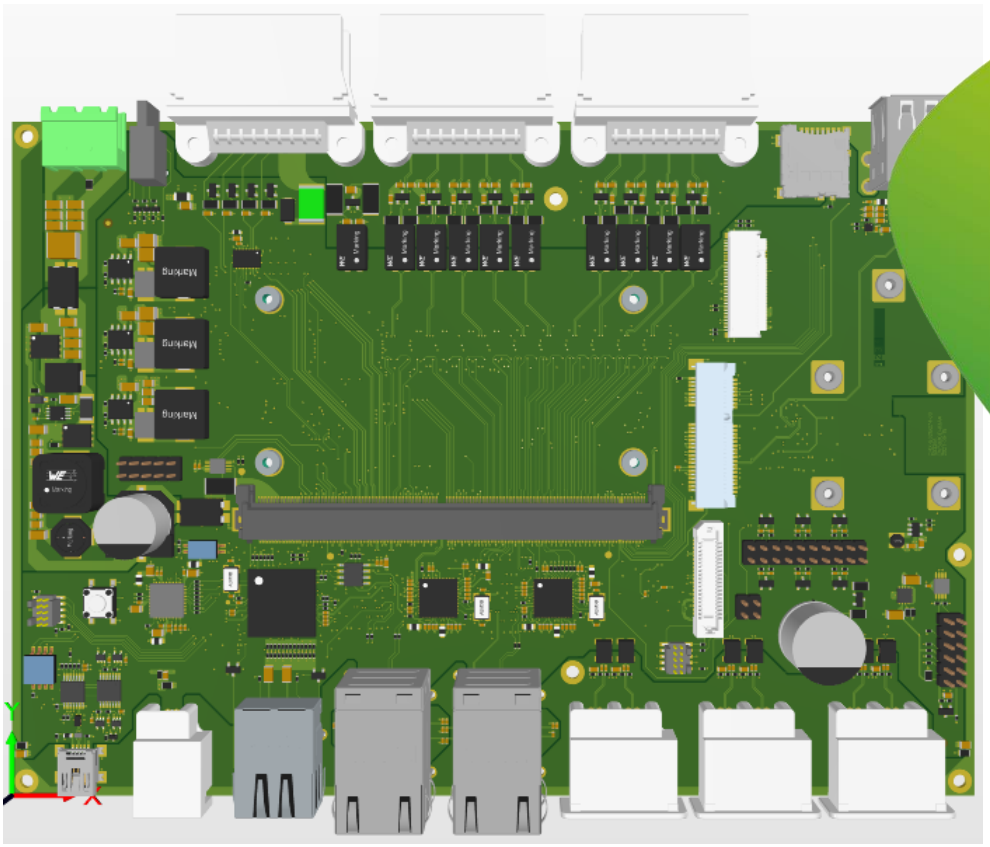

miriac SBC-S32G274A

User Manual (HW Revision 3)

V 3.6

Table of Contents

1 General Notes

1.1 Warranty

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1.5 Symbols, Conventions and Abbreviations

1.5.1 Symbols

Throughout this document, the following symbols will be used:

	***Information marked with this symbol MUST be obeyed to avoid the risk of severe injury, health danger, or major destruction of the unit and its environment***
	***Information marked with this symbol MUST be obeyed to avoid the risk of possible injury, permanent damage or malfunction of the unit.***
	***Information marked with this symbol gives important hints upon details of this manual, or in order to get the best use out of the product and its features.***

Table 1-1 Symbols

1.5.2 Conventions

Symbol	explanation
#	denotes a low active signal
←	denotes the signal flow in the shown direction
→	denotes the signal flow in the shown direction
↔	denotes the signal flow in both directions
→	denotes the signal flow in the shown direction with additional logic / additional ICs in the signal path
I/O	denotes a bidirectional pin
Input	denotes an input pin
matched	denotes the according signal to be routed impedance controlled and length matched
Output	denotes an output pin
Pin 1	refers to the numeric pin of a component package
Pin a1	refers to the array position of a pin within a component package
XXX-	denotes the negative signal of a differential pair
XXX+	denotes the positive signal of a differential pair
XXX	denotes an optional not mounted or fitted part

Table 1-2 Conventions

2 Introduction

Thank you for choosing the MicroSys SBC-S32G274A Single Board Computer system. This manual should help you gain a good understanding of all the features of the SBC-S32G274A.

2.1 Safety and Handling Precautions

	***ALWAYS use the correct type and polarity of the power supply!*** ***DO NOT exceed the rated maximum values for the power supply! This may result in severe permanent damage to the unit, as well as possible serious injury.*** ***ALWAYS keep the unit dry, clean and free of foreign objects. Otherwise, irreparable damage may occur.***
	***Parts of the unit may become hot during operation. Take care not to touch any parts of the circuitry during operation to avoid burns, and operate the unit in a well-ventilated location. Provide an appropriate cooling solution as required.***
	***ALWAYS handle the unit in an ESD-safe manner!*** ***Many pins on external connectors are directly connected to the SoC or other ESD sensitive devices.*** ***Make or break ANY connections ONLY while the unit is switched OFF.*** ***Otherwise, permanent damage to the unit may occur, which is not covered by warranty.***
	***There is no separate SHIELD connection.*** ***All the metal sheaths of shielded connectors are connected to GND.*** ***Also, all mounting holes of the carrier board are connected to GND.*** ***The module's mounting holes are not connected to GND*** ***Take this into account when handling and mounting the unit.***

Table 2-1 Safety and Handling Precautions

2.2 Short Description

The SBC-S32G274A is a small computer system consisting of

- the MPX-S32G274A module, based on NXP's S32G274A Vehicle Network Processor
- and the CRX-S32G carrier board.

It targets both

- evaluation of the MPX-S32G274A SoM
- direct usage as an industrial computing solution

This document gives you an overview on the board's connectors and how to take the first steps on the initial setup.

2.3 Shipping List

The SBC-S32G274A Development Kit contains the following items:

- The SBC-S32G274A system including a suitable heatsink
- Power Supply 12V DC stabilized / 2 A
- Cable adapter for the power supply
- USB cable type A – mini B
- microSD card with U-Boot and Linux
- Documentation:
  a) This hardware manual.
  b) Manual for MPX-S32G274A module "**miriac_MPX-S32G274A_User_Manual.pdf**"

3 Quick Start Guide

3.1 Prerequisites

Always take the necessary ESD precautions when handling the SBC-S32G274A. Otherwise, the unit may suffer permanent damage.

Do not place the unit directly flat on a metal surface, as this may result in short circuits and damage to the board.

Before first using the SBC, unpack the unit and make sure that is clean and free of visible damage or foreign objects.

3.1.1 Minimum Requirements

To operate the board, you will at least need the following items:

- an adequate power supply, delivering 12V DC (stabilized) / 2A minimum. Power ramp up <50ms (0 to 12V), <0,25V / ms.
- a USB cable (type A – mini B) connected to ST6.
- a serial terminal, such as a PC with a USB port running a terminal software (e.g. TeraTerm, HyperTerminal, minicom, putty, ckermit...), or else a hardware serial console. **Choose the following parameters:**
  - (a) **115200 Bd**
  - (b) **8 Data bits**
  - (c) **No parity**
  - (d) **1 Stop Bit**

3.1.2 Recommended Items

The following items are not absolutely necessary, but strongly recommended for practical operation and development purposes:

- Network connection to your local network installation
- TFTP server available for downloading within the network (may run on the same PC as the serial terminal)
- SD card as mass storage and/or boot media

3.2 Board Preparation and Power-Up

- Make sure the switches SW1 and SW2 are set properly in order to select the correct boot source and board configuration
- The board comes preconfigured to boot correctly on arrival.
- Connect the mini USB cable to ST6.
- Connect other peripherals (USB, LAN ...) as needed.
- Connect power to the PWR connector, while the power supply is still switched off.
- Switch on power.

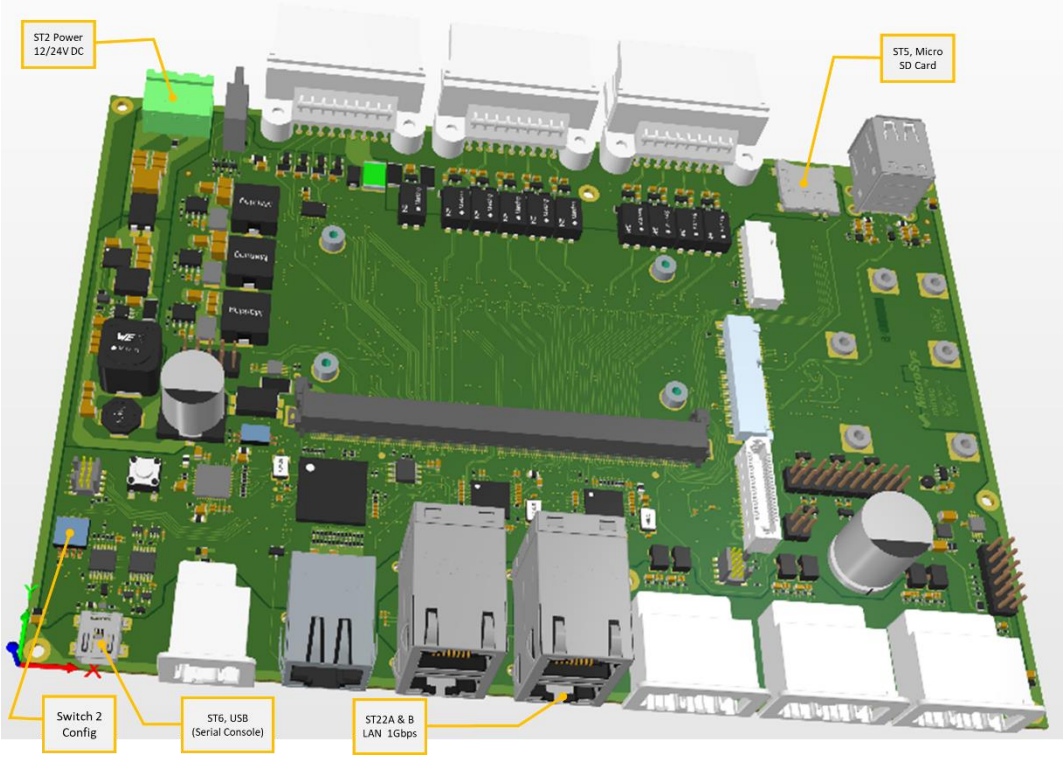


Figure 3-1 System setup example

3.3 Operation

After power-on, the green LED on the module should be lit and any red LED should be off.

IF NOT, DISCONNECT THE UNIT FROM POWER AND CHECK FOR FAULTS!

3.3.1 Default switch settings

Switch SW2 (S32G274A config):

Switch	Default	Function
1	Off	RCW select Default RCW
2	Off	On = boot from SPI on SoM Off = boot from SD card
3	Off	Off = root complex
4	Off	Off = JCOMP signal open

Table 3-1 Switch2 setting

Switch SW3 (SJA1110 config):

Switch	Default	Function
1	Off	BOOT_OPTION0 = 1
2	Off	BOOT_OPTION1 = 1

Table 3-2 Switch3 setting

3.3.2 U-Boot Startup

When power is supplied the system will start and boot into U-Boot.

The exact output may vary, depending on U-Boot and MPX-S32G274A module versions in use.

```
U-Boot 2020.04-4.1+g97081903ce (Mar 03 2021 - 07:18:34
+0000)

CPU: NXP S32G274A rev. 2.1.0
Reset cause: Power-On Reset
Model: MicroSys S32G274ASBC2
DRAM:  3.5 GiB
```

```
U-Boot 2020.04-4.1+g97081903ce (Mar 03 2021 - 07:18:34
+0000)

CPU: NXP S32G274A rev. 2.1.0
Reset cause: Power-On Reset
Model: MicroSys S32G274ASBC2
DRAM:  3.5 GiB
Board: Rev. 2
CA53 core 1 running.
CA53 core 2 running.
CA53 core 3 running.
All (4) cores are up.
MMC:   FSL_SDHC: 0
Loading Environment from EEPROM... OK
DIP EEPROM[0]
  PCIe0 CLK:        100MHz
  PCIe1/SGMII CLK:  125MHz
  RCON EEPROM WP:   no
  SEL SDHC:         SDHC
  BOOT MODE:        RCON
PCIe0 clock 100MHz
Using external clock for PCIe0
Frequency 100Mhz configured for PCIe0
Configuring PCIe0 as RootComplex(x1)&SGMII [XPCS0
OFF(PCIex1), XPCS1 1G]
PCIe1 clock 125MHz
Using external clock for PCIe1
Frequency 125Mhz configured for PCIe1
Configuring PCIe1 as SGMII(x2) [XPCS0 2.5G, XPCS1 OFF]
PCIe0: Failed to get link up
Pcie0: LINK_DBG_1: 0x00000000, LINK_DBG_2: 0x00000800
(expected 0x000000d1)
DEBUG_R0: 0x0070b500, DEBUG_R1: 0x08200000
PCIe1: Not configuring PCIe, PHY not configured
In:    serial
Out:   serial
Err:   serial
USB EHCI 1.00
Net:   eth0: eth_eqos PFE: emac0: sgmii emac1: rgmii
emac2: rgmii , eth1: eth_pfeng

Hit any key to stop autoboot:  0
=>
```

3.4 Ordering Information

Ordering information can be found on the website

https://microsys.de/en/home/

or contact your local sales representative.

4 System Description

This section describes all parts of the SBC-S32G274A system.

4.1 Block Diagram

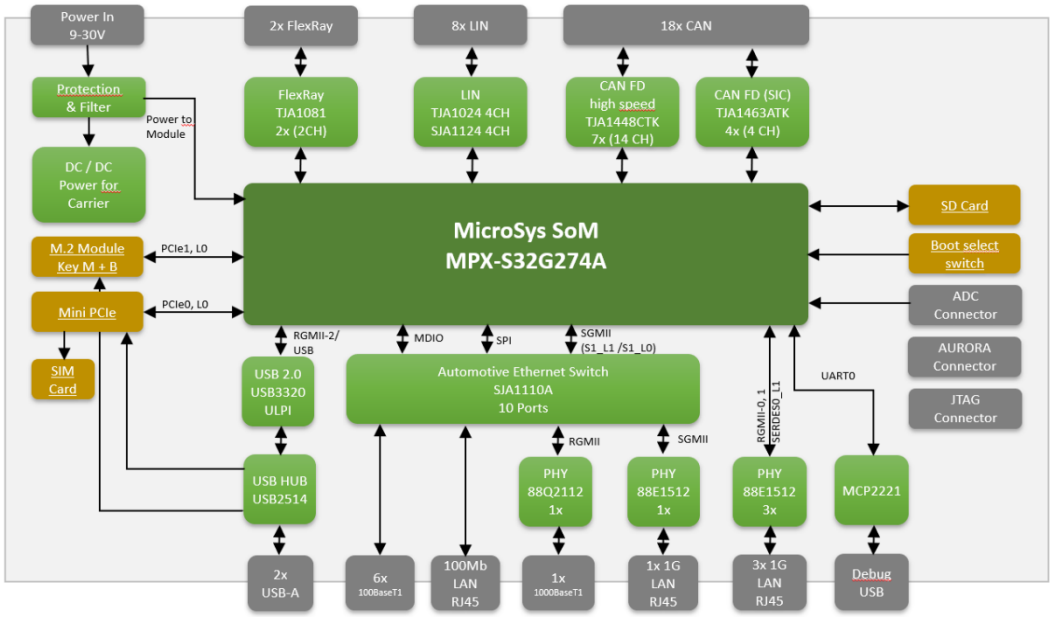


Figure 4-1 Block Diagram (MPX-S32G274A on carrier CRX-S32G-R3)

4.2 Feature Overview

The SBC-S32G274A offers the following features:

1. CRX-S32G carrier (size: 200mm x 140mm)
2. Single power input
    - Range +9V to +30Vdc (+12Vdc is nominal voltage)
    - For LIN operation supply should be limited to <18V; higher voltages will not destroy LIN parts but proper operation is not guaranteed
3. MPX-S32G274A module
    - NXP S32G274A SoC: 4 ARM® Cortex®-A53 64-bit cores, 3x dual-core ARM® Cortex®-M7 cores in lockstep
    - 4GB 64-bit soldered LPDDR4 RAM at 1600MT/s
    - 16GB eMMC and 512Mb QuadSPI Flash
4. Debugging
    - UART0 to USB (FTDI)
    - JTAG1 to SoM (3.3V)
    - JTAG2 interface to components on carrier (1.8V)
    - 40-pin Aurora interface
5. SD card as boot option (multiplexed with eMMC on SoM)
6. USB
    - MAC2 connects to USB-ULPI (Microchip USB3320)
    - USB-Hub (Microchip USB2514)
    - Port 1 to external USB-A connector top
    - Port 2 to mPCIe slot
    - Port 3 to M.2 slot
    - Port 4 to external USB-A connector bottom
7. LAN
    - 2x 1Gbps Ethernet via RGMII directly to S32G274A
    - 1x 1Gbps Ethernet via Serdes0_L1 directly to S32G274A
    - SJA1110 Automotive Ethernet Switch (S1_L1 alt. S1_L0)
        - 1x 100Mbps Ethernet
        - 6x 100Base-T1 Ethernet
        - 1x 1Gbps Ethernet via SGMII
        - 1x 1000BaseT1 Ethernet via RGMII
8. PCIe
    - 1x miniPCIe (Serdes0_L0)
    - 1x M.2 Module type M + B (Serdes1_L0)
9. CAN
    - 2x FlexCAN high speed (TJA1448CTK)
    - 12x LLCE CAN high speed (TJA1448CTK)
    - 4x LLCE CAN FD with SIC (TJA1463ATK)
10. LIN
    - 4x directly to S32G274A
    - 4x from SJA1124 via SPI interface
11. FlexRay (2 channels)
12. ADC
    - 12x analog inputs to ADCs
13. Powercap 0.47F for RTC
14. Development Kit for immediate start up (includes power supply, cables).

Table 4-1 Feature Overview

4.2.1 MPX-S32G274A

For a detailed description of the SoM please refer to the separate document “MPX-S32G274A User Manual”.

The SoM User Manual also provides detailed mechanical dimensions.

4.2.2 CRX-S32G

The following drawing shows the mechanical outline of the SBC-S32G274A assembly.

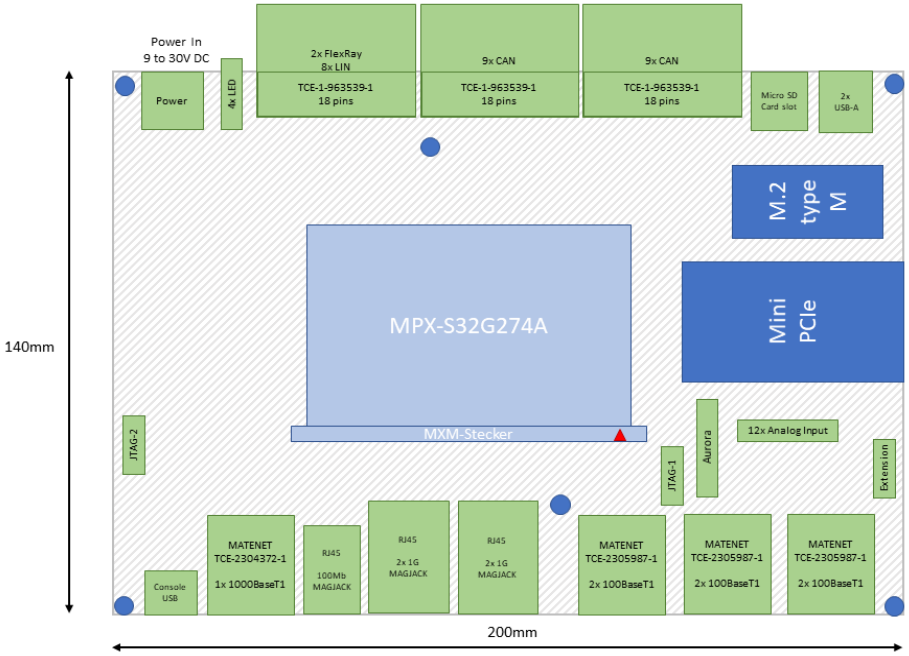


Figure 4-2 CRX-S32G Mechanical Dimensions

4.3 Connector Layout

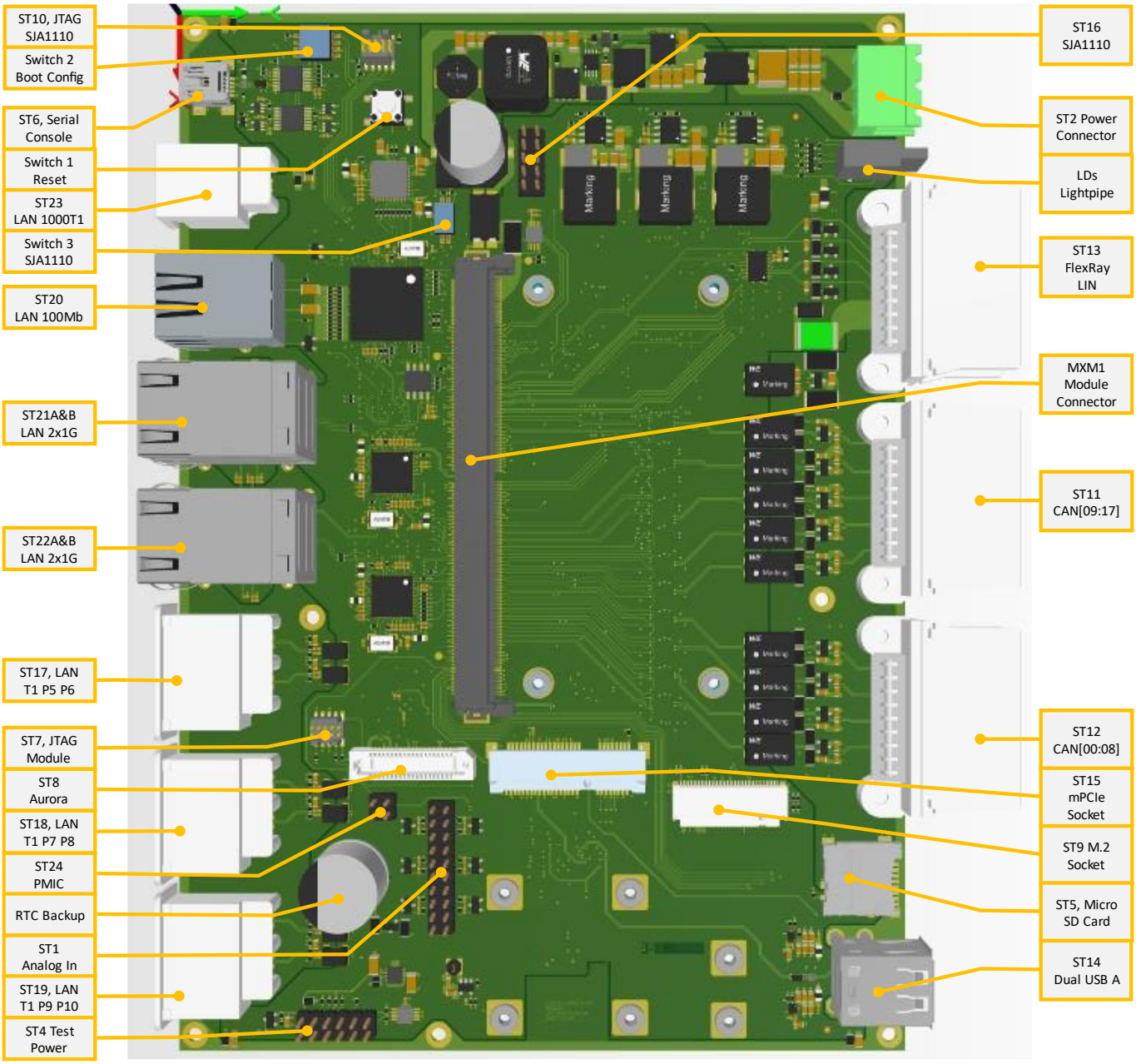


Figure 4-3 Top connectors

Figure 4-4 Bottom connector

4.4 Power Supply

4.4.1 Input Supply Rating

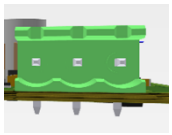
The SBC-S32G274A system is run from a single DC power supply with the following ratings:

Maximum Input Voltage Operating Range:	**9V - 36V DC**
Nominal Input Supply Voltage:	**12V DC**
(@12V / room temperature / U-Boot prompt):	**0.4A = 4.8W**
Carrier without module	**0.18A = 2.16W**
Module without carrier (calculated)	**4.8 – 2.16 = 2.64W**

ALWAYS use the correct type and polarity of the power supply!
DO NOT exceed the rated maximum values for the power supply! This may result in severe permanent damage to the unit, as well as possible serious injury.

4.4.2 Input Power Connector

Part Reference	ST2
Manufacturer:	Phönix Contact
Type:	PHX-1759020



Pinout:

Pin	Silkscreen Label	Signal	Function
1	„KL30“	KL30	Power
2	„KL15“	KL15	Power On
3	„KL31“	KL31	Return

Table 4-1 Pinout Pressure Clamp

4.4.3 Input Protection

The board is protected against wrong polarity and over-voltage spikes.

J1 is for surge protection. It monitors polarity and over-voltage. Voltage “VIN-1” is limited to 36.0V. This is the maximum voltage for supplying regulators and the SoM.

4.4.4 Power Supply Structure

- Input power from PWR connector is fed in parallel to:

  a) MPX-S32G274A module
  b) DC/DC 12V to 5V0 @5A
  c) DC/DC 12V to 3V3 @5A
  d) DC/DC 12V to 1V8 @5A
  e) DC/DC 12V to 7V5 @450mA
- The 3V3 DC are fed to
  a) DC/DC 3.3V to 1V5 @1A
  b) DC/DC 3.3V to 1V1 @1A
  c) DC/DC 3.3V to 0V9 @1A

The following diagram shows the Power Supply structure:

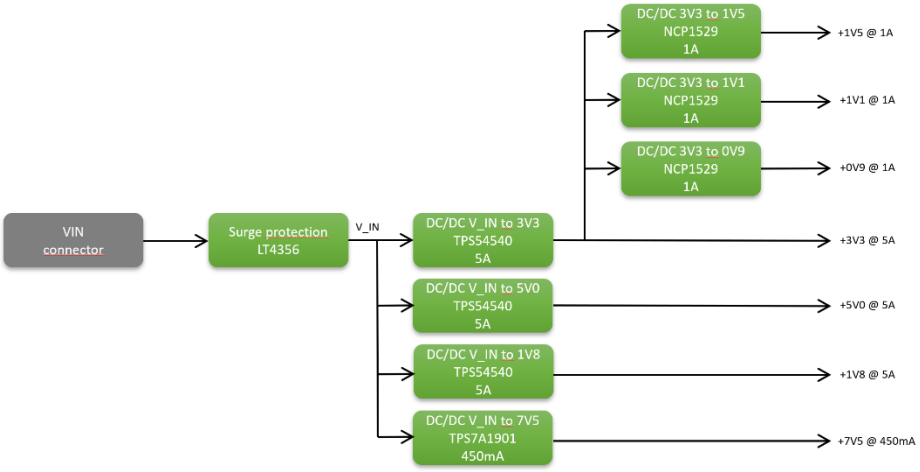


Figure 4-5 Power supply structure

4.4.5 Watchdog

Watchdog is triggered from the S32G274A port PB02. As long as PB02 is not activated the watchdog is inactive. As soon as PB02 is activated once, the watchdog is active and requires a permanent retrigger. It is not possible to stop watchdog activity.

MIC826			MXM1			S32G274A	
Pin	Name		Pin	Signal		Pin	Name
4	*WDI*	←	T111	*PB02*	←	W18	*PB02*

Table 4-2 Watchdog trigger

The MPX-S32G274A module has its own power supply. All SoM internal voltages are generated from V_IN supplied from the carrier.

4.4.6 RTC Backup Battery

The RTC on the module is supplied from a 470mF supercap (C77) that is charged by a power source on the carrier

4.4.7 Power control by KL15

Powerlines may be connected permanent to KL30 (+PWR) and KL31 (-PWR). As long as KL15 is open the board is in standby.

There are 3 scenario for power control:

1. Power controlled
   a) Connect KL30 and KL15 to +PWR
   b) Switch +PWR external
2. KL15 controlled
   a) Connect KL30 to +PWR
   b) Connect KL15 to +PWR to switch ON
   c) Disconnect KL15 (open) to switch OFF
3. KL15 controlled with power hold
   a) Connect KL30 to +PWR
   b) Connect KL15 to +PWR to switch ON
   c) Set GPIO2 in IO-expander J47 (addr 0x44) to 1 for HOLD
   d) Disconnect KL15 (open) to switch OFF
   e) System will remain ON by HOLD
   f) Reset GPIO2 in IO-expander J47 (addr 0x44) to 0 to switch OFF

4.5 Changes from R2 to R3

On R3 some additional functions are available:

Feature	CRX-S32G-R2	CRX-S32G-R3
Board	Size 200 x 140 mm Connector limited to board edge	Size 200 x 140 mm Connectors 2mm beyond board edge to allow for an enclosure
Fixation holes	6 holes	6 holes same position as R2; 1 additonal hole at position 197/50 mm
ST6	Console interface limited to board edge	No change
ST5	SD card connector limited to board edge	No change
ST2	2-pin socket clamp WE-691-101-710-002	3-pin MSTB 2.5/3-G-5.08, PHX-1759020 KL30, KL15, KL31 (automotive)
PowerIN	9 to 30V Board power permanent on Switch external	9 to 36V Board power switched ON by KL15 Power Hold software controlled
ST3	DC Power Jack 90° WE-694-106-106-102	Not available
ST4	10-pin header Voltages with 1K serial resistors	12-pin header Pin 1 to 10 same signals as R2 Pin 3 = +3V3 **NO** serial resistor Pin 6 = +5V0 **NO** serial resistor Pin 11 = I2C2_SDA (buffered) Pin 12 = I2C2_SCL (buffered)
VDD_OTP	Fixed +7.5V set by Adapter Board	Dynamic +7.5V pulse once on power-on
M.2 module	Only size 22/30	Size 22/42 or 22/30 possible Broaching nut for size 22/42
M.2 module	PCIE0_CLKC to M.2 connector	PCIE1_CLKC to M.2 connector
mPCIe	---	Additional micro SIM card connector WE-693-023-010-811
USB	1 USB port Micro USB 2.0 Type B WE-629-105-150-921	2 USB ports Dual USB type A WE-614-008-26021
USB	3-port USB hub USB2513BI	4-port USB hub USB2514BI (if 4-port part is not available 3-port part may be assembled, in which case only 1 port available on ST14)
LEDs	LD1 = green = +5V0 ok LD2 = red = reset	LD1 = green = +5V0 ok LD2 = red = reset LD3 = green = user LED LD4 = red = user LED Lightpipe Mentor 1296.1004

5 System Core, Boot Configuration and On-Board Memory

5.1 S32G274A Processor

The S32G274A is a high-performance vehicle network processor based on Arm Cortex-M7 and Cortex-A53 technology.

- Cluster 0: Dual ARM Cortex-A53
- Cluster 1: Dual ARM Cortex-A53
- L1 cache: 32KB I-cache / 32 KB D-cache per Cortex-A53
- L2 cache: 512 KB per cluster
- Maximum frequency: 1 GHz

For real-time and safety:

- 3x dual-core Arm Cortex-M7 (lockstep)
- L1 cache: 32KB I-cache / 32 KB D-cache per Cortex-M7

5.2 Reset Structure

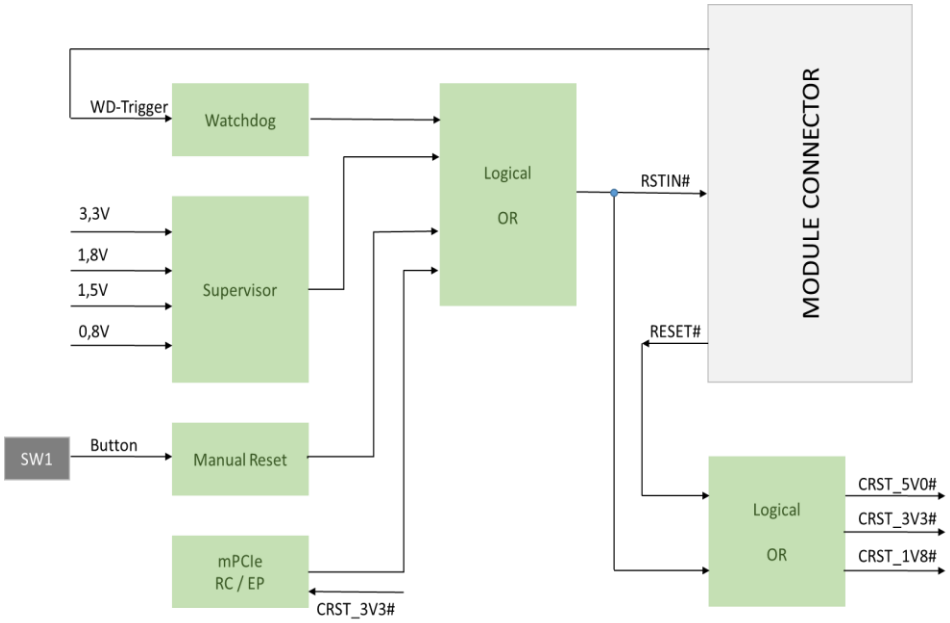


Figure 5-1 Reset Structure (Carrier CRX-S32G-R3)

5.3 Clock Distribution

The clocks are generated and distributed on the SoM.

Please refer to the MPX-S32G274A User Manual.

5.4 Boot Configuration

Boot configuration is described in SoM User Manual.

The boot configuration may be forced by hardware using switch SW2.

5.5 eMMC

Please refer to the MPX-S32G274A User Manual.

5.6 QSPI Flash

Please refer to the MPX-S32G274A User Manual.

5.7 I²C Bus

The SBC-S32G274A offers five independent I²C busses.

The following tables show the I²C addresses as 7-bit addresses. The R/W bit is not displayed.

5.7.1 I2C-0

Used on module for boot configuration.

I²C Bus 0 (7-bit address):

Address	Device	Function
0x51	PCF85263ATL	RTC
0x4C	TMP451AIDQF	Temperature sensor
0x54	BR24G128NUX-3	EEPROM
0x43	FXL6408	IO-Expander
0x4D	PCA9561PW	EEPROM Dip-switch
non	FXMA2102	Bus isolation
0x50	AT24C01C-XHM	EEPROM (boot config)
0x56	AT24C01C-XHM	EEPROM (boot config alternate)

Table 5-1 I²C0 bus map

The I²C Bus 0 has the following layout:

I/O Range: LVTTL

Device	SCL (Signal Name)	Pin	SDA (Signal Name)	Pin
S32G274A	PB01_I2C0_SCL	E7	PB00_I2C0_SDA	W12
	↓		↕	
PCF85263ATL	SCL	5	SDA	8
	↓		↕	
TMP451AIDQF	SCK	8	SDA	7
	↓		↕	
BR24G128NUX-3	SCL	6	SDA	5
	↓		↕	
FXL6408	SCL	13	SDA	14
	↓		↕	
FXMA2102	SCL	2	SDA	3
	↓		↕	
Module Connector	PB01_I2C0_SCL	B133	PB00_I2C0_SDA	B134

Table 5-2 I²C-0 pin assignment

There are no devices on the carrier using this bus.

5.7.2 I2C-1

Available on carrier, no components on module, pull up to +3V3_LDO3.

I²C Bus 1 (7-bit address):

Address	Device	Function
0x43	FXL6408	IO-Expander
0x44	FXL6408	IO-Expander
0x7F	MAX961xAUB	Current sensor
undefined	PCA9511	I2C buffer
undefined	mPCIe slot	Depends on card inserted

Table 5-3 I²C1 bus map

The I²C Bus 1 has the following layout:

I/O Range: LVTTL

Device	SCL (Signal Name)	Pin	SDA (Signal Name)	Pin
S32G274A	PB03_I2C1_SCL	C6	PB04_I2C1_SDA	E8
	↓		↕	
Module Connector	PB03_I2C1_SCL	B135	PB04_I2C1_SDA	B136
	↓		↕	
MAX961x	SCL	6	SDA	7
	↓		↕	
FXL6408	SCL	13	SDA	14
	↓		↕	
FXL6408	SCL	13	SDA	14
	↓		↕	
PCA9511	SCL	3	SDA	6

Table 5-4 I²C-1 pin assignment

5.7.3 I2C-2

Available on carrier, no components on module, pull up to +3V3_LDO3.

The I²C Bus 2 has the following layout:

I/O Range: LVTTL

Device	SCL (Signal Name)	Pin	SDA (Signal Name)	Pin
S32G274A	PB05_I2C2_SCL	A6	PB06_I2C2_SDA	G9
	↓		↕	
Module Connector	PB05_I2C2_SCL	B137	PB06_I2C2_SDA	B138
	↓		↕	
PCA9517ADP	PB05_I2C2_SCL	7	PB05_I2C2_SDA	6
	↓		↕	
ST4	I2C2_SCL_EXT	12	I2C2_SDA_EXT	11

Table 5-5 I²C-2 pin assignment

5.7.4 I2C-3

Pins available on carrier but used for FXCAN3.

The I²C Bus 3 has the following layout:

I/O Range: LVTTL

Device	SCL (Signal Name)	Pin	SDA (Signal Name)	Pin
S32G274A	PB13_FXCAN3_TX	G7	PB14_FXCAN3_RX	E6
	↓		↕	
Module Connector	PB13_FXCAN3_TX	B102	PB14_FXCAN3_RX	B103

Table 5-6 I²C-3 pin assignment

5.7.5 I2C-4

Used on module for PMIC communication. Not available on carrier

The I²C Bus 4 has the following layout:

I/O Range: LVTTL

Device	SCL (Signal Name)	Pin	SDA (Signal Name)	Pin
S32G274A	PC02_I2C4_SCL_PMIC	W8	PC01_I2C4_SDA_PMIC	Y8
	↓		↕	
MVR5510AMDA4ES	SCL	10	SDA	11

Table 5-7 I²C-4 pin assignment

5.7.6 I2C_SCL_PROG

Interface to program RCON EEPROM on SoM.

5.8 IO-Expander

GPIO pins on the S32G274A are extended by a GPIO expander FXL6408:

- I²C clock frequency up to 400 kHz
- One interrupt out signaling pin state changes

J14 has 8 GPIOs which are used as follows:

GPIO Expander						
Pin	**Signal**			**Pin**	**Signal**	**Signal conditioning**
12	GPIO0 IN	←	J27	13	SJA1124_STAT	PU: 1K0
11	GPIO1 IN	←	J27	16	SJA1124_INT#	PU: 1K0
8	GPIO2 IN	←	J39	D5	AETH_IRQ#	PU: 1K0
7	GPIO3 OUT	←	J39	G4	AETH_RST_CORE#	PU: 1K0
6	GPIO4 IN	←	J41	12	LAN_IRQ#	PU: 1K0
5	GPIO5 IN	←	ST5	9	SD_CD#	PU: 1K0
4	GPIO6 OUT	←	J26	2,5,8,11	LIN_SLP	PU: 1K0
3	GPIO7 OUT	←				

Table 5-8 GPIO Expander: Pin description

J47 has 8 GPIOs which are used as follows:

GPIO Expander						
Pin	**Signal**			**Pin**	**Signal**	**Signal conditioning**
12	GPIO0 IN	←	J45	9	SERDES_SEL	PU: 10K0
11	GPIO1 IN	←	TR22	6	KL15_IN	PU: 10K0
8	GPIO2 OUT	←	TR22	5	KL15_HOLD	PU: 10K0
7	GPIO3 OUT	←				
6	GPIO4 OUT	←	TR23	1	USR_LED1	PU: 10K0
5	GPIO5 OUT	←	TR24	1	USR_LED1	PU: 10K0
4	GPIO6 OUT	←	J59	6	CANSIC_EN	PU: 10K0
3	GPIO7 OUT	←	J57	2	STBY_ON#	PD: 1K0

Table 5-9 GPIO Expander: Pin description

S32G274A			GPIO Expander		
Ball	**Signal**		**Pin**	**Signal**	**Signal conditioning**
B5	PB15	←	1	PB15	

Table 5-10 GPIO Expander: IRQ

6 Peripherals

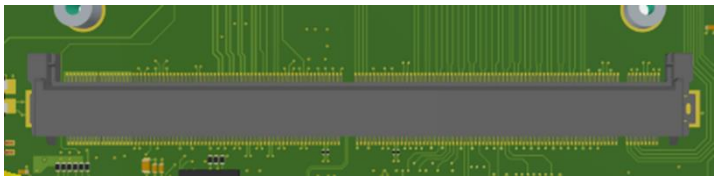
6.1 Connector References

Reference	Function	Ass	Mating Parts
MXM1	SoM Connector JAE-MM70-314-B1-2	✓	Module with edge connector
ST1	ADC-Connector Header WE-61302021121	✓	Any socket 2x10 pin, 2.54mm
ST2	Power connector PHX- 1759020	✓	PHX-1754571
ST4	Test connector supply Header WE-6130-12-211-21	✓	Any socket 2x6 pin, 2.54mm
ST5	Micro SD slot PJS-008-2130	✓	Micro SD card
ST6	Mini USB 2.0 type B WE-65100516121	✓	Mini USB type B
ST7	JTAG i/f to module MIPI-10 SAM-FTSH-105-01-L-DV-K	✓	MIPI-10 connector
ST8	Aurora interface SAM-ASP-130367-01	✓	
ST9	M.2 interface type M (B) TCE-2199230-6	✓	M.2 standard card
ST10	JTAG i/f to SJA1110 SAM-FTSH-105-01-L-DV-K	✓	MIPI-10 connector
ST11	CAN 09 to 17 Automotive connector MQS TCE-1-963539-1	✓	TCE-1355348-1
ST12	CAN 00 to 08 Automotive connector MQS TCE-1-963539-1	✓	TCE-1355348-1
ST13	FlexRay, LIN Automotive connector MQS TCE-1-963539-1	✓	TCE-1355348-1
ST14	Dual USB-A WE- 614-008-26-021	✓	Dual USB type A
ST15	Mini PCIe slot TYC-2041119-1-MPCIE	✓	Mini PCIe cards
ST16	SPI to SJA1110 Header WE-6130-10-211-21	✓	Any socket 2x5 pin, 2.54mm
ST17	MATENET to T1 TCE-2305987-1	✓	TCE-8-2307961-9
ST18	MATENET to T1 TCE-2305987-1	✓	TCE-8-2307961-9
ST19	MATENET to T1 TCE-2305987-1	✓	TCE-8-2307961-9
ST20	RJ45 connector 100MB WE-749-901-1121A	✓	RJ45 standard cable
ST21	Dual RJ45 connector 1G WE-749-915-1120	✓	RJ45 standard cable
ST22	Dual RJ45 connector 1G WE-749-915-1120	✓	RJ45 standard cable
ST23	MATENET to T1 TCE-2320201-1	✓	TCE-2302510-1

Table 6-1 Connector reference overview

6.2 Module Connector

The carrier CRX-S32G provides connector MXM1 which accepts compatible SoMs from the MicroSys MPX2 family.



Manufacturer:	JAE
Type:	JAE-MM70-314-B1-2
Used with:	MicroSys MPX2 module family

6.3 PCIe / SerDes Usage

The S32G274A processor has 2 SerDes interfaces each with 2 lanes. Valid SerDes configurations can be found in the S32G274A Reference Manual under SerDes Working Modes. The table below shows the configurations used on the CRX-S32G carrier. To increase functionality the CRX-S32G uses a SerDes multiplexer for the SerDes_1 lanes. The so-called default selection allows the mPCIe and M.2 slots to be used simultaneously and the SGMII connection between processor and SJA1110 is 1Gbps (with a SerDes reference clock of 100MHz). With the alternate selection the M.2 slot is not available, but the SGMII connection between S32G274A and SJA1110 is now 2.5Gbps (with a SerDes reference clock of 125MHz).

SerDes names reference connector names. Some differ from numbering at the processor. Note that PCIE0_0 is synonomous with 'SerDes_0 lane 0' and correspondingly PCIE1_1 is 'SerDes_1 lane 1'.

Connector	S32G274A	Usage
PCIE0_0	PCIE0_0	Mini PCIe connector
PCIE0_1	PCIE0_1	1G SGMII to ST21A
PCIE1_0	PCIE1_0	Default: M.2 connector Alternate: 2.5G SGMII to SJA1110 port4
PCIE1_1	PCIE1_1	Default: 1G SGMII SJA1110 port4 Alternate: not available

Table 6-2 SerDes Usage

The U-Boot environment variable hwconfig is used to switch between default (M2) and alternate (2G5) by means of the SERDES_SEL signal.

6.4 LAN Connections

The SBC-S32G274A system offers:

- 1 Gigabit LAN connection to automotive switch SJA1110 (default SerDes_1 lane 1)
- 2.5 Gigabit LAN connection to automotive switch SJA1110 (alternate SerDes_1 lane 0)
- 5 independent 1Gbps LAN connections
    - 1x SerDes_0 lane1

  - 2x RGMII to S32G274A
  - 1x SGMII to SJA1110
  - 1x 1000BaseT1 via RGMII to SJA1110
- 1x 100Mb LAN connection to SJA1110
- 6x 100BaseT1 LAN to SJA1110

The RJ45 connectors use the standard pinning for Gbit Ethernet, i.e. the pairs are 1-2, 3-6, 4-5 and 7-8.

Pin	Pair
1	D-A+
2	D-A-
3	D-B+
4	D-C+
5	D-C-
6	D-B-
7	D-D+
8	D-D-

Table 6-3 LAN Gigabit Ethernet connector pairs

6.4.1 LAN Structure

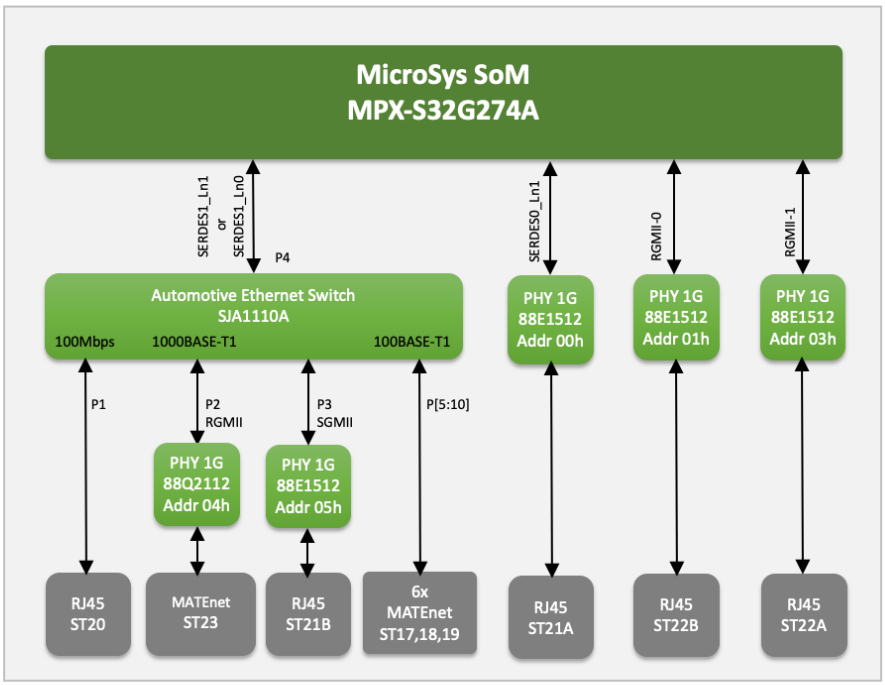


Figure 6-1 CRX-S32G LAN structure

The following diagram shows LAN connectors:

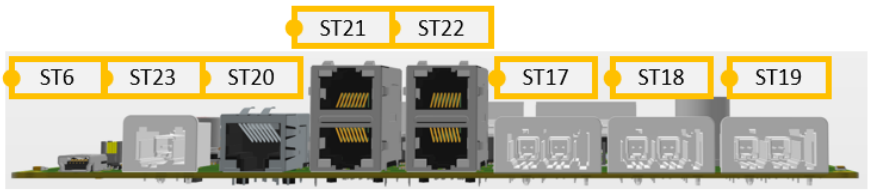


Figure 6-2 LAN connector view

SoM MPX-S32G274A	Switch SJA1110	PHY	Connector
SerDes_0 Lane0	---	---	Mini PCIe TCE- 2041119-1
SerDes_1 Lane0	---	---	M.2 Module TCE-2199230-M
---	P1	SJA1110 internal 100Base-TX	RJ45 WE-749-901-1121A
---	P2	1000BaseT1 LAN 88Q2112 RGMII MDIO addr = 0x04	MATENET TCE-2304372-1
---	P3	1G LAN PHY 88E1512P SGMII MDIO addr = 0x05	RJ45 WE-749-915-1120
SerDes_1 Lane1 (default)	P4 1Gbps i/f MDIO addr = 0x010	---	---
SerDes_1 Lane0 (alternate)	P4 2.5Gbps i/f MDIO addr = 0x010	---	---
---	P[5:10]	SJA1110 internal 6 ports 100Base-T1	MATENET TCE-2305987-1
SerDes_0 Lane1	---	1G LAN PHY 88E1512P SGMII MDIO addr = 0x00	RJ45 WE-749-915-1120
RGMII0	---	1G LAN PHY 88E1512P RGMII MDIO addr = 0x01	RJ45 WE-749-915-1120
RGMII1	---	1G LAN PHY 88E1512P RGMII MDIO addr = 0x03	RJ45 WE-749-915-1120
RGMII2	---	USB-ULPI Microchip USB3320 Followed by hub Microchip USB2514	Dual USB-A WE- 614-008-26021

Table 6-4 LAN Structure

6.4.2 MDIO addressing

MDIO-0 from MAC0 is connected to PHYs: 2x 88E1512P, SJA1110

Part	component	Address
J41	88E1512P	Addr = 0x00h (ST21A) (SGMII from S32G)
J43	88E1512P	Addr = 0x01h (ST22B) (RGMII from S32G)
J39	SJA1110	Addr = 0x10h Addr = 0x08h … 0x0dh (6x T1 Phys)

Table 6-5 LAN / MDIO0 / Addressing

MDIO-1 from MAC1 is connected to PHYs: 1x 88E1512P

Part	component	Address
J44	88E1512P	Addr = 0x03h (ST22A) (RGMII from S32G)

Table 6-6 LAN / MDIO1 / Addressing

MDIO-SJA1110 is connected to PHYs: 1x 88E1512P, 1x 88Q2112

Part	component	Address
J42	88E1512P	Addr = 0x05h (ST21B) (SGMII from SJA1110)
J8	88Q2112	Addr = 0x04h (ST23) (RGMII from SJA1110)

Table 6-7 LAN / MDIO0 / Addressing

6.4.3 1G LAN SerDes_0 Lane1 (ST21A)

The SGMII lanes connect to Marvell PHY 88E1512P.

88E1512P			MXM1			S32G274A	
Pin	Name		Pin	Signal		Pin	Name
1	*S_INP*	←	T88		←	W18	*PCIE1_TX1_P*
2	*S_INN*	←	T87		←	Y18	*PCIE1_TX1_N*
4	*S_OUTP*	→	T73		→	AB21	*PCIE1_RX1_P*
5	*S_OUTN*	→	T72		→	AC21	*PCIE1_RX1_N*

Table 6-8 SerDes 1 pin assignment

LED	Signal (in SCM)	Port (88E1512P)	Pin
GN	SGMII_P0_LED0	LED[0]	14
YE	SGMII_P0_LED1	LED[1]	13

Table 6-9 ST21A (1G) LEDs

Connector pinning is standard RJ45

6.4.4 1G LAN RGMII-0 (ST22B)

Marvell PHY 88E1512P connected to:

88E1512P			MXM1			S32G274A	
Pin	Name		Pin	Signal		Pin	Name
46	*RX_CLK*	→	T59		→	V21	*RGMII0_RX_CLK*
43	*RX_CTRL*	→	T58		→	W23	*RGMII 0_RXDV*
44	*RXD0*	→	T56		→	T20	*RGMII 0_RXD0*
45	*RXD1*	→	T55		→	Y23	*RGMII 0_RXD1*
47	*RXD2*	→	T54		→	W21	*RGMII 0_RXD2*
48	*RXD3*	→	T53		→	W22	*RGMII 0_RXD3*
53	*TX_CLK*	←	T67		←	V20	*RGMII 0_TX_CLK*
50	*TXD0*	←	T64		←	U19	*RGMII 0_TXD0*
51	*TXD1*	←	T63		←	T19	*RGMII 0_TXD1*
54	*TXD2*	←	T62		←	U18	*RGMII 0_TXD2*
55	*TXD3*	←	T61		←	U20	*RGMII 0_TXD3*
56	*TX_CTRL*	←	T66		←	T18	*RGMII 0_TX_EN*
8	*MDIO*	↔	T51		↔	V17	*RGMII 0_MDIO*
7	*MDC*	←	T50		←	Y21	*RGMII 0_MDC*
9	*CLK125*	→			→		

Table 6-10 Port 2 (RGMII0) interface to S32G274A

LED	Signal	Port (88E1512P)	Pin
GN	RGMII_P3_LED0	LED[0]	14
YE	RGMII_P3_LED1	LED[1]	13

Table 6-11 ST22B (1G) LEDs

Connector pinning is standard RJ45

6.4.5 1G LAN RGMII-1 (ST22A)

Marvell PHY 88E1512P connected to:

88E1512P			MXM1			S32G274A	
Pin	Name		Pin	Signal		Pin	Name
46	*RX_CLK*	→	T39		→	R21	*RGMII 1_RX_CLK*
43	*RX_CTRL*	→	T40		→	R23	*RGMII 1_RXDV*
44	*RXD0*	→	T37		→	P19	*RGMII 1_RXD0*
45	*RXD1*	→	T36		→	P18	*RGMII 1_RXD1*
47	*RXD2*	→	T35		→	N18	*RGMII 1_RXD2*
48	*RXD3*	→	T34		→	U21	*RGMII 1_RXD3*
53	*TX_CLK*	←	T48		←	P20	*RGMII 1_TX_CLK*
50	*TXD0*	←	T45		←	T23	*RGMII 1_TXD0*
51	*TXD1*	←	T44		←	T22	*RGMII 1_TXD1*

88E1512P			MXM1			S32G274A	
54	*TXD2*	←	T43		←	U22	*RGMII 1_TXD2*
55	*TXD3*	←	T42		←	T21	*RGMII 1_TXD3*
56	*TX_CTRL*	←	T47		←	U23	*RGMII 1_TX_EN*
8	*MDIO*	↔	T32		↔	R19	*RGMII 1_MDIO*
7	*MDC*	←	T32		←	V23	*RGMII 1_MDC*
9	*CLK125*	→			→		

Table 6-12 Port 3 (RGMII1) interface to S32G

LED	Signal	Port (88E1512P)	Pin
GN	RGMII_P2_LED0	LED[0]	14
YE	RGMII_P2_LED1	LED[1]	13

Table 6-13 ST22A (1G) LEDs

Connector pinning is standard RJ45

6.4.6 SJA1110 Automotive Switch

Ethernet capabilities are extended by the use of an SJA1110A automotive Ethernet switch with 10 ports. The SJA1110A integrates:

- Six IEEE 100BaseT1 Phys
- One IEEE 100BaseTX PHY
- Two MII/RMII/RGMII interfaces
- Four SGMII interfaces
- An Arm Cortex-M7 based host controller

SJA1110A supports Audio Video Bridging (AVB) and the latest Time-Sensitive Networking (TSN) standards.

Port	Usage
P1	100Mbps LAN, ST20
P2	1000Base-T1, RGMII to 88Q2112 PHY, ST23
P3	1G LAN, SGMII to 88E1512P PHY, ST21B
P4	SerDes connection to S32G274A, SerDes_1_Lane1 (alternate SerDes_1_Lane0)
P5	100Base-T1, ST17
P6	100Base-T1, ST17
P7	100Base-T1, ST18
P8	100Base-T1, ST18
P9	100Base-T1, ST19
P10	100Base-T1, ST19

Table 6-14 SJA1110 Port Usage

Default: (M.2 mode) SerDes_1 Lane1 is used to connect S32G274A to SJA1110 port 4.

SJA1110 (port 4)			MXM1			S32G274A	
Pin	Name		Pin	Signal		Pin	Name
K2	*S_INP*	←	T88		←		*PCIE1_TX1_P*
K1	*S_INN*	←	T87		←		*PCIE1_TX1_N*
L2	*S_OUTP*	→	T73		→		*PCIE1_RX1_P*
L1	*S_OUTN*	→	T72		→		*PCIE1_RX1_N*

Table 6-15 SerDes1_L1 pin assignment

Alternate: (2G5) SerDes_1 Lane0 is used to connect S32G274A to SJA1110 port 4.

SJA1110 (port 4)			MXM1			S32G274A	
Pin	Name		Pin	Signal		Pin	Name
K2	*S_INP*	←	T85		←	W19	*PCIE1_TX0_P*
K1	*S_INN*	←	T84		←	Y18	*PCIE1_TX0_N*
L2	*S_OUTP*	→	T70		→	AA22	*PCIE1_RX0_P*
L1	*S_OUTN*	→	T69		→	AB22	*PCIE1_RX0_N*

Table 6-16 SerDes1_L0 pin assignment

Default / Alternate is determined by a multiplexer using the SERDES_SEL signal.

6.4.7 1G LAN SGMII (ST21B)

Marvell PHY 88E1512P is connected to SJA1110 port 3:

88E1512P					SJA1110	
Pin	Name				Pin	Name
1	*S_INP*	←		←	L16	*AETH_P3_TX_P*
2	*S_INN*	←		←	L15	*AETH_P3_TX_N*
4	*S_OUTP*	→		→	K16	*AETH_P3_RX_P*
5	*S_OUTN*	→		→	K15	*AETH_P3_RX_N*

Table 6-17 1G LAN interface to SJA1110 port 3

LED	Signal (in SCM)	Port (88E1512P)	Pin
GN	SGMII_P0_LED0	LED[0]	14
YE	SGMII_P0_LED1	LED[1]	13

Table 6-18 ST21B (1G) LEDs

Connector pinning is standard RJ45

6.4.8 100Mbps LAN (ST20)

The SJA1110A automotive Ethernet switch includes a 100Mbps PHY.

Signals are directly connected to ST20.

Externally there is 1 pair for transmit (pins 1, 2) and 1 pair for receive (pins 3, 6).

LED	Signal (in SCM)	GPIO (on SJA1110)	Pin
GN	CBTX_LED_GN	GPIO15	M5
YE	CBTX_LED_YE	GPIO14	L5

Table 6-19 100Mbps LEDs

6.4.9 1000Base-T1 (ST23)

Marvell PHY 88Q2112 is connected to SJA1110 port 2:

88Q2112 (J8)					SJA1110	
Pin	Name				Pin	Name
23	*RX_CLK*	→		→	B5	*AETH_MII2_RX_CLK*
22	*RX_CTRL*	→		→	A3	*AETH_MII2_RXDV*
21	*RXD0*	→		→	A5	*AETH_MII2_RXD0*
20	*RXD1*	→		→	B4	*AETH_MII2_RXD1*
19	*RXD2*	→		→	A4	*AETH_MII2_RXD2*
18	*RXD3*	→		→	B3	*AETH_MII2_RXD3*
25	*TX_CLK*	←		←	B6	*AETH_MII2_TX_CLK*
27	*TXD0*	←		←	A8	*AETH_MII2_TXD0*
28	*TXD1*	←		←	B8	*AETH_MII2_TXD1*
29	*TXD2*	←		←	A7	*AETH_MII2_TXD2*
30	*TXD3*	←		←	B7	*AETH_MII2_TXD3*
26	*TX_CTRL*	←		←	A6	*AETH_MII2_TX_EN*
39	*MDIO*	↔		↔	C16	*AETH_MDIO*
38	*MDC*	←		←	C15	*AETH_MDC*

Table 6-20 Port 1 interface to SJA1110 port 2

ST23	Signal (in SCM)	Port (SJA1110)	88Q2112
1	L1000B-T1_P	Port 2	4
2	L1000B-T1_N	Port 2	5

Table 6-21 ST23 Pinout

6.4.10 100Base-T1 LAN (ST17, ST18, ST19)

SJA1110 automotive switch includes 6x 100Base-T1 PHYs.

Signals are directly connected to ST17, ST18, ST19 (2 ports each)

ST17	Signal (in SCM)	Port (SJA1110)	Pin
1	ENET1_P	Port 5	T3
2	ENET1_N	Port 5	T4
3	ENET2_P	Port 6	T5
4	ENET2_N	Port 6	T6

Table 6-22 ST17 Pinout

ST18	Signal (in SCM)	Port (SJA1110)	Pin
1	ENET3_P	Port 7	T7
2	ENET3_N	Port 7	T8
3	ENET4_P	Port 8	T9
4	ENET4_N	Port 8	T10

Table 6-23 ST18 Pinout

ST19	Signal (in SCM)	Port (SJA1110)	Pin
1	ENET5_P	Port 9	T11
2	ENET5_N	Port 9	T12
3	ENET6_P	Port 10	T13
4	ENET6_N	Port 10	T14

Table 6-24 ST19 Pinout

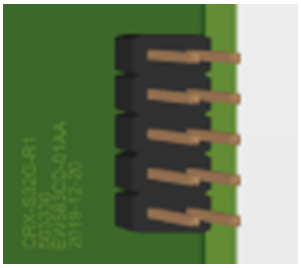
6.4.11 SJA1110 Standalone (ST16)

ST16 is used if SJA1110 is operating standalone. In this case, the SJA1110 EEPROM may be programmed via this connector.

ST16 signals are available on a 2x5 pin header.

Interface is 3.3V logic level.

Part Reference:	ST16
Manufacturer:	any
Type:	HEADER-2.54-180-M-2X5 WE-6130-10-211-21



ST16			MXM1			S32G274A	
Pin	**Signal**		**Pin**	**Signal**		**Pin**	**Signal**
1	+3V3						
2	GND						
3	PA13_DSPI0_SCK	←	B68		←	U12	PA13_DSPI0_SCK
4	PB09_DSPI0_CS1	←	B70		←	AA10	PB09_DSPI0_CS1
5	PA14_DSPI0_SIN	→	B69		→	AA12	PA14_DSPI0_SIN
6	PB10_DSPI0_CS2	←	B71		←	V11	PB10_DSPI0_CS2
7	PA15_DSPI0_SOUT	←	B67		←	W13	PA15_DSPI0_SOUT
8	RGMII2_MDC/DSPIO_CS7	←	T12		←	M19	RGMII2_MDC/DSPIO_CS7
9	MAC0_MDIO	↔	B51		↔	V17	MAC0_MDIO
10	MAC0_MDC	←	B50		←	Y21	MAC0_MDC

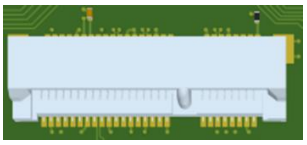
Table 6-25 SJA1110 Programming Connector Pinout

6.5 PCIe Connections

6.5.1 Mini PCIe Slot (ST15)

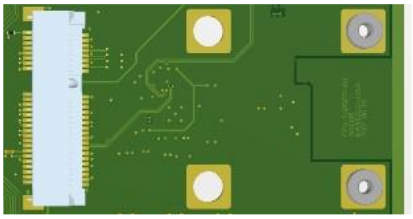
There is one mini PCIe slot with USB support on the carrier.

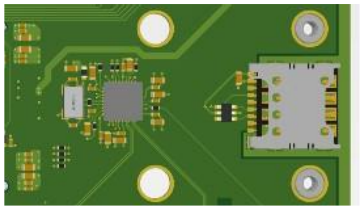
Part Reference:	ST15
Manufacturer:	Tyco
Type:	2041119-1
Used with:	Half-size mini PCIe cards are preferred



Broaching nuts for both half and full size cards are placed on the carrier. When full-size cards are used care has to be taken to choose cards that do not have parts on the bottom side accidentally shorting signals.

MicroSys recommends to use only half-size cards with this slot!





Pin:			Pin:
1	WAKE# ➔ PU +3V3	+3.3V	2
3	COEX1 ➔ nc	GND	4
5	COEX2 ➔ nc	+1.5V	6
7	CLKREQ# ➔ nc	UIM-PWR ➔ nc	8
9	GND	UIM-DAT ➔ nc	10
11	REFCLK-	UIM-CLK ➔ nc	12
13	REFCLK+	UIM-RST ➔ nc	14
15	GND	UIM-VPP ➔ nc	16
MECHANICAL KEY			
17	Reserved ➔ nc	GND	18
19	Reserved ➔ nc	WDIS# ➔ nc	20
21	GND	PERST#	22
23	PER0- = PCIE0_RX0_N	+3.3V	24
25	PER0+ = PCIE0_RX0_P	GND	26
27	GND	+1.5V	28
29	GND	SMB-CLK = I2C1_SCL_PCIE1	30
31	PET0- = PCIE0_TX0_N	SMB-DAT = I2C1_SDA_PCIE1	32
33	PET0+ = PCIE0_TX0_P	GND	34
35	GND	USB-D- = USB2_D_N	36
37	GND	USB-D+ = USB2_D_P	38
39	+3.3V	GND	40

Pin:			Pin:
41	+3.3V	LED-WWAN# ➔ nc	42
43	GND	LED_WLAN# ➔ nc	44
45	Reserved ➔ nc	LED_WPAN#➔ nc	46
47	Reserved➔ nc	+1.5V	48
49	Reserved ➔ nc	GND	50
51	Reserved ➔ nc	+3.3V	52

Table 6-26 mPCIe Slot Pinout

The following table shows the internal connections:

ST15			MXM1			S32G274A	
Pin	Name		Pin	Signal		Pin	Name
23	*PCIE0_RX0_N*	→	T75		→	AC19	*PCIE0_RX0_N*
25	*PCIE0_RX0_P*	→	T76		→	AB19	*PCIE0_RX0_P*
31	*PCIE0_TX0_N*	←	T90		←	Y16	*PCIE0_TX0_N*
33	*PCIE0_TX0_P*	←	T91		←	W16	*PCIE0_TX0_P*

Table 6-27 mPCIe Slot SerDes_0_Ln0 Assignment

NOTE

AC coupling capacitors for PER0_N and PER0_P have to be placed on the plug-in card near the transmitter.

USB channel is connected to USB2 from hub J33 (USB2514).

Mini-PCIe card connector is interfaced to SIM-card connector on CRX-S32G carrier via UIM-interface. SIM-card is located on bottom under mini-PCIe card. It is accessible from the right side of the board.
If there is a SIM-card on the module either card on module or the card on carrier may be used, but only one at time.

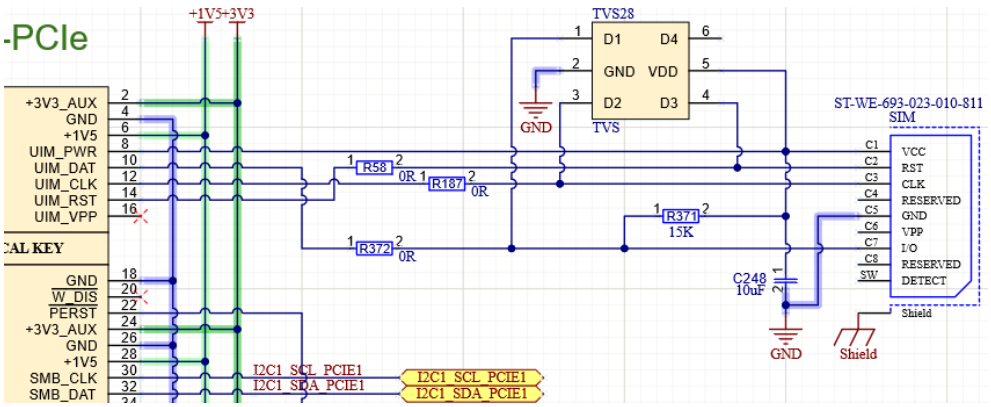
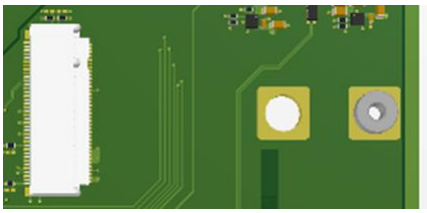


Figure 6-3 SIM-card interface on carrier

6.5.2 M.2 Socket (ST9)

There is one M.2 slot with USB support on the carrier. Key IDs of B and M are supported. A mounting hole for M.2 cards of length 42 / 30mm is provided. Longer M.2 cards can be inserted but will protrude over the edge of the carrier.

Part Reference:	ST9
Manufacturer:	Tyco
Type:	2199230-6
Used with:	M.2 NVMe cards



Pin:			Pin:
1	GND	+3.3V	2
3	GND	+3.3V	4
5	PERN3	NC6	6
7	USB_D+ = USB3_D_P	PLN# ➔ PU +3V3	8
9	USB_D- = USB3_D_N	DAS/DSS#	10
11	PETN3	+3.3V	12
13	PETP3	+3.3V	14
15	GND	+3.3V	16
17	PERN2	+3.3V	18
19	PERP2	NC20	20
21	GND	NC22	22
23	PETN2	NC24	24
25	PETP2	NC26	26
27	GND	NC28	28
29	PERN1	PLA#	30
31	PERP1	NC32	32
33	GND	NC34	34
35	PETN1	NC36	36
37	PETP1	DEVSLP	38
39	GND	NC40	40
41	PERN0 = PCIE0_RX1_N	NC42	42
43	PERP0 = PCIE0_RX1_P	NC44	44
45	GND	NC46	46
47	PETN0 = PCIE0_TX1_N	NC48	48
49	PETP0 = PCIE0_TX1_P	PERST# =CRST_1V8#	50
51	GND	CLKREQ#	52
53	REFCLK- = PCIE_REFCLK2_N	PEWAKE# ➔ PU +3V3	54
55	REFCLK+ = PCIE_REFCLK2_P	MFG1	56
57	GND	MFG2	58
MECHANICAL KEY			
67	NC67	SUSCLK	68
69	PEDET	+3.3V	70
71	GND	+3.3V	72
73	GND	+3.3V	74
75	GND		

Table 6-28 M.2 M-key Pinout

The following table shows the internal connections:

ST9			MXM1			S32G274A	
Pin	Name		Pin	Signal		Pin	Name
43	*M2_TX0_P*	→	T85		←	W19	*PCIE1_TX0_P*
41	*M2_TX0_N*	→	T84		←	Y18	*PCIE1_TX0_N*
49	*M2_RX0_P*	←	T70		→	AA22	*PCIE1_RX0_P*
47	*M2_RX0_N*	←	T69		→	AB22	*PCIE1_RX0_N*

Table 6-29 M.2 M-key Slot SerDes_1_Ln0 Assignment

6.5.3 PCIe Root Complex / Endpoint

Switch SW2-3 can be used to change the configuration of the SBC-S32G274A from “Root Complex” to “Endpoint”.

Mode	Description
„Root Complex“ (standard) SW2-3 off	*The SoM is a PCIe Root Complex.* *The SBC-S32G274A drives PCIe lanes and controls reset and clock to any PCIe card plugged in ST15*
„Endpoint“ SW2-3 on	*The SoM is a PCIe Endpoint.* *The SBC-S32G274A expects to be controlled by any PCIe Root Complex connected via ST15. This includes reset, clock and PCIe lanes.*

Table 6-30 PCIe Root Complex / Endpoint

It is also necessary to adapt the software configuration of the two systems involved in the setup.

By setting the “Endpoint” mode without correct software configuration the behaviour of the SBC-S32G274A may be unpredictable.

6.6 USB

USB is using the multi-function interface MAC2 of the S32G274A processor. This is connected to USB-ULPI device USB3320 (J32).

J32 (USB3320)			MXM1			S32G274A	
Pin	Name		Pin	Signal		Pin	Name
3	*DATA[0]*	↔	T23		↔	P23	*RGMII2_TXD2/USB_D0*
4	*DATA[1]*	↔	T22		↔	L21	*RGMII2_TXD3/USB_D1*
5	*DATA[2]*	↔	T21		↔	P21	*RGMII2_RX_CLK/USB_D2*
6	*DATA[3]*	↔	T20		↔	M23	*RGMII2_RXDV/USB_D3*
7	*DATA[4]*	↔	T18		↔	N20	*RGMII2_RXD0/USB_D4*
9	*DATA[5]*	↔	T17		↔	N21	*RGMII2_RXD1/USB_D5*
10	*DATA[6]*	↔	T16		↔	M21	*RGMII2_RXD2/USB_D6*
13	*DATA[7]*	↔	T15		↔	N23	*RGMII2_RXD3/USB_D7*
29	*STP*	←	T28		←	P22	*RGMII2_TXD0/USB_STP*
2	*NXT*	→	T25		→	N22	*RGMII2_TXD1/USB_NXT*
31	*DIR*	→	T28		→	L23	*RGMII2_TX_EN/USB_DIR*
1	*CLKOUT*	→	T29		→	N19	*RGMII2_TX_CLK/USB_CLK*

Table 6-31 ULPI interface to S32G274A

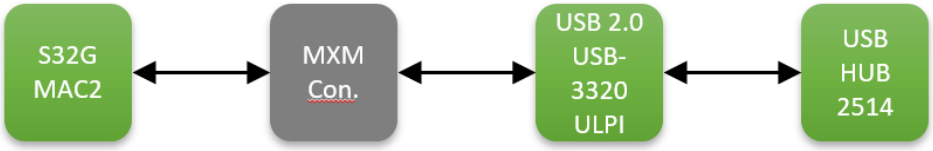


Figure 6-4 USB signal path

USB hub supports:

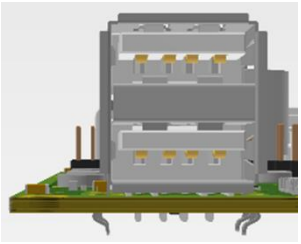
- USB1 = external interface ST14-Top
- USB2 = mini PCIe slot
- USB3 = M.2 connector (key B)
- USB4 = external interface ST14-Bottom

6.6.1 USB1, USB4 (ST14)

USB1 is available on a USB-A connector top.

USB4 is available on a USB-A connector bottom.

Part Reference:	ST14
Manufacturer:	Würth Elektronik
Type:	614 008 26 021
Used with:	Dual USB type A cables



6.6.2 USB2 (mPCIe)

USB2 from hub USB2514 is connected to mPCIe slot.

6.6.3 USB3 (M.2)

USB3 from hub USB2514 is connected to M.2 slot.

6.7 CAN, LIN, FlexRay connectors

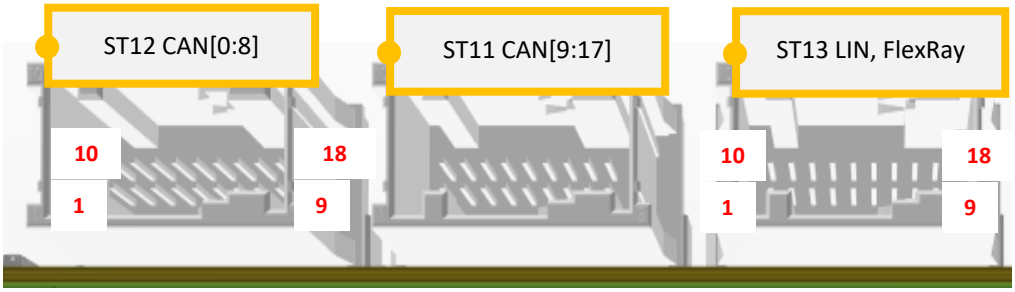


Figure 6-5 CAN, LIN, FlexRay Connectors

NOTE

CAN transceivers are set to standby by default. They are enabled during Linux boot by the Cortex-A53 cores. If the system is booted from an M7 core, the I/O expander on I2C-1 at address 0x44 must be configured to set GPIO7 high for CAN operation.

6.8 CAN (ST11, ST12)

S32G274A						Connector	
Pin	Signal		Module Pin	Transceiver		Pin	Name
G11	CAN00_TX	→	B20	TJA1448CTK	↔	ST12-1	*CAN00_N*
F15	CAN00_RX	←	B19	TJA1448CTK	↔	ST12-10	*CAN00_P*
B11	CAN01_TX	→	B23	TJA1448CTK	↔	ST12-2	*CAN01_N*
D17	CAN01_RX	←	B22	TJA1448CTK	↔	ST12-11	*CAN01_P*
D10	CAN02_TX	→	B26	TJA1448CTK	↔	ST12-3	*CAN02_N*
C15	CAN02_RX	←	B25	TJA1448CTK	↔	ST12-12	*CAN02_P*
C11	CAN03_TX	→	B29	TJA1448CTK	↔	ST12-4	*CAN03_N*
D15	CAN03_RX	←	B28	TJA1448CTK	↔	ST12-13	*CAN03_P*
D12	CAN04_TX	→	B32	TJA1448CTK	↔	ST12-5	*CAN04_N*
F16	CAN04_RX	←	B31	TJA1448CTK	↔	ST12-14	*CAN04_P*
B12	CAN05_TX	→	B35	TJA1448CTK	↔	ST12-6	*CAN05_N*
D16	CAN05_RX	←	B34	TJA1448CTK	↔	ST12-15	*CAN05_P*
E12	CAN06_TX	→	B38	TJA1448CTK	↔	ST12-7	*CAN06_N*
E16	CAN06_RX	←	B37	TJA1448CTK	↔	ST12-16	*CAN06_P*
A11	CAN07_TX	→	B41	TJA1448CTK	↔	ST12-8	*CAN07_N*
C16	CAN07_RX	←	B40	TJA1448CTK	↔	ST12-17	*CAN07_P*
A10	CAN08_TX	→	B44	TJA1448CTK	↔	ST12-9	*CAN08_N*
A15	CAN08_RX	←	B43	TJA1448CTK	↔	ST12-18	*CAN08_P*
F11	CAN09_TX	→	B47	TJA1448CTK	↔	ST11-1	*CAN09_N*
D14	CAN09_RX	←	B46	TJA1448CTK	↔	ST11-10	*CAN09_P*
E11	CAN10_TX	→	B50	TJA1448CTK	↔	ST11-2	*CAN10_N*
F14	CAN10_RX	←	B49	TJA1448CTK	↔	ST11-11	*CAN10_P*
D11	CAN11_TX	→	B53	TJA1448CTK	↔	ST11-3	*CAN11_N*
B15	CAN11_RX	←	B52	TJA1448CTK	↔	ST11-12	*CAN11_P*
C10	CAN12_TX	→	B56	TJA1463ATK	↔	ST11-4	*CAN12_N*
F13	CAN12_RX	←	B55	TJA1463ATK	↔	ST11-13	*CAN12_P*
E10	CAN13_TX	→	B59	TJA1463ATK	↔	ST11-5	*CAN13_N*
E14	CAN13_RX	←	B58	TJA1463ATK	↔	ST11-14	*CAN13_P*
A9	CAN14_TX	→	B62	TJA1463ATK	↔	ST11-6	*CAN14_N*
C14	CAN14_RX	←	B61	TJA1463ATK	↔	ST11-15	*CAN14_P*
C9	CAN15_TX	→	B65	TJA1463ATK	↔	ST11-7	*CAN15_N*
B13	CAN15_RX	←	B64	TJA1463ATK	↔	ST11-16	*CAN15_P*
G8	FXCAN2_TX	→	B100	TJA1448CTK	↔	ST11-8	*CAN16_N*
F8	FXCAN2_RX	←	B99	TJA1448CTK	↔	ST11-17	*CAN16_P*
G7	FXCAN3_TX	→	B103	TJA1448CTK	↔	ST11-9	*CAN17_N*
E6	FXCAN3_RX	←	B102	TJA1448CTK	↔	ST11-18	*CAN17_P*

Table 6-32 CAN Connector Pinout

CAN termination on the CRX-S32G carrier.

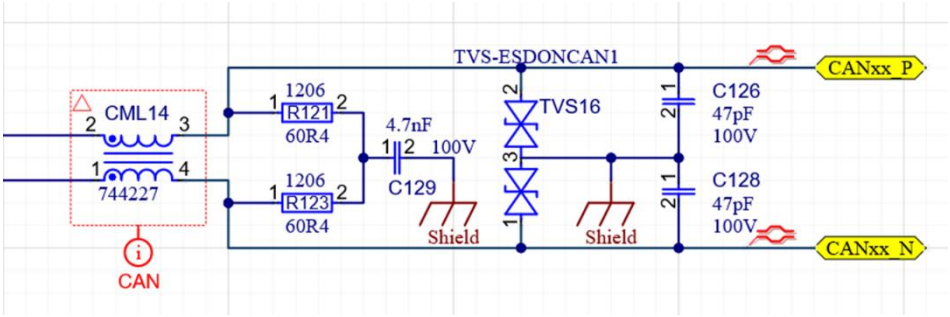


Figure 6-6 CAN Termination

NOTE

CAN termination and CAN protection are referenced to Shield

CRX-S32G-R3**V1**Ax has CAN-termination on carrier as described in above schematic.

CRX-S32G-R3**V2**Ax has **NO** CAN-Termination on carrier. Resistors (2x 60R4) are not populated.

6.9 LIN (ST13)

LIN from S32G274A

S32G274A						Connector	
Pin	**Signal**		**Module Pin**	**Transceiver**		**Pin**	**Name**
	+12V					ST13-4	*LIN_PWR0*
	LIN0_TX	→	B106	TJA1024	↔	ST13-5	*LIN0*
	LIN0_RX	←	B105				
	LIN1_TX	→	B109	TJA1024	↔	ST13-6	*LIN1*
	LIN1_RX	←	B108				
	LIN2_TX	→	B112	TJA1024	↔	ST13-7	*LIN2*
	LIN2_RX	←	B111				
	LIN3_TX	→	B115	TJA1024	↔	ST13-8	*LIN3*
	LIN3_RX	←	B114				
	GND					ST13-9	*GND*

Table 6-33 LIN Connector Pinout, Part 0

LIN from SJA1124, connected to S32G274A via DSPI5 (or SPI5)

SJA1124						Connector	
Pin	**Signal**		**Module Pin**	**Transceiver**		**Pin**	**Name**
	+12V					ST13-13	*LIN_PWR1*
				SJA1124	↔	ST13-14	*LIN4*
				SJA1124	↔	ST13-15	*LIN5*
				SJA1124	↔	ST13-16	*LIN6*
				SJA1124	↔	ST13-17	*LIN7*
	GND					ST13-18	*GND*
	S32G274A						
U10	PA09_DSPI5_SCK	→	B79	SJA1124			
E13	PA10_DSPI5_SIN	→	B80	SJA1124			
D8	PA11_DSPI5_SOUT	→	B78	SJA1124			
C7	PA12_DSPI5_CS0	→	B81	SJA1124			

Table 6-34 LIN Connector Pinout, Part 1

6.10 FlexRay (ST13)

FlexRay from S32G274A

S32G274A						Connector	
Pin	Signal		Module Pin	Transceiver		Pin	Name
A8	FLXR0A_TX	→	B92	TJA1081	↔	ST13-1	*FXRAYA_N*
A13	FLXR0A_RX	←	B91	TJA1081	↔	ST13-10	*FXRAYA_P*
C8	FLXR0B_TX	→	B96	TJA1081	↔	ST13-2	*FXRAYB_N*
D13	FLXR0B_RX	←	B95	TJA1081	↔	ST13-11	*FXRAYB _P*

Table 6-35 FlexRay Connector Pinout

All FlexRay ports are terminated on the CRX-S32G carrier:

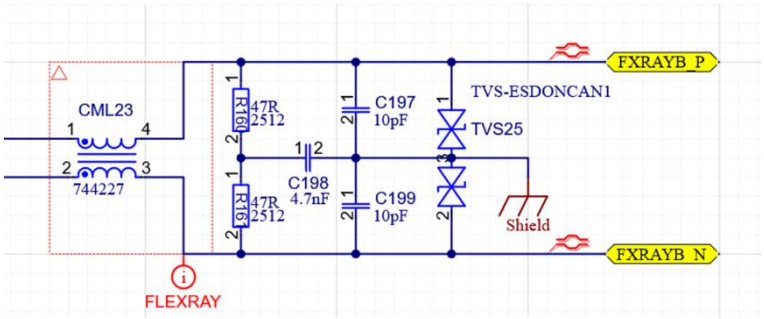


Figure 6-7 FlexRay Termination

NOTE

FlexRay termination and FlexRay protection are referenced to Shield

CRX-S32G-R3**V1**Ax has FlexRay-termination on carrier as described above.

CRX-S32G-R3**V2**Ax has **NO** FlexRay-Termination on carrier. Resistors (2x 47R) are not populated.

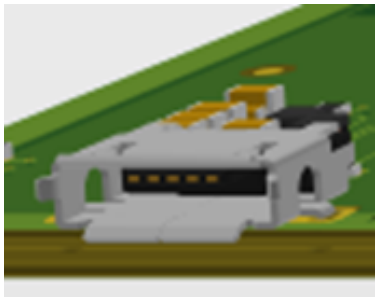
6.11 Console (ST6)

USB port ST6 is not a native USB port from the SoC, but converts the UART0 by means of an MCP2221 chip.

ST6 is available on a USB mini connector type B.

The port is used as the console of the S32G274A.

Part Reference:	ST6
Manufacturer:	Würth Elektronik
Type:	651 005 161 21
Used with:	Mini USB type B cables



The following table shows the internal connections:

ST6			MPX1			S32G274A	
Pin	**Signal**		**Pin**	**Signal**		**Pin**	**Name**
1	Vbus+		B37	PC10_UART0_RX	→	Y12	PC10_UART0_RX
2	D-	J15	B38	PC09_UART0_TX	←	U11	PC09_UART0_TX
3	D+						
4	ID						
5	GND						

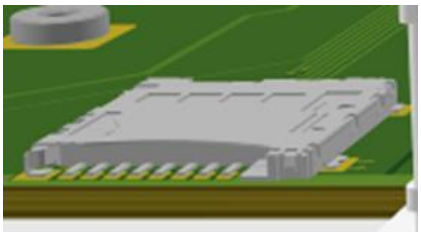
Table 6-36 USB Console pin assignment

6.12 microSD (ST5)

The SBC-S32G274A offers a microSD card slot (using push-push method).

The microSD card can also be configured as a boot device via SW2.

Part Reference:	ST5
Manufacturer:	Yamaichi
Type:	PJS-008-2130-0
Used with:	microSD cards



The following table shows the connections of the microSD card slot:

I/O Range	ST5			MXM1			S32G274A	
	Pin	Name		Pin	Signal		Pin	Name
LVTTL	1	DAT2	↔	T8	SD-D2	↔	H19	SDHC_D2
LVTTL	2	CD/DAT3	↔	T9	SD-D3	↔	H20	SDHC_D3
LVTTL	3	CMD	↔	T4	SD-CMD	↔	F21	SDHC_CMD
	4	Vdd						
LVTTL	5	CLK	←	T2	SD-CLK	←	E19	SDHC_CLK
	6	Vss						
LVTTL	7	DAT0	↔	T6	SD-D0	↔	G22	SDHC_D0
LVTTL	8	DAT1	↔	T7	SD-D1	↔	E20	SDHC_D1
LVTTL	9	SW1	→		SDC-CD#			
LVTTL	10	SW2	→					Pull down

Table 6-37 microSD card slot pin assignment

6.13 JTAG

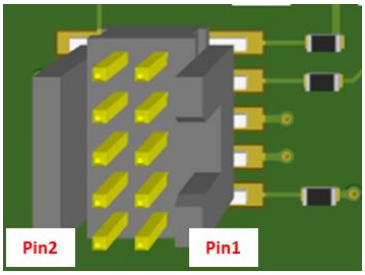
There are 2 separate JTAG ports. One for the SoM and one for the SJA1110 on the carrier.

6.13.1 JTAG for MPX-S32G274A (ST7)

The JTAG signals are available on a MIPI-10 header. This provides a direct connection to the S32G274A processor on the SoM.

Note that when debugging the processor, the JCOMP signal needs to be pulled high - meaning that DIP switch SW2-4 must be ON.

Part Reference:	ST7
Manufacturer:	Samtec
Type:	SAM-FTSH-105-01-L-DV-K



ST7			MXM1			S32G274A	
Pin	**Signal**		**Pin**	**Signal**		**Pin**	**Signal**
1	JTAG_VREF						
2	JTAG_TMS	↔	B85	JTAG_TMS	↔	U7	PA_05/TMS
3	GND						
4	JTAG_TCK	→	B82	JTAG_TCK	→	W9	PA_04/TCK
5	GND						
6	JTAG_TDO	←	B83	JTAG_TDO	←	AA7	PA_01/TDO
7	n/c		B86	JCOMP		W7	JCOMP
8	JTAG_TDI	→	B84	JTAG_TDI	→	V7	PA_00/TDI
9	GND						
10	RESET#						

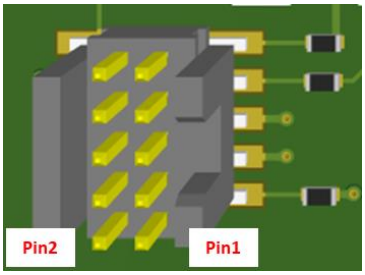
Table 6-38 JTAG Connector Pinout

6.13.2 JTAG for SJA1110 (ST10)

The JTAG signals are available on a MIPI-10 header. This TAP connects to the SJA1110 automotive switch and can be used to program the QSPI Flash connected to the SJA1110 and to debug the Cortex-M7 in the switch.

Interface uses a 1.8V logic level.

Part Reference:	ST10
Manufacturer:	Samtec
Type:	SAM-FTSH-105-01-L-DV-K



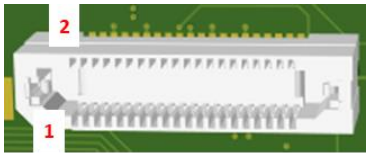
JTG2			Carrier components
Pin	**Signal**		
1	JTG2_VREF	→	1.8V
2	JTG2_TMS		J39
3	GND		
4	JTG2_TCK	→	J39
5	GND	←	
6	JTG2_TDO	→	J39
7	n/c		
8	JTG2_TDI	→	J39
9	GND	→	
10	RESET#		

Table 6-39 JTAG Connector Pinout

6.14 Aurora (ST8)

ST8 is an Aurora interface for debugging purposes - using a 40-pin connector.

Part Reference:	ST8
Manufacturer:	Samtec
Type:	ASP-130367-01



Pin:			Pin:
1	--	+3V3	2
3	--	--	4
5	GND	GND	6
7	AUR_TX2_P	--	8
9	AUR_TX2_N		10
11	GND	GND	12
13	AUR_TX0_P	--	14
15	AUR_TX0_N	--	16
17	GND	GND	18
19	AUR_CLK_P	RESET# (0R resistor)	20
21	AUR_CLK_N	--	22
23	GND	GND	24
25	AUR_TX1_P	--	26
27	AUR_TX1_N	RTCK_AURORA 10K PU (+3V3), 10k PD	28
29	GND	GND	30
31	AUR_TX3_P	--	32
33	AUR_TX3_N	--	34
35	GND	--	36
37	--	--	38
39	--	--	40

Table 6-40 Aurora Connector Pinout

The following table shows the internal connections:

ST8			MXM1			S32G274A	
Pin	Name		Pin	Signal		Pin	Name
7	AUR_TX2_P	↔	T100		↔	AC9	AUR_TX2_P
9	AUR_TX2_N	↔	T99		↔	AB9	AUR_TX2_N
13	AUR_TX0_P	↔	T103		↔	AC8	AUR_TX0_P
15	AUR_TX0_N	↔	T102		↔	AB8	AUR_TX0_N
19	AUR_CLK_P	→	T97		→	AC11	AUR_CLK_P
21	AUR_CLK_N	→	T96		→	AB11	AUR_CLK_N
25	AUR_TX1_P	↔	T106		↔	AB6	AUR_TX1_P
27	AUR_TX1_N	↔	T105		↔	AC6	AUR_TX1_N
31	AUR_TX3_P	↔	T109		↔	AB5	AUR_TX3_P
33	AUR_TX3_N	↔	T108		↔	AC5	AUR_TX3_N

Table 6-41 Aurora interconnection to Soc

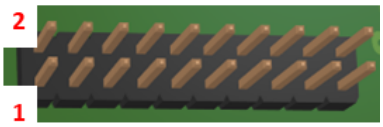
6.15 Analog In (ST1)

ST1 hosts connections to ADC inputs of the S32G274A processor.

ADCxx inputs are protected with 1k serial resistor an diode to 1.8V. That means voltage level is limited to 1.8V at cpu input.

Do not apply more than 1.8V to these inputs!!!

Part Reference:	ST1
Manufacturer:	any
Type:	HEADER-2.54-180-M-2X10 WE-6130-20-211-21



ST1			MXM1			S32G274A	
Pin	**Signal**		**Pin**	**Signal**		**Pin**	**Signal**
1	GND						
2	GND						
3	ADC_CH_00	→	B17		→	F23	ADC_CH_00
4	ADC_CH_01	→	B16		→	E22	ADC_CH_01
5	ADC_CH_02	→	B14		→	E23	ADC_CH_02
6	ADC_CH_03	→	B13		→	D22	ADC_CH_03
7	GND						
8	GND						
9	ADC_CH_04	→	B11		→	B21	ADC_CH_04
10	ADC_CH_05	→	B10		→	B22	ADC_CH_05
11	ADC_CH_06	→	B8		→	D23	ADC_CH_06
12	ADC_CH_07	→	B7		→	C22	ADC_CH_07
13	GND						
14	GND						
15	ADC_CH_08	→	B5		→	A19	ADC_CH_08
16	ADC_CH_09	→	B4		→	B20	ADC_CH_09
17	ADC_CH_10	→	B2		→	A20	ADC_CH_10
18	ADC_CH_11	→	B1		→	C21	ADC_CH_11
19	GND						
20	GND						

Table 6-42 ADC Connector Pinout

6.16 Switches

6.16.1 SW1 = Reset button

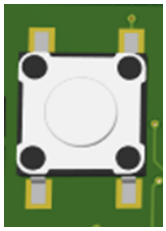


Figure 6-8 Reset Button

Pressing the reset button “SW1” triggers a Hard Reset.

The reset button is connected to J9 and triggers the RSTIN# signal on MXM1 pin “T127”.

6.16.2 SW2 = Configuration (boot selection)

The boot device can be selected by means of switch “SW2”.

Figure 6-9 Config Switch

The following configuration is supported by the SBC-S32G274A:

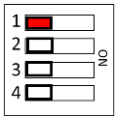
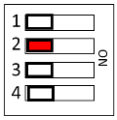
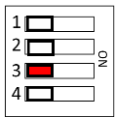
Setting	DIP Switch				Signal	Function
	4	3	2	1		
	*X*	X	X	H/L	RCW_SEL## Select between default and alternate	H: (OFF) use default RCW-EEPROM L: (ON) use alternate RCW-EEPROM
	*X*	X	H/L	*X*	MUX_SEL#	H: (OFF) boot from device on SoM L: (ON) force to boot from SD card on carrier, independent of SW setting
	*X*	H/L	X	*X*	SEL_CLK_RC/EP#	H: (OFF) RC (root complex) L: (ON) EP (endpoint)
	H/L	*X*	*X*	*X*	JCOMP	L: (OFF) JCOMP = 0 normal operation H: (ON) JCOMP = 1 allow JTAG debugging of CPU

Figure 6-10 Config Settings

SW2-1, SW2-2, SW2-3 may be controlled by software via GPIOs from debug port.

The following table shows the internal connections of the configuration pins:

SW2			MXM1			S32G274A	
Switch	Signal		Pin	Signal		Pin	Name
2-1	RCW_SEL#	→	T131		→		*Mux*
2-2	MUX_SEL#	→	T132		→		*Mux*
2-3	SEL_CLK_RC/EP#	→	T130		→		Mux
2-4	JCOMP	→	B86		→	W7	JCOMP

Table 6-43 Configuration Pin Assignment

6.16.3 SW3 = SJA1110 boot configuration

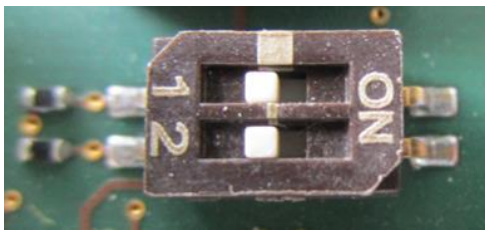


Figure 6-11 Boot Device Switch

The boot device can be selected by the switch “SW3”.

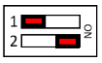
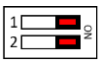
Setting	SW 3-1	SW 3-2	Boot device	Features
	OFF	OFF	Serial Download	An image is downloaded at Linux boot time.
	OFF	ON	EEPROM	Not used.
	ON	OFF	SPI Flash	Not used.
	ON	ON	QSPI Flash	Pre-programmed with an image.

Figure 6-12 SJA1110 boot settings

6.17 LEDs

6.17.1 LEDs on Carrier

There are 4 LEDs on carrier available via lightpipe on board edge next ot power connector. Organized from bottom to top: LD1, LD2, LD3, LD4

LED	Function
LD1 Green	LED ON: Power-up sequence of the module has finished, power is good LED OFF: Power fail
LD2 Red	LED ON: Any reset is active LED OFF: All resets are inactive
LD3 Green	User-LED LED1 ON: I2C addr 44 reg 5 Data 0bxxx1.xxxx LED1 OFF: I2C addr 44 reg 5 Data 0bxxx0.xxxx
LD4 Red	User-LED LED2 ON: I2C addr 44 reg 5 Data 0bxx1x.xxxx LED2 OFF: I2C addr 44 reg 5 Data 0bxx0x.xxxx

Table 6-44 Indicator LEDs – Carrier

User Leds are controlled by IO-Expander J47 (FXL6408) GPIO5, GPIO4.

I2C dev 1

I2C nm 0x44 3	0bxx11.xxxx	
I2C nm 0x44 5	0bxx00.xxxx	
I2C nm 0x44 7	0bxx11.xxxx	both LED ON
I2C nm 0x44 7	0bxx10.xxxx	red LED ON
I2C nm 0x44 7	0bxx01.xxxx	green LED ON
I2C nm 0x44 7	0bxx00.xxxx	both LED OFF

6.17.2 LEDs on Module

On the SoM there are 4 additional LEDs. For more details please refer to the MPX-S32G274A User Manual.

6.18 Test and expansion Connector (ST4)

ST4 is a 12-pin header for board testing and external I2C devices

Part Reference:	ST4
Manufacturer:	any
Type:	HEADER-2.54-180-M-2X6 WE-6130-12-211-21

Pin:			Pin:
1	VDD_OTP To module (PMIC)	+7V5 May be connected by jumper to pin 1 to force PMIC permanently into debug mode	2
3	+3V3 For measurement and external power	V_IN With 1K serial resistor For measurement only	4
5	+1V8 With 1K serial resistor For measurement only	+5V0 For measurement and external power	6
7	+1V5 With 1K serial resistor For measurement only	nc	8
9	+1V1 With 1K serial resistor For measurement only	GND	10
11	I2C2_SDA_EXT Buffered external I2C2	I2C2_SCL_EXT Buffered external I2C2	12

Table 6-45 ST4 Test Connector Pinout

+3V3 and +5V0 may be used to feed external extension boards. Boards may be controlled by I2C2 i/f.

7 Software

7.1 U-Boot

The SBC-S32G274A uses U-Boot as the standard boot loader which is always programmed into the board's QSPI Flash memory on delivery.

Additionally, U-Boot is installed on the microSD card provided with the Development Kit.

Either boot option can be selected by the Boot Configuration switch (SW2).

7.2 Operating System Support

MicroSys Electronics GmbH currently only offers Linux 5.4 for the board.

Other Operating Systems are available on request only.

If you have ordered a Development Kit, the most recent Linux release, at time of shipment, will be on the SD card, so you can start to develop and test your application right away.

In case support for interrupts shall be used in Linux (BSP33 and later) all Ethernet Phys must be configured for interrupt support and not only one. The interrupts are wired and, but the default configuration of the Phys is LED driver with push pull output. So, all Phys need to be configured for open drain. Per default polling mode is used, which does not cause any trouble.

8 Appendix

8.1 Acronyms

These acronyms are being used within the document; note that this list does not claim to be complete or exhaustive:

DC ..... *Direct Current*
ESD ..... *Electrostatic Discharge*
GND ..... *Ground*
GPL ..... *General Public License*
LAN ..... *Local Area Network*
MCU ..... *Microcontroller Unit*
SBC ..... *Single Board Computer*
SOM ..... *System On Module*
USB ..... *Universal Serial Bus*

8.2 Table of Figures

8.3 Table of Tables

9 History

Date	Version	Change Description
2020-07-07	**1.0**	Initial version for carrier CRX-S32G Revision 1
2021-04-19	**2.0**	Initial version for carrier CRX-S32G Revision 2
2021-05-21	**2.1**	6.8 Termination for CAN added 6.10 Termination for FlexRay added 6.18 ST4 pin description added
2021-07-19	**3.1**	Initial version for carrier CRX-S32G Revision 3 Differences shown in 4.5
2021-10-29	**3.2**	Updated ST23 connector type Added SIM-Card interface description
2021-12-06	**3.3**	3.3.1 added minimum power up ramp time
2022-10-20	**3.4**	6.7 added note for standby configuration
2022-11-03	**3.5**	7.2 added warning about interrupt on Phys
2023-06-27	**3.6**	Clarified Table 6-10 JTAG

Table 9-1 Document History