

miriac SBC-LS1088A-TSN

User Manual (CRX06 Revision 2)

V 2.1

Table of Contents

1	General Notes	4	5.8	I ² C Bus.....	31
1.1	Warranty.....	4	5.8.1	I2C-1.....	31
1.2	Links.....	4	5.8.2	I2C-2.....	32
1.3	Liability.....	4	6	Peripherals	34
1.4	Offer to Provide Source Code of Certain Software.....	5	6.1	Connector References.....	34
1.5	Symbols, Conventions and Abbreviations.....	6	6.2	Module Connector.....	35
1.5.1	Symbols.....	6	6.3	Serdes usage.....	35
1.5.2	Conventions.....	6	6.4	LAN Connections.....	35
2	Introduction	7	6.4.1	Possible LAN-Configurations.....	36
2.1	Safety and Handling Precautions.....	7	6.4.2	SRD1 (XFI / SGMII).....	37
2.2	Short Description.....	8	6.4.3	SRD6 (XFI / SGMII).....	37
2.3	Shipping List.....	8	6.4.4	SRD2 (QSGMII / SGMII).....	37
2.4	Functional Coverage.....	9	6.4.5	SRD3 (QSGMII / SGMII).....	38
3	Quick Start Guide	10	6.4.6	TSN 1-4 Connections.....	40
3.1	Prerequisites.....	10	6.4.7	TSN 5-8 Connections.....	41
3.1.1	Minimum Requirements.....	10	6.4.8	MDIO1 addressing.....	42
3.1.2	Recommended Items.....	10	6.4.9	MDIO2 addressing.....	42
3.2	Board Preparation and Power-Up.....	11	6.5	PCIe Connections.....	43
3.3	Operation.....	12	6.6	MicroSD Card Slot.....	46
3.3.1	U-Boot Startup.....	12	6.7	USB.....	47
3.3.2	Linux.....	14	6.7.1	USB1.....	47
4	System Description	15	6.7.2	USB2.....	48
4.1	Block Diagram.....	15	6.7.3	USB3.....	49
4.2	Feature Overview.....	15	6.8	MCU Connector.....	50
4.3	Mechanical Dimensions.....	18	6.9	JTAG 1 Connector (Processor).....	51
4.3.1	MPX-LS1088A.....	18	6.10	JTAG 2 Connector (Carrier Components) ..	52
4.3.2	SBC-LS1088A-TSN.....	19	6.11	I2C / SPI Extension (JP1).....	53
4.4	Connector Layout – Top.....	20	6.12	GPIO Extension (JP2).....	53
4.5	Power Supply.....	21	6.13	Fan Connector (PWE).....	55
4.5.1	Input Supply Rating.....	21	7	Switches, Buttons and Jumpers	56
4.5.2	Input Power Connector.....	21	7.1	Boot Device Switch.....	56
4.5.3	Power Supply Structure.....	22	7.2	Board Configuration Switch.....	57
4.5.4	RTC Backup Battery.....	22	7.3	Reset Button.....	58
4.5.5	Current Measurement.....	23	8	LEDs	59
4.5.6	Fuses.....	23	8.1	RJ45 LEDs 10Gb.....	59
5	System Core, Boot Configuration and On-Board Memory	24	8.2	RJ45 LEDs QSGMII.....	60
5.1	Processor NXP LS1088A.....	24	8.3	RJ45 LEDs TSN.....	61
5.2	JTAG Chain.....	24	8.4	Power And Reset LEDs.....	63
5.3	Reset Structure.....	24	8.5	RGB LEDs.....	64
5.4	Clock Distribution.....	26	9	Software	65
5.5	Boot Configuration.....	28	9.1	U-Boot.....	65
5.6	NAND Flash.....	29	9.2	Operating System Support.....	65
5.7	QSPI Flash.....	30	9.3	Flash Layout.....	66
			9.3.1	NAND Flash.....	66

9.3.2	SD Card	66	10.3	Table of Tables.....	68
9.3.3	QSPI Flash.....	66	11	History.....	70
10	Appendix.....	67			
10.1	Acronyms	67			
10.2	Table of Figures	68			

1 General Notes

Copyright MicroSys Electronics GmbH, January 2017

All rights reserved. All rights in any information which appears in this document belong to MicroSys Electronics GmbH or our licensors. You may copy the information in this manual for your personal, non-commercial use.

Copyrighted products are not explicitly indicated in this manual. The absence of the copyright (©) and trademark (TM or ®) symbols does not imply that a product is not protected. Additionally, registered patents and trademarks are similarly not expressly indicated in this manual.

1.1 Warranty

To the extent permissible by applicable law all information in this document is provided without warranty of any kind, whether expressed or implied, including but not limited to any implied warranty of satisfactory quality or fitness for a particular purpose, or of non-infringement of any third party's rights. We try to keep this document accurate and up-to-date but we do not make any warranty or representation about such matters. In particular we assume no liability or responsibility for any errors or omissions in this document.

MicroSys Electronics GmbH neither gives any guarantee nor accepts any liability whatsoever for consequential damages resulting from the use of this manual or its associated product.

MicroSys Electronics GmbH further reserves the right to alter the layout and/or design of the hardware without prior notification and accepts no liability for doing so.

1.2 Links

We make no warranty about any other sites that are linked to or from this document, whether we authorise such links or not.

1.3 Liability

To the extent permissible by applicable law, in no circumstance, including (but not limited to) negligence, shall we be liable for your reliance on any information in this document, nor shall we be liable for any direct, incidental, special, consequential, indirect or punitive damages nor any loss of profit that result from the use of, or the inability to use, this document or any material on any site linked to this document even if we have been advised of the possibility of such damage. In no event shall our liability to you for all damages, losses and causes of action whatsoever, whether in contract, tort (including but not limited to negligence) or otherwise exceed the amount, if any, paid by you to us for gaining access to this document.

MicroSys Electronics GmbH
Muehlweg 1
D-82054 Sauerlach
Germany

Phone: +49 8104 801-0
Fax: +49 8104 801-110

1.4 Offer to Provide Source Code of Certain Software

This product contains copyrighted software that is licensed under the General Public License (“GPL”) and under the Lesser General Public License Version (“LGPL”). The GPL and LGPL licensed code in this product is distributed without any warranty. Copies of these licenses are included in this product.

You may obtain the complete corresponding source code (as defined in the GPL) for the GPL Software, and/or the complete corresponding source code of the LGPL Software (with the complete machine-readable “work that uses the Library”) for a period of three years after our last shipment of the product including the GPL Software and/or LGPL Software, which will be no earlier than December 1, 2010, for the cost of reproduction and shipment, which is dependent on the preferred carrier and the location where you want to have it shipped to, by sending a request to:

MicroSys Electronics GmbH
Muehlweg 1
D-82054 Sauerlach
Germany

In your request please provide the product name and version for which you wish to obtain the corresponding source code and your contact details so that we can coordinate the terms and cost of shipment with you.

The source code will be distributed WITHOUT ANY WARRANTY and licensed under the same license as the corresponding binary/object code.

This offer is valid to anyone in receipt of this information.

MicroSys Electronics GmbH is eager to duly provide complete source code as required under various Free Open Source Software licenses. If however you encounter any problems in obtaining the full corresponding source code we would be much obliged if you give us a notification to the email address gpl@microsys.de, stating the product and describing the problem (please do NOT send large attachments such as source code archives etc to this email address)

1.5 Symbols, Conventions and Abbreviations

1.5.1 Symbols

Throughout this document, the following symbols will be used:



*Information marked with this symbol **MUST** be obeyed to avoid the risk of severe injury, health danger, or major destruction of the unit and its environment*



*Information marked with this symbol **MUST** be obeyed to avoid the risk of possible injury, permanent damage or malfunction of the unit.*



Information marked with this symbol gives important hints upon details of this manual, or in order to get the best use out of the product and its features.

Table 1-1 Symbols

1.5.2 Conventions

Symbol	explanation
#	denotes a low active signal
←	denotes the signal flow in the shown direction
→	denotes the signal flow in the shown direction
↔	denotes the signal flow in both directions
→	denotes the signal flow in the shown direction with additional logic / additional ICs in the signal path
I/O	denotes a bidirectional pin
Input	denotes an input pin
matched	denotes the according signal to be routed impedance controlled and length matched
Output	denotes an output pin
Pin 1	refers to the numeric pin of a component package
Pin a1	refers to the array position of a pin within a component package
XXX-	denotes the negative signal of a differential pair
XXX+	denotes the positive signal of a differential pair
XXX	denotes an optional not mounted or fitted part

Table 1-2 Conventions

2 Introduction

Thank you for choosing the MicroSys SBC-LS1088A Single Board Computer system. This manual should help you to get the best performance and details out all of its features.

2.1 Safety and Handling Precautions



ALWAYS use the correct type and polarity of the power supply!

DO NOT exceed the rated maximum values for the power supply! This may result in severe permanent damage to the unit, as well as possible serious injury.

ALWAYS keep the unit dry, clean and free of foreign objects. Otherwise, irreparable damage may occur.



Parts of the unit may become hot during operation. Take care not to touch any parts of the circuitry during operation to avoid burns, and operate the unit in a well-ventilated location. Provide an appropriate cooling solution as required.



ALWAYS take care of ESD-safe handling!

Many pins on external connectors are directly connected to the CPU or other ESD sensitive devices.

Make or break ANY connections ONLY while the unit is switched OFF.

Otherwise, permanent damage to the unit may occur, which is not covered by warranty.



There is no separate SHIELD connection.

All the metal sheaths of shielded connectors are connected to GND.

Also, all mounting holes of the carrier board are connected to GND.

The module's mounting holes are not connected to GND

Take this into account when handling and mounting the unit.

Table 2-1 Safety and Handling Precautions

2.2 Short Description

The SBC-LS1088A-TSN is a small computer system consisting of

- the MPX-LS1088A module, based on NXP's LS1088A Multicore Communications Processors
- and the CRX06 carrier board.

It targets both

- evaluation of the respective MPX-LS1088A SOM
- direct usage as an industrial computing solution

This document gives you an overview on the board's connectors and how to take the first steps on the initial setup.

2.3 Shipping List

The SBC-LS1088A-TSN EvalKit package contains the following items:

- The SBC-LS1088A-TSN system, mounted with cooling solution
- Power Supply 12V DC stabilized / 2 A
- Cable adapter for the power supply
- USB cable type A – mini B
- Micro-SD-Card with U-Boot and root file system

2.4 Functional Coverage

The following table shows the coverage achieved by the SBC-LS1088A-TSN compared to the features which are available on the carrierboard:

Interfaces provided by CRX06 carrierboard		Interfaces available with the SBC-LS1088A-TSN
SerDes 0	PCIe, port 2	✓
SerDes 1	XFI, SGMII	✓
SerDes 2	QSGMII, SGMII	✓
SerDes 3	QSGMII, SGMII	✓
SerDes 4	PCIe, port 0	✓
SerDes 5	PCIe, port 1	✓
SerDes 6	XFI, SGMII	✓
SerDes 7	PCIe, port 3	✓
RGMII 1	TSN switch	✓
RGMII 2	TSN switch	✓
USB 1	2.0 / 3.0	✓ (3.0)
USB 2	2.0 / 3.0	✓ (3.0)
SD-Card	1bit / 4 bit & boot device	✓
UART 1	UART to USB (debug console)	✓
UART 2	TTL only	✓
I ² C 1	Multiple devices	✓
I ² C 2	Multiple devices	✓
JTAG	Signals on non-standard connector	✓
Watchdog	Hardware watchdog with trigger signal from module	✓
RTC backup	Battery	✓
Manual Reset	Button	✓
Reset / Power LEDs	2x red, 1x green	✓
User LEDs	4x RGB	✓

Table 2-2 Functional coverage

3 Quick Start Guide

3.1 Prerequisites



Always make sure to handle the SBC-LS1088A-TSN unit ESD-safe! Otherwise, the unit may suffer permanent damage. However, do not place the unit directly flat on a metal surface, as this may result in short circuits and damage to the board.

At first time operation unpack the unit and make sure that is clean and free of visible damage or foreign objects.

3.1.1 Minimum Requirements

To operate the board, you will at least need the following items:

- an adequate power supply, delivering 12V DC (stabilized) / 2A minimum.
- an USB cable (type A – mini B) adapted to connector ST5
- a serial terminal, such as a PC with an USB port running a terminal Software (e.g. TeraTerm, HyperTerminal, putty, ckermit...), or else a hardware serial console. **Choose the following parameters:**
 - (a) **115200 Bd**
 - (b) **8 Data bits**
 - (c) **No parity**
 - (d) **1 Stop Bit**

3.1.2 Recommended Items

The following items are not absolutely necessary, but strongly recommended for practical operation and development purposes:

- Network connection to your local network installation
- TFTP server available for downloading within the network (Hint: may run on the same PC as the serial Terminal)
- SD card as mass storage and/or boot media

3.2 Board Preparation and Power-Up

- Make sure the switches SW1 and SW2 are set properly in order to select the correct boot source and board configuration
- The board comes preconfigured to boot correctly on arrival.
- Connect the mini USB cable to ST5.
- Connect other peripherals (USB, LAN ...) as far as intended.
- Connect the power line to the PWR connector, while the power supply is still switched off.
- Switch on power.

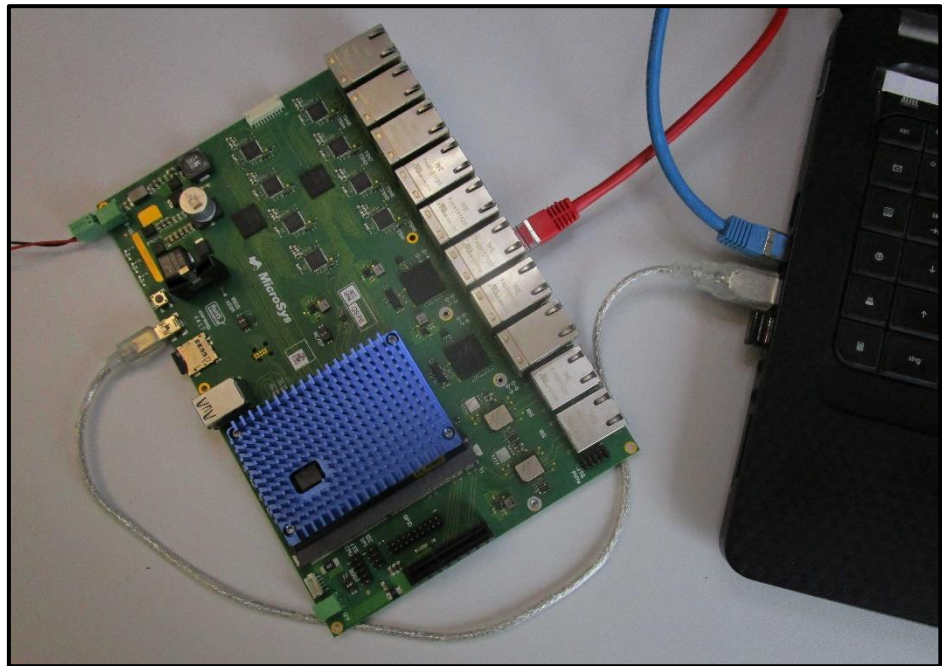


Figure 3-1 System setup example

3.3 Operation



After Power-up, the green LED on the module should light up and any red LED should be off.
IF NOT, DISCONNECT THE UNIT FROM POWER AND CHECK FOR FAULTS!

3.3.1 U-Boot Startup

When power is supplied the system will start.

On startup, U-Boot will come up similar to the following:



The exact output may vary, depending on U-Boot and MPX-LS1088A module versions in use.

```
U-Boot SPL 2019.04 (Jul 16 2019 - 11:01:22 +0200)
Initializing DDR...
Address hashing enabled.
Trying to boot from MMC1
```

```
U-Boot 2019.04 (Jul 16 2019 - 11:01:22 +0200)
```

```
SoC: LS1088AE Rev1.0 (0x87030010)
```

```
Clock Configuration:
```

```
  CPU0(A53):1600 MHz CPU1(A53):1600 MHz CPU2(A53):1600 MHz
```

```
  CPU3(A53):1600 MHz CPU4(A53):1600 MHz CPU5(A53):1600 MHz
```

```
  CPU6(A53):1600 MHz CPU7(A53):1600 MHz
```

```
  Bus: 600 MHz DDR: 2100 MT/s
```

```
Reset Configuration Word (RCW):
```

```
  00000000: 40005418 00000040 00000000 00000000
```

```
  00000010: 00000000 000a0000 00300000 00000000
```

```
  00000020: 03c01140 00002580 00000000 00000040
```

```
  00000030: 01800054 00000000 00000083 00000000
```

```
  00000040: 00000000 00000000 00000000 00000000
```

```
  00000050: 00000000 00000000 00000000 00000000
```

```
  00000060: 00000000 00000000 00000000 000009e7
```

```
  00000070: 34110000 00008888
```

```
I2C: ready
```

```
DRAM: Initializing DDR...
```

```
Detected UDIMM Fixed DDR on board
```

```
3.9 GiB
```

```
DDR 3.9 GiB (DDR4, 64-bit, CL=15, ECC on)
```

```
SEC0: RNG instantiated
```

```
FSL_SDHC: 0
```

```
PPA Firmware: Version LSDK-18.09
```

```
Using SERDES1 Protocol: 25 (0x19)
```

```
Using SERDES2 Protocol: 12 (0xc)
```

```
NAND: 512 MiB
```

```

MMC: Loading Environment from MMC... OK
EEPROM: NXID v1
In: serial
Out: serial
Err: serial
Model: MicroSys MPXLS1088
Board: MPXLS1088, SD card
PORSR1: 0x207f4f7f RCW_SRC: 0x0040
GPIO2_7: SGMII3
GPIO2_16: QSGMII2
GPIO2: 0x00000000
Net:
FSL_MDIO1 PHY@11: Revision 0x1a 11 1/1:
#####
#####
#####
FSL_MDIO1 PHY@11: Firmware version: 0.3.4.0

FSL_MDIO1 PHY@10: Revision 0x1a 11 1/1:
#####
#####
#####
FSL_MDIO1 PHY@10: Firmware version: 0.3.4.0
PCIe0: pcie@3400000 Root Complex: no link
PCIe1: pcie@3500000 disabled
PCIe2: pcie@3600000 disabled
DPMAC1@xgmii [PRIME], DPMAC2@xgmii, DPMAC3@sgmii, DPMAC4@rgmii-
id, DPMAC5@rgmii-id, DPMAC7@qsgmii, DPMAC8@qsgmii, DPMAC9@qsgmii,
DPMAC10@qsgmii
Device: FSL_SDHC
Manufacturer ID: 74
OEM: 4a60
Name: USD
Bus Speed: 25000000
Mode : SD Legacy
Rd Block Len: 512
SD version 3.0
High Capacity: Yes
Capacity: 3.7 GiB
Bus Width: 4-bit
Erase Group Size: 512 Bytes

MMC read: dev # 0, block # 20480, count 2048 ... 2048 blocks read: OK

MMC read: dev # 0, block # 26624, count 8192 ... 8192 blocks read: OK

MMC read: dev # 0, block # 28672, count 8192 ... 8192 blocks read: OK
crc32+
fsl-mc: Booting Management Complex ... SUCCESS
fsl-mc: Management Complex booted (version: 10.16.2, boot status: 0x1)
Hit any key to stop autoboot: 0
=>
    
```

3.3.2 Linux

For detailed setup instructions, refer to the text document "linux-fsl-sdk-v2.0-1703-mpxls1088.txt" delivered in the "Linux" directory along with the unit!



The text document mentioned here may refer to an older version.

4 System Description

This section describes all parts of the SBC-LS1088A-TSN system.

4.1 Block Diagram

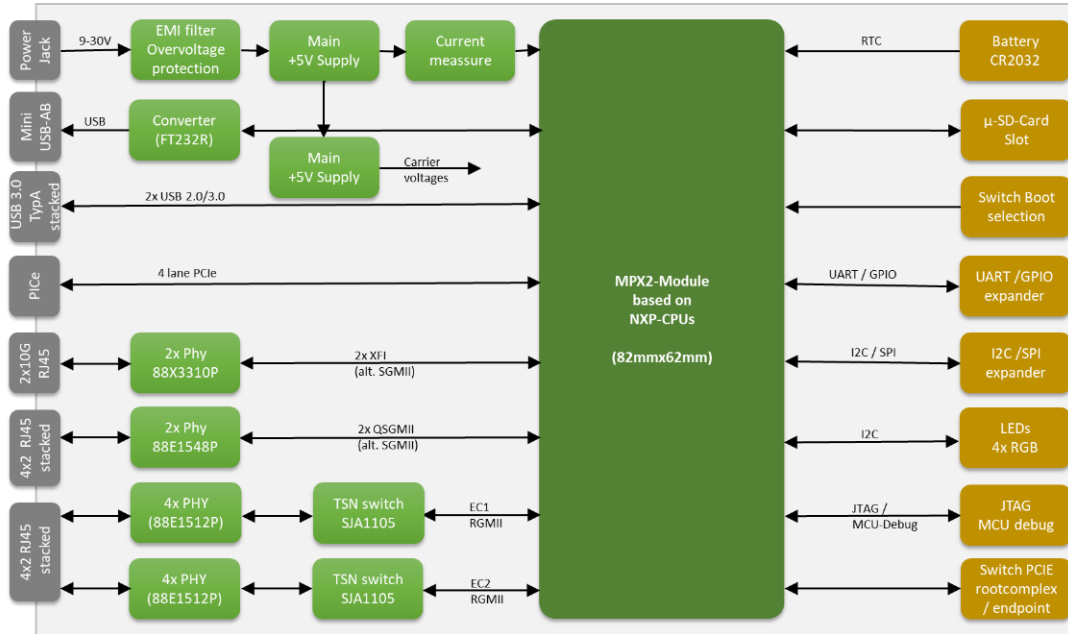


Figure 4-1 Block Diagram (MPX-LS1088A Revision 2 on carrier CRX06 Revision 2)

4.2 Feature Overview

The SBC-LS1088A-TSN offers the following features:

QorIQ ARM Cortex A72 cores 4xCPU Processor		
SDRAM	64-bit DDR4 interface	Default: 2GByte up to 4GByte up to 2100MT/s 4 x DDR4 (x16) single bank
Synchronous Memory	8-bit NAND Flash	Default: 512 MB up to 2 GByte
PCI Express port	3.0 / 8Gbps Lane x4 Root complex operations Serdes 4, 5, 0, 7	PCIe connector
USB	USB 3.0 Phy	USB connector type A
	USB 3.0 Phy	USB connector type A

QorIQ ARM Cortex A72 cores 4xCPU Processor		
Serial Interfaces	UART1	Converted to USB (FT232), Available on USB connector type mini B
	UART2	4-wire Extension Port LVTTTL
I2C	I2C-1	400 kbps
		Connected Devices: TMP451AIDQF Temperature Sensor 2x BR24G128NUX-3 EEPROM RX-8803 RTC IDT6V49205B Clock Generator TLC59116 RGB LED Driver
	I2C-2	400 kbps
		Connected Devices: SC18IS602BIPW I2C-to-SPI Bridge MAX9611AUB Current monitor PCA9517ADP I ² C Buffer
10G Ethernet Controller	Serdes 1: XFI, SGMII	10Gbps 10/100/1000 Mbps
	Serdes 6: XFI, SGMII	10Gbps 10/100/1000 Mbps
Gigabit Ethernet Controller	Serdes 2: QSGMII, SGMII	10/100/1000 Mbps
		10/100/1000 Mbps
		10/100/1000 Mbps
		10/100/1000 Mbps
Gigabit Ethernet Controller	Serdes 3: QSGMII, SGMII	10/100/1000 Mbps
		10/100/1000 Mbps
		10/100/1000 Mbps
		10/100/1000 Mbps
TSN Switch 1	RGMII 1	10/100/1000 Mbps
		10/100/1000 Mbps
		10/100/1000 Mbps
		10/100/1000 Mbps
TSN Switch 2	RGMII 2	10/100/1000 Mbps
		10/100/1000 Mbps
		10/100/1000 Mbps

QorIQ ARM Cortex A72 cores 4xCPU Processor		
		10/100/1000 Mbps
System JTAG Controller	JTAG	10 pin header
Power Management	Primary Supply	LM25116MH Input: 9-30V DC Output: 5V DC / peak 8A
	Backup Supply (RTC backup)	Battery CR2032

Table 4-1 Feature Overview

4.3 Mechanical Dimensions

4.3.1 MPX-LS1088A

The following drawing shows the mechanical outline of the MPX-LS1088A module that is plugged in the CRX06 carrier board.



This drawing is not to scale.



For 3D data files please contact MicroSys.

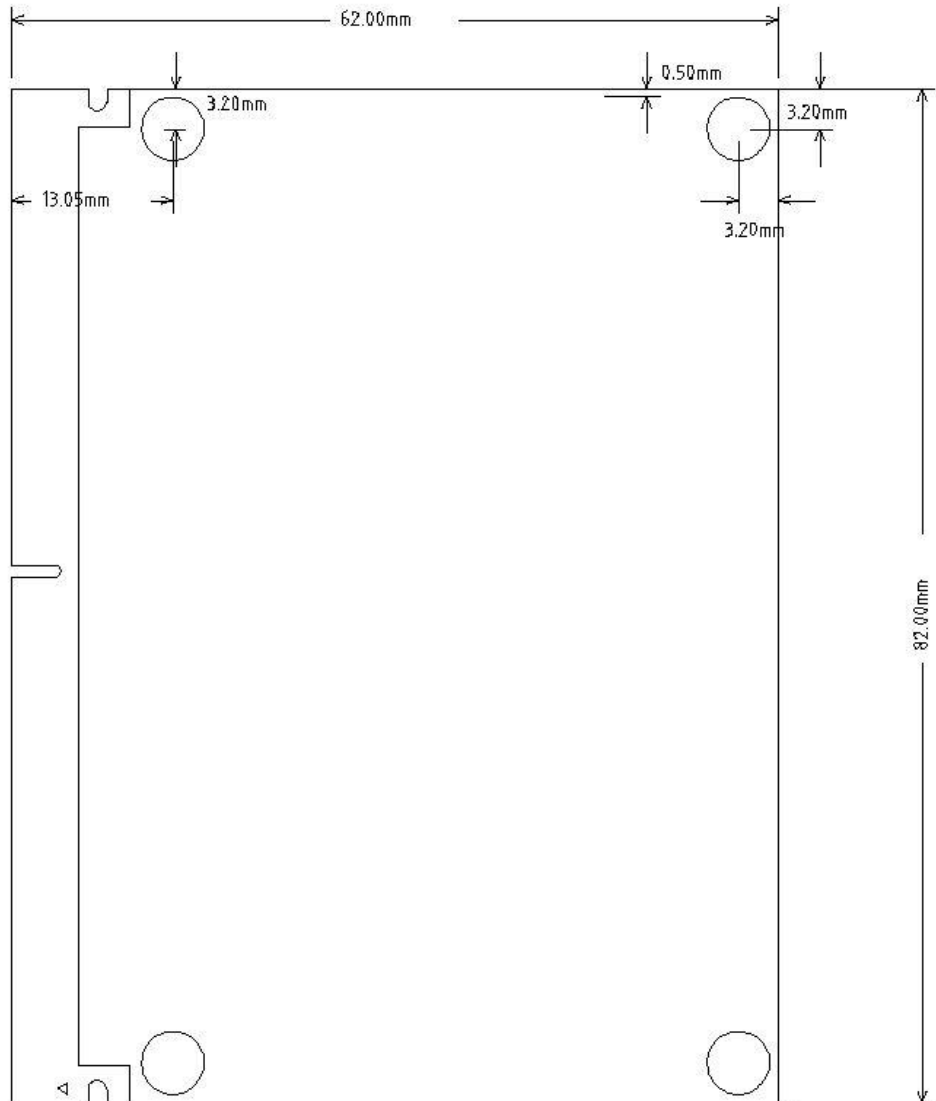


Figure 4-2 Mechanical Dimensions Module

4.3.2 SBC-LS1088A-TSN

The following drawing shows the mechanical outline of the SBC-LS1088A-TSN assembly.



This drawing is not to scale.

For 3D data files please contact MicroSys.

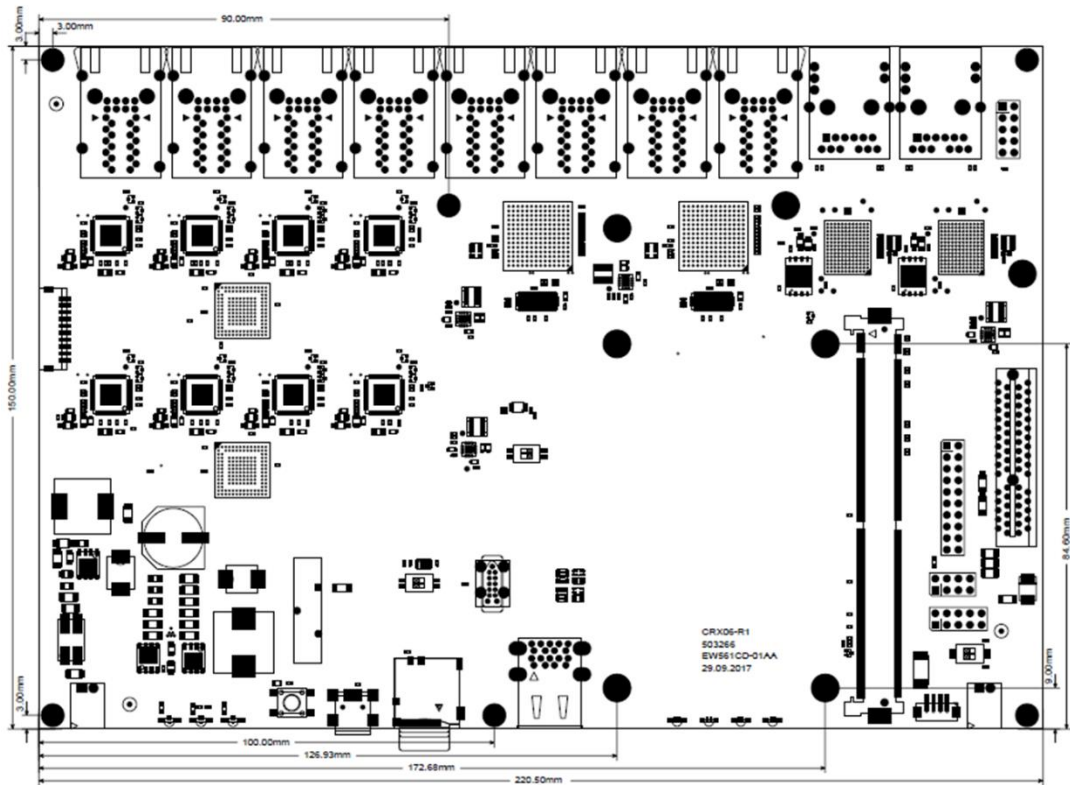


Figure 4-3 CRX06 Mechanical Dimensions

4.4 Connector Layout – Top

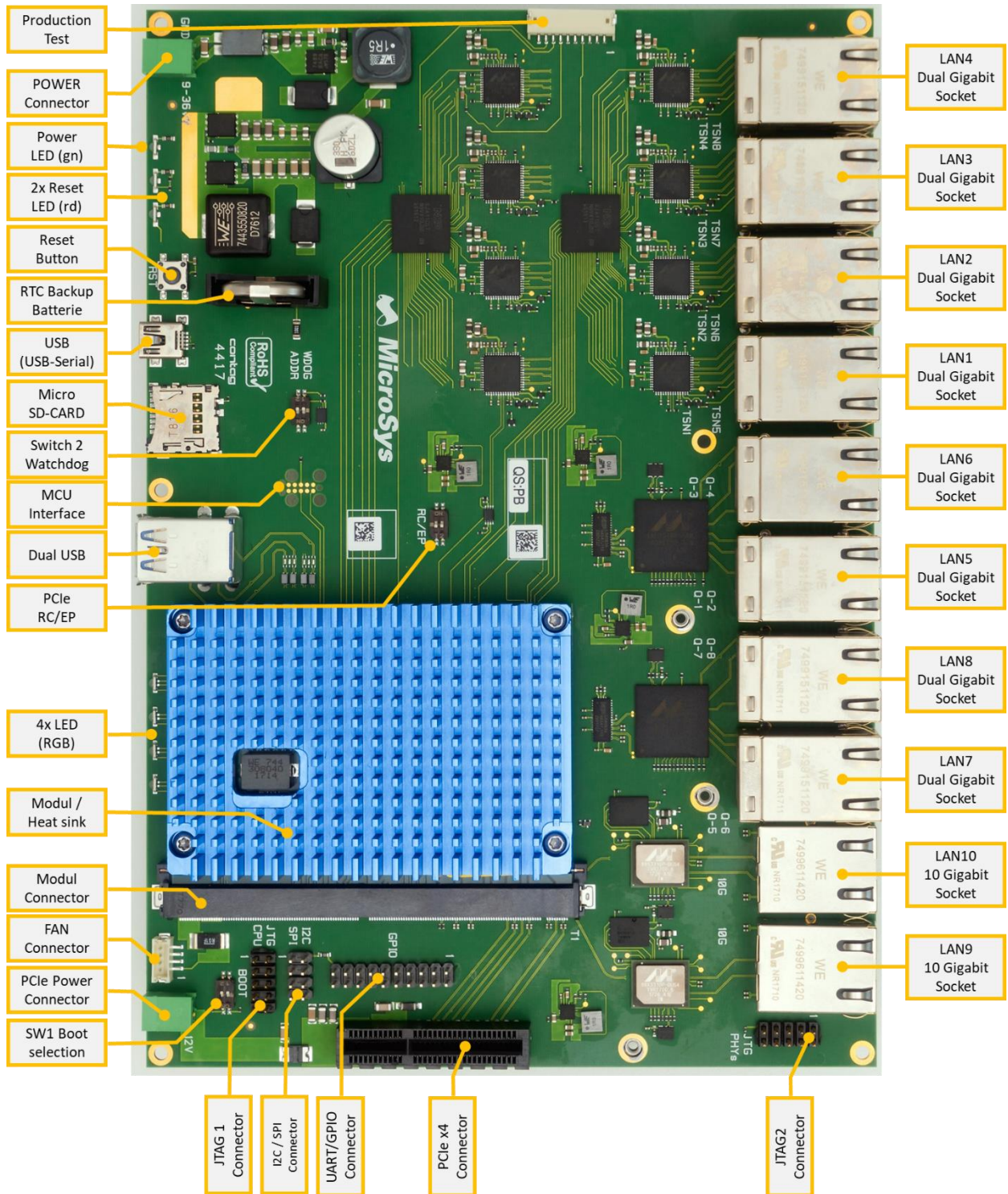


Figure 4-4 Top connectors

4.5 Power Supply

4.5.1 Input Supply Rating

The SBC-LS1088A-TSN system is run from a single DC power supply with the following ratings:

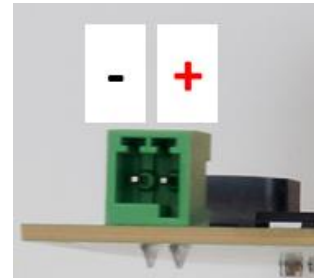
Maximum Input Voltage Operating Range:	9V - 30V DC
Nominal Input Supply Voltage:	12V DC
Typical Current Consumption (@12V / room temperature / U-boot prompt):	~1,50A



**ALWAYS use the correct type and polarity of the power supply!
DO NOT exceed the rated maximum values for the power supply! This may result in severe permanent damage to the unit, as well as possible serious injury.**

4.5.2 Input Power Connector

Part Reference	PWR
Manufacturer:	Würth Elektronik
Type:	691 382 010 002
Mates with:	691 381 000 002 (included in delivery)



Pin-out:

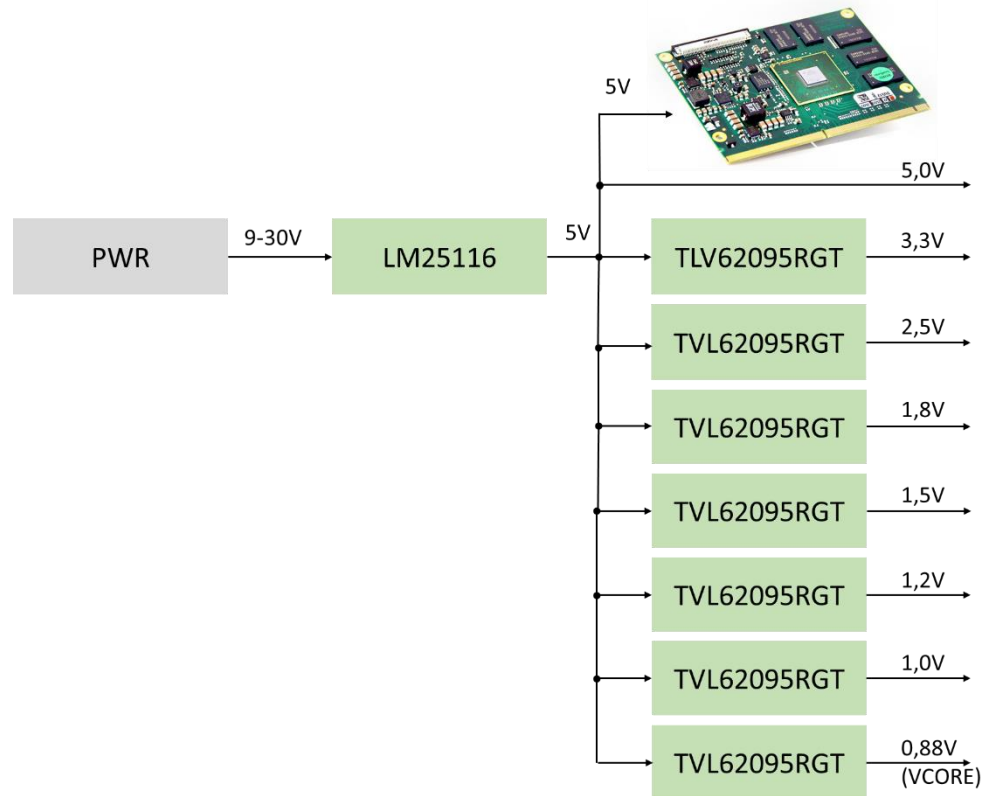
Pin	Name	Function
1	„-“	GND
2	„+“	+VIN (= typ. 12V)

Table 4-1 Pinout PWR

4.5.3 Power Supply Structure

- Input Power from PWR connector is fed to the primary step-down converter.
- The primary step-down converter produces 5V DC / max. 8A peak from the input supply which supplies both the LS1088A module and peripheral devices on the carrierboard CRX06.
- The 5V DC are fed to 7 secondary step-down converter in parallel, which produces 3.3V, 2.5V, 1.8V, 1.5V, 1.2V, 1.0V, 0.88V DC / max. 4A peak each.

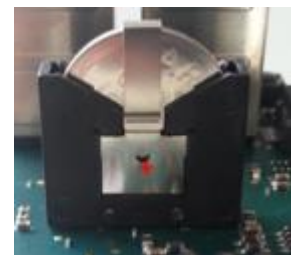
The following diagram shows the Power Supply structure:



4.5.4 RTC Backup Battery

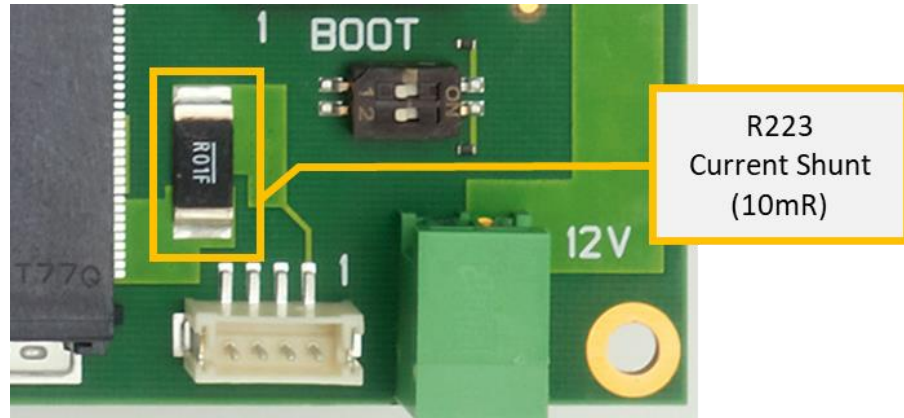
The RTC on the module is supplied from replaceable CR2032 battery.

Part Reference:	BAT1
Manufacturer:	Renata Batteries
Type:	VBH2032-1
Used with:	CR2032 battery



4.5.5 Current Measurement

For current measurements the carrierboard provides a 10m Ω shunt resistor in the 5V path supplying the CPU module.



For automated measurements there's a MAX9611AUB current sense amplifier. It is interfaced by I²C.

4.5.6 Fuses

There are no fuses on the SBC-LS1088A-TSN.

5 System Core, Boot Configuration and On-Board Memory

5.1 Processor NXP LS1088A

The LS1088A Processor by NXP is a QorIQ Layerscape CPU with four CPU cores. It exposes a wide variety of external interfaces, which are explained in detail in the following chapters. The cores have an unified L2 Cache.

The four CPU cores run at a maximum clock speed of 1800 MHz, 1600 MHz, 1400 MHz or 1200 MHz respectively, depending on the ordered type. The CPU frequency can be clocked down if necessary.

5.2 JTAG Chain

The JTAG chain of the SBC-LS1088A-TSN includes the LS1088A processor only. The JTAG port is directly connected to the connector “JTG1”.

The JTAG connector footprint provides JTAG signals. For interfacing standard debugger pinouts an additional intermediate adapter is necessary.

Please see chapter 0 for a description of the JTAG connector.

5.3 Reset Structure

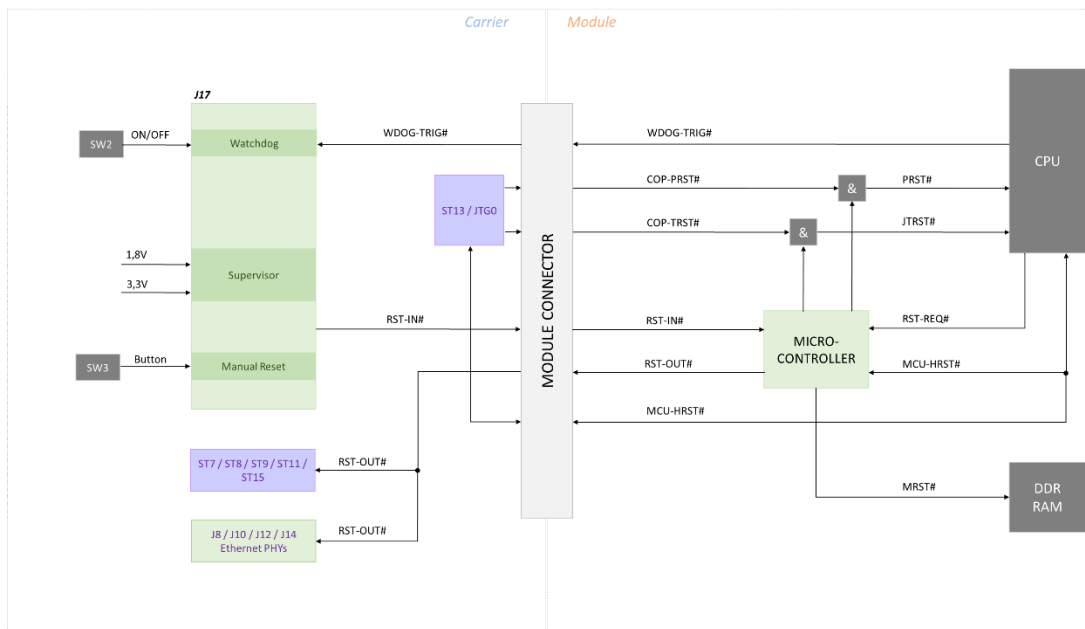


Figure 5-1 Reset Structure (carrier CRX06 Revision 2)

Pin Number on ST4	Signal Name	Signal Direction	Function
T136	RST-IN#	Input to the module	Active low module reset: while active the module is held in reset state
T135	RST-OUT#	Output from the module	Active low peripheral reset: while active peripheral devices shall be held in reset state
B118	WDOG-TRIG#	Output from the module	Watchdog service signal from the module which has to be triggered periodically. When the watchdog is active and the service stops the module will be reset.
B111	MCU-HRST#	Bi-directional	Please contact MicroSys
B110	COP-PRST#	Input to the module	Please contact MicroSys
B106	COP-TRST#	Input to the module	Please contact MicroSys

Table 5-1 Reset signal overview



The default state for RST-IN# is active. Consequently the module is always in a reset state when the RST-IN# signal is not actively driven high by the carrierboard.

The RST-IN# is an input to the module. It signals voltage supplies on the carrierboard are within their limits and no manual reset is triggered. When active (signal is low) the microcontroller unit on the module initiates the reset sequence in order to keep the CPU in a defined reset state. No further interaction from the carrierboard is necessary. In case the module reset is active, the module triggers the RST-OUT# signal which is intended to control the reset of peripheral devices on the carrierboard i.e. Ethernet PHYs, PCIe slots and devices.

The RST-IN# signal can be triggered by either a powerfault situation, a manual reset button press (SW3) or a missing watchdog trigger signal WDOG-TRIG# from the CPU in case the watchdog has been manually enabled beforehand via SW2.

MCU-HRST#, COP-PRST# and COP-TRST# are for JTAG and debugging purposes only.



**The watchdog is off by default.
The watchdog is implemented on the carrier board.**

The following voltages on the carrier board are monitored by a Maxim MAX6751KA29 chip:

Voltage	Monitoring	Voltage Limit
3,3V	Undervoltage	Typ. 2,925V [2,867V-2,984V]
1,8V	Undervoltage	Typ. 1,72V [1,69V-1,75V]

Table 5-2 Voltage monitoring limits (carrier)

5.4 Clock Distribution

The following diagram shows the clock distribution of the SBC-LS1088A-TSN system



IDT6V49205B		LS1088A	
Pin	Name	Name	Pin
23	PCleT_LR0	SD1-REFCLK1	AA8
24	PCleC_LR0	SD1-REFCLK1#	AB8
26	PCleT_LR1	SD1-REFCLK2	AB18
25	PCleC_LR1	SD1-REFCLK2#	AB19

		ST4		PCIE	
		Signal	Pin		
36	PCleT_LR4	SRD-CLK1+	T50	PCIE-CLK+	A13
35	PCleC_LR4	SRD-CLK1-	T51	PCIE-CLK-	A14

Table 5-3 Clock distribution

5.5 Boot Configuration

The SBC-LS1088A-TSN board offers three possible boot devices to choose from. The settings can be done via SW1 (see chapter 7 for details). SW1 configures two signals “BOOT-SEL1” and “BOOT-SEL2” which have a default high state (10k pullups are on the module) when no connection is made or SW1 is off. When the switch is on, the respective pin is grounded.

The BOOT-SELx pins are decoded to the following configuration (1= high, 0=low):

LS1088A		BOOT-SEL2 BOOT-SEL1 =		
Signal	Pin	SDHC =[10]	SPI =[11]	NAND =[01]
IFC_AD08	B9	0	0	1
IFC_AD09	A9	0	0	0
IFC_AD10	A10	1	1	0
IFC_AD11	B11	0	0	0
IFC_AD12	A11	0	0	0
IFC_AD13	B12	0	0	0
IFC_AD14	A12	0	1	1
IFC_AD15	A13	0	0	1
IFC_CLE	F16	0	1	1

Table 5-4 Hard wired boot signals

5.6 NAND Flash

The SBC-LS1088A-TSN system is equipped with 2GB of NAND Flash by default. Different sizes may be available on request/order. The following table shows the connections and signal levels for the NAND Flash.

I/O Range	NAND Flash		SBC-LS1088A-TSN Signal	LS1088A		Description
	Pin	Name		Pin	Name	
1,8V	G5	LOCK				Lock
1,8V	C8	RY/BY	→ IFC-RB0#	→ C16	IFC_RB0#	ready/busy, 4,7K pullup
1,8V	D4	RE#	← IFC-OE#	← C18	IFC_OE#	read enable
1,8V	C6	CE#	← IFC-CS0#	← C17	IFC_CS0#	chip select
1,8V	D3,G4,H8, J6	VCC	+1.8V			
	C5,F7,K3, K8	GND	GND			
1,8V	D5	CLE	← IFC-CLE	← C19	IFC_CLE	command latch enable
1,8V	C4	ALE	← IFC-AVD	← A18	IFC_AVD	address latch enable
1,8V	C7	WE#	← IFC-WE#	← C15	IFC_WE0#	write enable
1,8V	C3	WP#	← IFC-WP#	← D19	IFC_WP0#	write protect
1,8V	H4	D0	↔ IFC-AD7	↔ B12	IFC_AD7	data line
1,8V	J4	D1	↔ IFC-AD6	↔ A11	IFC_AD6	data line
1,8V	K4	D2	↔ IFC-AD5	↔ B11	IFC_AD5	data line
1,8V	K5	D3	↔ IFC-AD4	↔ A10	IFC_AD4	data line
1,8V	K6	D4	↔ IFC-AD3	↔ A9	IFC_AD3	data line
1,8V	J7	D5	↔ IFC-AD2	↔ B9	IFC_AD2	data line
1,8V	K7	D6	↔ IFC-AD1	↔ A8	IFC_AD1	data line
1,8V	J8	D7	↔ IFC-AD0	↔ B8	IFC_AD0	data line
	G3	n.c.				Not connect
	G8	n.c.				Not connect

Table 5-5 NAND Flash pin assignments

5.7 QSPI Flash

The SBC-LS1088A-TSN system is equipped with 16MB of QSPI Flash on the LS1088A's QSPI port. Up to 64 MB are available on request/order.

The following table shows the internal connections:

I/O Range	QSPI Flash MT25QU128ABA8E12			LS1088A	
	Pin	Name		Pin	Name
LVTTL	C2	CS	←	D8	QSPI_A_CS0
LVTTL	B2	CLK	←	C9	QSPI_A_SCK
	B3	GND	←		
LVTTL	D3	D0	↔	D11	QSPI_A_DATA0
LVTTL	D2	D1	↔	C12	QSPI_A_DATA1
LVTTL	C4	D2	↔	D13	QSPI_A_DATA2
LVTTL	D4	D3	↔	C13	QSPI_A_DATA3
	B4	+1.8V			

Table 5-6 QSPI Flash pin assignment

5.8 I²C Bus

The SBC-LS1088A-TSN offers two independent I²C busses.

The following tables show the I²C addresses as 7 Bit addresses. The R/W bit is not displayed.

5.8.1 I²C-1

I²C Bus 1 (7-Bit address):

Address	Device	Function
0x32	RX-8803LC	RTC
0x4C	TMP451AIDQF	Temperature sensor
0x50	BR24G128NUX-3	EEPROM (on module)
0x57 / (0x55) Selectable via SW2 (see 7.2)	BR24G128NUX-3	EEPROM (on carrier)
0x60	TLC59116IRHBR	RGB LED Driver Slave Address
0x68		All Call Address (must be disabled!)
0x6B		Software Reset Address
0x69	IDT6V49205BNLGI	Clock Generator

Table 5-7 I²C1 bus map



I²C address 0x68 is existing twice on I²C-1 bus.

Therefore, the so-called “All Call I²C address” of the TLC59116IRHBR RGB LED driver has to be disabled before GP input pins of the MAX7325 port expander can be read correctly. This can be achieved by setting the default value 1 of Bit 0 in MODE1 register to 0.

The I²C Bus 1 has the following layout:

I/O Range: LVTTTL

Device	SCL (Signal Name)	Pin	SDA (Signal Name)	Pin
LS1088A	IIC1_SCL	N1	IIC1_SDA	M1
	↓		↑	
RX-8803LC	SCL	5	SDA	8
	↓		↑	
BR24G128NUX-3	SCL	6	SDA	5
	↓		↑	
TMP451AIDQF	SCK	8	SDA	7
	↓		↑	
IDT6V49205B	SCLK	46	SDATA	47
	↓		↑	
Module Connector	I2C1_SCL	B78	I2C1_SDA	B77
	↓		↑	
MAX7325	SCL	19	SDA	20
	↓		↑	
BR24G128NUX-3	SCL	6	SDA	5
	↓		↑	
TLC59116IRHBR	SCL	25	SDA	26

Table 5-8 I²C-1 pin assignment

5.8.2 I²C-2

I²C Bus 2 (7-Bit address):

Address	Device	Function
no	PCA9517ADP	I2C buffer for external busses
0x7F	MAX9611AUB	Current Monitor for module consumption

Table 5-9 I²C2 bus map



I²C-2 is not available when SD-card boot mode is selected!

The I²C bus 2 has the following layout:

I/O Range: LVTTTL

Device	SCL (Signal Name)	Pin	SDA (Signal Name)	Pin
LS1088A	IIC2_SCL	K3	IIC2_SDA	L3
	↓		↑	
Module Connector	I2C2_SCL	B75	I2C2_SDA	B74
	↓		↑	
MAX9611AUB	SCL	6	SDA	7
	↓		↑	
PCA9517ADP	SCL	2	SDA	3

Table 5-10 I²C-2 pin assignment

6 Peripherals

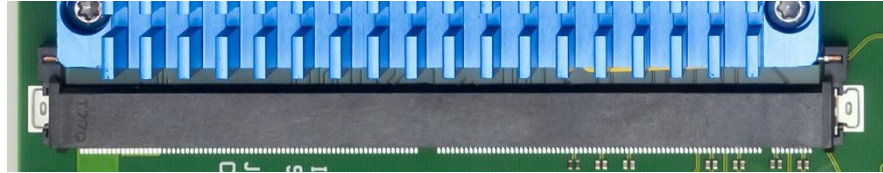
6.1 Connector References

Reference	Function	Populated?	Top / Bottom
ST1	Micro SD slot	✓	Top
ST2	Production test only	✓	Top
ST4	CPU Module Connector	✓	Top
ST5	USB to serial connector	✓	Top
ST6	Dual USB connector	✓	Top
PWR	Power connector	✓	Top
PWE	Fan connector	✓	Top
PCIPWR	Power connector +12V PCI	✓	Top
PCIE	PCIe extension connector	✓	Top
JP1	I2C / SPI extension	✓	Top
JP2	GPIO extension	✓	Top
JTG1	JTAG connector	✓	Top
JTG2	JTAG connector	✓	Top
MCU	Microcontroller	TAG connect	Top
LAN1	RJ45 connector TSN	✓	Top
LAN2	RJ45 connector TSN	✓	Top
LAN3	RJ45 connector TSN	✓	Top
LAN4	RJ45 connector TSN	✓	Top
LAN5	RJ45 connector 1G	✓	Top
LAN6	RJ45 connector 1G	✓	Top
LAN7	RJ45 connector 1G	✓	Top
LAN8	RJ45 connector 1G	✓	Top
LAN9	RJ45 connector 10G	✓	Top
LAN10	RJ45 connector 10G	✓	Top

Table 6-1 Connector reference overview

6.2 Module Connector

The carrierboard CRX06 provides a connector “ST4” which accepts compatible CPU modules from the MicroSys MPX2-family.



Manufacturer:	JAE
Type:	MM70-314-310-B1-1-R300
Used with:	MicroSys MPX2 module family

6.3 Serdes usage

Serdes names reference to connector names. Some differ from numbering at processor.

Connector	LS1088A	usage
SRD0	SD2-2	PCIe x4, port 2 to PCIe connector
SRD1	SD1-0	XFI, SGMII
SRD2	SD1-3	QSGMII, SGMII
SRD3	SD1-2	QSGMII, SGMII
SRD4	SD2-0	PCIe x4, port 0 to PCIe connector
SRD5	SD2-1	PCIe x4, port 0 to PCIe connector
SRD6	SD1-1	XFI, SGMII
SRD7	SD2-3	PCIe x4, port 3 to PCIe connector

Table 6-2 LAN / DTSEC / SerDes / usage

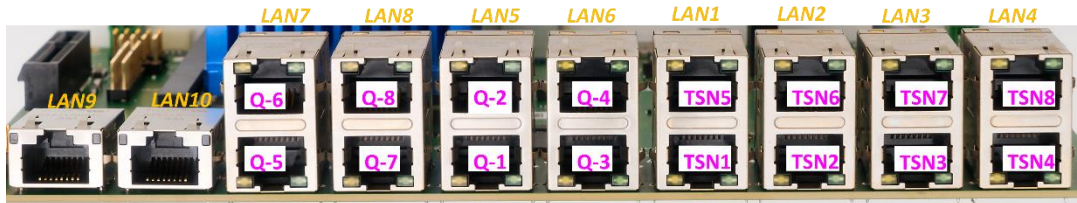
6.4 LAN Connections

The SBC-LS1088A-TSN system offers:

- 2 independent 10 Gigabit LAN connections (depending on processor and configuration). If 10Gb is no available or not configured, port may be used as 1Gb interface.
- 8 independent 1Gb LAN connections (depending on availability of QSGMII on processor module).
- 8 independent 1Gb TSN connections. These three ports are distributed over four connectors named “LAN1” to “LAN4”. The connectors have integrated magnetics.

The following picture shows the view of the LAN connectors as placed on the CRX06 baseboard. For further information on the LEDs please see chapter 8

LAN9	LAN10	LAN7	LAN8	LAN5	LAN6	LAN1	LAN2	LAN3	LAN4
		Q-6	Q-8	Q-2	Q-4	TSN5	TSN6	TSN7	TSN8
10Gb	10Gb	Q-5	Q-7	Q-1	Q-3	TSN1	TSN2	TSN3	TSN4



Part Reference:	LAN9, LAN10	LAN1 bis LAN8
Manufacturer:	Würth Elektronik	Würth Elektronik
Type:	749-961-1420	749 915 1120
Mates with:	RJ45 patch cable, category depending on speed	RJ45 patch cable, category depending on speed

The LAN Sockets have a standard layout for GBit Ethernet, i.e. the pairs are 1-2, 3-6, 4-5 and 7-8.

Pin	Pair
1	D-A+
2	D-A-
3	D-B+
4	D-C+
5	D-C-
6	D-B-
7	D-D+
8	D-D-

Table 6-3 LAN Gigabit Ethernet connector pairs

6.4.1 Possible LAN-Configurations

Serdes 2 and 3 are principle useable for QSGMII and SGMII. Seclotion has to be done in RCW and additional in controlling the hardware multiplexer on CRX05.

Serdes 2 = connector pin B116 = LS1088A pin D17 = GPIO2_7
 Serdes 3 = connector pin B117 = LS1088A pin E17 = GPIO2_16

GPIO2_7 and GPIO2_16 are not available on LS1088 as long as QSPI support is enabled via hardware strapping. They cannot control multiplexers.

That results in default setting is QSGMII (PullUp at selcetpin of multiplexer). So only QSGMII is available with MPX-LS1088A.

On CRX06 this leads to the limitation that QSGMII cannot be driven in SGMII-mode. Therefore two network configurations are supported for MPXLS1088/CRX06:

1. 2x XFI, 2x QSGMII: this is the configuration with 10 MACs enabled in total which is the maximum MACs that the LS1088A can support.
2. 2x XFI, 1x QSGMII, 2x RGMII: this is the configuration with 2 TSN-switches enabled.

6.4.2 SRD1 (XFI / SGMII)

Port 1 is connected to a 10G RJ-45 socket “LAN10”. It uses the SerDes Lanes 1 provided by the LS1088A CPU configured as SGMII port. The SGMII lanes connect to a Marvell PHY 88X3310P.

88X3310P			ST4			LS1088A	
Pin	Name		Pin	Signal		Pin	Name
C10	SRD-TX1+	←	T41	SRD-TX1+	←	AD6	SD1-TX0
D10	SRD-TX1-	←	T42	SRD-TX1-	←	AE6	SD1-TX0#
A9	SRD-RX1+	→	T38	SRD-RX1+	→	AG6	SD1-RX0
B9	SRD-RX1-	→	T39	SRD-RX1-	→	AH6	SD1-RX0#

Table 6-4 SerDes 1 pin assignment

6.4.3 SRD6 (XFI / SGMII)

Port 6 is connected to a 10G RJ-45 socket “LAN9”. It uses the SerDes Lanes 6 provided by the LS1088A CPU configured as SGMII port. The SGMII lanes connect to a Marvell PHY 88X3310P.

88X3310P			ST4			LS1088A	
Pin	Name		Pin	Signal		Pin	Name
C10	SRD-TX6+	←	T11	SRD-TX6+	←	AD19	SD2-TX3
D10	SRD-TX6-	←	T12	SRD-TX6-	←	AE19	SD2-TX3#
A9	SRD-RX6+	→	T9	SRD-RX6-	→	AH19	SD2-RX3#
B9	SRD-RX6-	→	T8	SRD-RX6+	→	AG19	SD2-RX3

Table 6-5 SerDes 6 pin assignment

6.4.4 SRD2 (QSGMII / SGMII)

Port 2 is connected to standard RJ-45 sockets “LAN5, LAN6”. It uses the SerDes Lanes 2 provided by the LS1088A CPU configured as QSGMII or SGMII port. The serdes lanes connect to a Marvell PHY 88E1548P.

88E1548P		M U X	ST4		LS1088A	
Pin	Name		Pin	Signal	Pin	Name
B1	SRD2-TXS+	0	T35	SRD-TX2+	AD11	SD-TX3
B9	SRD2-TXQ+	1 ←	T36	SRD-TX2-	AE11	SD-TX3#
A1	SRD2-TXS-	0	T32	SRD-RX2+	AG11	SD-RX3
A9	SRD2-TXQ-	1 ←	T33	SRD-RX2-	AH11	SD-RX3#
B2	SRD2-RXS+	0				
A8	SRD2-RXQ+	1 →				
A2	SRD2-RXS-	0				
B8	SRD2-RXQ-	1 →				

Table 6-6 SerDes 2 pin assignment

In case of QSGMII (LS1088) the system offers 4 ports 10/100/1000 Mbit. Connect to:

LAN5-A, LAN5-B, LAN6-A, LAN6-B

In case of SGMII the system offers only 1 port 10/100/1000 Mbit. Connect to:

LAN5-A

As Marvell PHY 88E1548P is using different connection pins for QSGMII and SGMII there is a multiplexer CBTL04083ABS (J20) to switch between connection groups. The multiplexer is controlled by GPIO

1 = QSGMII

0 = SGMII (is not possible to use with MXP-LS1088A)

CBTL04083ABS		←	ST4		←	LS1088A	
Pin	Name		Pin	Signal		Pin	Name
9	SRD2-SQ		B116	SRD2-SQ		D17	GPIO2_7

GPIO2_7 is not available on MPX-LS1088A with QSPI hardware strapping.

6.4.5 SRD3 (QSGMII / SGMII)

Port 3 is connected to standard RJ-45 sockets “LAN7, LAN8”. It uses the SerDes Lanes 3 provided by the LS1088A CPU configured as QSGMII or SGMII port. The serdes lanes connect to a Marvell PHY 88E1548P.

88E1548P		M U X	ST4		LS1088A	
Pin	Name		Pin	Signal	Pin	Name
B1	SRD3-TXS+	0	T41	SRD-TX3+	AD10	SD1-TX1
B9	SRD3-TXQ+	1 ←				

88E1548P			MUX	ST4			LS1088A	
Pin	Signal	MUX		Pin	Signal		Pin	Signal
A1	SRD3-TXS-	0	←	T42	SRD-TX3-	←	AE10	SD1-TX1#
A9	SRD3-TXQ-	1		T38	SRD-RX3+		AG10	SD1-RX1
B2	SRD3-RXS+	0	→	T39	SRD-RX3-	→	AH10	SD1-RX1#
A8	SRD3-RXQ+	1						
A2	SRD3-RXS-	0						
B8	SRD3-RXQ-	1						

Table 6-7 SerDes 3 pin assignment

In case of QSGMII the system offers 4 ports 10/100/1000 Mbit. Connect to:
LAN7-A, LAN7-B, LAN8-A, LAN8-B

In case of SGMII the system offers only 1 port 10/100/1000 Mbit. Connect to:
LAN7-A

As Marvell PHY 88E1548P is using different connection pins for QSGMII and SGMII there is a multiplexer CBTL04083ABS (J20) to switch between connection groups. The multiplexer is controlled by GPIO

1 = QSGMII

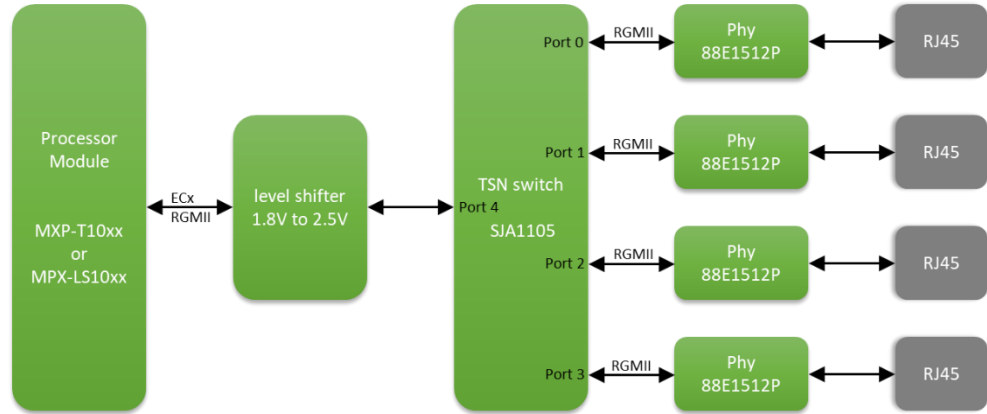
0 = SGMII (is not possible to use with MXP-LS1088A)

CBTL04083ABS		←	ST4		←	LS1088A	
Pin	Name		Pin	Signal		Pin	Name
9	SRD3-SQ		B117	SRD3-SQ		E17	GPIO2_16

GPIO2_16 is not available on MPX-LS1088A with QSPI hardware strapping.

6.4.6 TSN 1-4 Connections

TSN 1-4 is handled via EC1 (RGMII). SJA1105 (automotive 5 port ethernet switch) is connected to EC1 to expand to 4 external 1Gb ports. SJA1105 is conneted to 4x Marvell 88E1512P ethernet PHY.



The following table shows the internal connections for Port 4.

SJA1105 Port 4		ST4		LS1088A			
Pin	Name	Pin	Signal	Pin	Name		
P10	MII4-RX_CLK	→	T86	MII1-RXCK	→	W1	MII_RX_CLK
N12	MII4-RX_CTL	→	T95	MII1-RXDV	→	AB1	MII_RX_DV
N10	MII4-RXD0	→	T88	MII1-RXD0	→	AA2	MII_RXD0
P11	MII4-RXD1	→	T89	MII1-RXD1	→	AA1	MII_RXD1
N11	MII4-RXD2	→	T91	MII1-RXD2	→	Y1	MII_RXD2
P12	MII4-RXD3	→	T92	MII1-RXD3	→	W2	MII_RXD3
N9	MII4-TX_CLK	←	T94	MII1-TXCK	←	W4	MII_TX_CLK
P7	MII4-TXD0	←	T97	MII1-TXD0	←	AB3	MII_TXD0
N7	MII4-TXD1	←	T98	MII1-TXD1	←	AA3	MII_TXD1
P8	MII4-TXD2	←	T100	MII1-TXD2	←	Y4	MII_TXD2
N8	MII4-TXD3	←	T101	MII1-TXD3	←	Y3	MII_TXD3
P9	MII4-TX_CTL	←	T103	MII1-TXEN	←	AB4	MII_TXEN

Table 6-8 Port 4 pin assignment

88E1512P		SJA1105					
Pin	Name	Pin P0	Pin P1	Pin P2	Pin P3	Signal	
46	RX_CLK	→	E2	B6	B14	J13	TSNx-RX_CLK
43	RX_CTRL	→	G1	A4	A11	G14	TSNx-RX_CTL
44	RXD0	→	E1	A6	A13	J14	TSNx-RXD0
45	RXD1	→	F2	B5	B12	H13	TSNx-RXD1
47	RXD2	→	F1	A5	A12	H14	TSNx-RXD2

88E1512P			SJA1105				
48	RXD3	→	G2	B4	B11	G13	TSNx-RXD3
53	TX_CLK	←	D1	A7	C14	K14	TSNx-TX_CLK
50	TXD0	←	A2	B9	E13	M13	TSNx-TXD0
51	TXD1	←	B1	A9	E14	M14	TSNx-TXD1
54	TXD2	←	C2	B8	D13	L13	TSNx-TXD2
55	TXD3	←	C1	A8	D14	L14	TSNx-TXD3
56	TX_CTRL	←	D2	B7	C13	K13	TSNx-TX_CTL

Table 6-9 Port 0-3 pin assignment

6.4.7 TSN 5-8 Connections

TSN 5-8 is handled via EC2 (RGMII2). SJA1105 (automotive 5 port ethernet switch) is connected to EC2 to expand to 4 external 1Gb ports. SJA1105 is conneted to 4x Marvell 88E1512P ethernet PHY.

Blockdiagramm is same as for TSN1-4, but connected to RGMII2.

The following table shows the internal connections for Port 4.

SJA1105 Port 4		ST4		LS1088A			
Pin	Name	Pin	Signal	Pin	Name		
P10	MII4-RX_CLK	→	T75	MII2-RXCK	→	AC1	MII_RX_CLK
N12	MII4-RX_CTL	→	T66	MII2-RXDV	→	AF1	MII_RX_DV
N10	MII4-RXD0	→	T68	MII2-RXD0	→	AE2	MII_RXD0
P11	MII4-RXD1	→	T69	MII2-RXD1	→	AE1	MII_RXD1
N11	MII4-RXD2	→	T71	MII2-RXD2	→	AD1	MII_RXD2
P12	MII4-RXD3	→	T72	MII2-RXD3	→	AC2	MII_RXD3
N9	MII4-TX_CLK	←	T65	MII2-TXCK	←	AC4	MII_TX_CLK
P7	MII4-TXD0	←	T59	MII2-TXD0	←	AF3	MII_TXD0
N7	MII4-TXD1	←	T60	MII2-TXD1	←	AE4	MII_TXD1
P8	MII4-TXD2	←	T62	MII2-TXD2	←	AE3	MII_TXD2
N8	MII4-TXD3	←	T63	MII2-TXD3	←	AD3	MII_TXD3
P9	MII4-TX_CTL	←	T56	MII2-TXEN	←	AG3	MII_TXEN

Table 6-10 Port 4-7 pin assignment

Interconnecting SJA1105 switch for TSN5-8 is same as for TSN1-4.

6.4.8 MDIO1 addressing

MDIO1 is connected to Phys: 2x 88E1548P, 8x 88E1512P.

Part	component	Address
J8	88E1512P	Addr = 0x00h
J10	88E1512P	Addr = 0x01h
J12	88E1512P	Addr = 0x02h
J14	88E1512P	Addr = 0x03h
J9	88E1512P	Addr = 0x04h
J11	88E1512P	Addr = 0x05h
J13	88E1512P	Addr = 0x06h
J15	88E1512P	Addr = 0x07h
J41	88E1548P	Addr = 0x08h to 0x0Bh
J42	88E1548P	Addr = 0x0Ch to 0x0Fh

Table 6-11 LAN / MDIO1 / Addressing

6.4.9 MDIO2 addressing

MDIO2 is connected to Phys: 2x 88X3310P.

Part	component	Address
J22	88X3310P	Addr = 0x10h
J23	88X3310P	Addr = 0x11h

Table 6-12 LAN / MDIO2 / Addressing

6.5 PCIe Connections

The SBC-LS1088A-TSN offers one x4 lane on the following connectors. That may be configured to two x2 or four x1 lanes. PCIe x4 is not available with MPX-T10xx modules.

Serdes	PCIe Port 0	PCIe Port 1	PCIe Port 2	PCIe Port 3
Lane 4	✓			
Lane 5		✓		
Lane 0			✓	
Lane 7				✓

Table 6-13 PCIe SerDes assignment

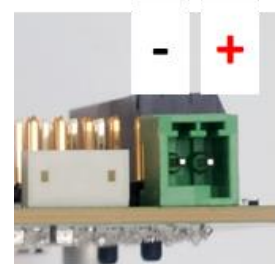
Basically, the carrierboard offers four x1 lanes on different connectors which may be available in combination with other MPX2 modules.

Part Reference:	PCIe
Manufacturer:	Molex
Type:	MOL-0877159100
Used with:	PCIe cards



If +12V power is required for external board, separate power has to be connected to connector PCIPWR. Voltage has to be exactly 12V. There is just protection for reverse polarity but no protection for overvoltage.

Part Reference	PCIPWR
Manufacturer:	Würth Elektronik
Type:	691 382 010 002
Mates with:	691 381 000 002



Pin-out:

Pin	Name	Function
1	„-“	GND
2	„+“	+VIN (= typ. 12V)

Table 6-14 PCIPWR

Pin:			Pin:
1a	PRSNT1#	+12V	1b
2a	+12V	+12V	2b
3a	+12V	+12V	3b
4a	GND	GND	4b
5a	JTCK	SMCLK	5b
6a	JTDI	SMDAT	6b
7a	JTDO	GND	7b
8a	JTMS	+3.3V	8b
9a	+3.3V	JTRST#	9b
10a	+3.3V	+3.3V	10b
11a	PERST#	GND	11b
MECHANICAL KEY			
12a	GND	RSVD1	12b
13a	RFCLK+	GND	13b
14a	RFCLK-	PET0+	14b
15a	GND	PET0-	15b
16a	PER0+	GND	16b
17a	PER0-	PRSNT2#	17b
18a	GND	GND	18b
19a	RSVD2	PET1+	19b
20a	GND	PET1-	20b
21a	PER1+	GND	21b
22a	PER1-	GND	22b
23a	GND	PET2+	23b
24a	GND	PET2-	24b
25a	PER2+	GND	25b
26a	PER2-	GND	26b
27a	GND	PET3+	27b
28a	GND	PET3-	28b
29a	PER3+	GND	29b
30a	PER3-	RSVD3	30b
31a	GND	PRSNT2#	31b
32a	RSVD4	GND	32b

Table 6-15 mPCIe Slot pinout

The following table shows the internal connections:

PCIE			ST4			LS1088A	
Pin	Name		Pin	Signal		Pin	Name
14b	PET0+	←	T23	SRD-TX4+	←	AD15	SD2-TX0
15b	PET0-	←	T24	SRD-TX4-	←	AE15	SD2-TX0#
16a	PER0+	→	T20	SRD-RX4+	→	AG15	SD2-RX0
17a	PER0-	→	T21	SRD-RX4-	→	AH15	SD2-RX0#
19b	PET1+	←	T17	SRD-TX5+	←	AD16	SD2-TX1_P
20b	PET1-	←	T18	SRD-TX5-	←	AE16	SD2-TX1_N
21a	PER1+	→	T14	SRD-RX5+	→	AG16	SD2-RX1_P
22a	PER1-	→	T15	SRD-RX5-	→	AH16	SD2-RX1_N
23b	PET2+	←	T47	SRD-TX0+	←	AD18	SD2-TX2
24b	PET2-	←	T48	SRD-TX0-	←	AE18	SD2-TX2#
25a	PER2+	→	T44	SRD-RX0+	→	AG18	SD2-RX2
26a	PER2-	→	T45	SRD-RX0-	→	AH18	SD2-RX2#
27b	PET3+	←	T5	SRD-TX7+	←	AD19	SD2_TX3_P
28b	PET3-	←	T6	SRD-TX7-	←	AE19	SD2_TX3_N
29a	PER3+	→	T2	SRD-RX7+	→	AG19	SD2_RX3_P
30a	PER3-	→	T3	SRD-RX7-	→	AH19	SD2_RX3_N

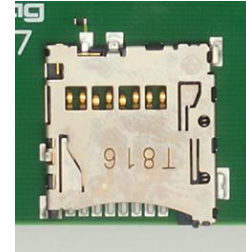
Table 6-16 PCIe Slot SerDes 4 assignment

6.6 microSD Card Slot

The SBC-LS1088A-TSN system offers a microSD Card slot.

The microSD card can also be configured as a boot device.

Part Reference:	ST1
Manufacturer:	Yamaichi
Type:	PJS-008-2130-0
Used with:	microSD cards



The following table shows the connections of the microSD card slot:

I/O Range	ST1			ST4			LS1088A	
	Pin	Name		Pin	Signal		Pin	Name
LVTTL	1	DAT2	↔	B96	SDC-D2	↔	R1	SDHC_DAT2
LVTTL	2	CD/DAT3	↔	B95	SDC-D3	↔	T1	SDHC_DAT3
LVTTL	3	CMD	↔	B99	SDC-CMD	↔	P2	SDHC_CMD
	4	Vdd						
LVTTL	5	CLK	←	B100	SDC-CLK	←	P3	SDHC_CLK
	6	Vss						
LVTTL	7	DAT0	↔	B98	SDC-D0	↔	P1	SDHC_DAT0
LVTTL	8	DAT1	↔	B97	SDC-D1	↔	R2	SDHC_DAT1
LVTTL	9	SW1	→	B90	SDC-CD#			
LVTTL	10	SW2	→	B89	SDC-WP			

Table 6-17 microSD card slot pin assignment



NOTE

The microSD card slot uses a copy of the reference voltage on pin B81 of the module connector ST4 as I/O voltage (3.3V).

This voltage is generated on the carrierboard.

6.7 USB

The SBC-LS1088A-TSN system features a stacked USB connector for two ports.

Both USB host ports support USB super speed mode

Part Reference:	ST6
Manufacturer:	Würth Elektronik
Type:	692 141 030 100
Mates with:	USB Type A cables



6.7.1 USB1

The following table shows the internal connections:

ST6 (Bottom)			ST4			LS1088A	
Pin	Signal		Pin	Signal		Pin	Name
1	Vbus+	→	B133	USB1-VBUS	→	E7	USB1_VBUS
2	D-	↔	T131	USB1-D-	↔	E6	USB1_D_M
3	D+	↔	T130	USB1-D+	↔	F6	USB1_D_P
4	GND						
5	SSRX-	→	T118	USB1-SSRX+	→	E3	USB1_RX_P
6	SSRX+	→	T119	USB1-SSRX-	→	E4	USB1_RX_M
7	GND						
8	SSTX-	←	T122	USB1-SSTX-	←	F2	USB1_TX_M
9	SSTX+	←	T121	USB1-SSTX+	←	F1	USB1_TX_P
J4							
Pin	Signal						
4	ENABLE	←	B132	USB1-EN	←	H6	USB1_DRVVBUS
3	FAULT#	→	B131	USB1-OC	→	G6	USB1_PWRFAULT
		→	B130	USB1-UID	→	F5	USB1_ID

Table 6-18 USB Host-Only Port 1 pin assignment

USB port 1 can be individually enabled and has a separate overcurrent signal.



USB1_PWRFAULT is a high-active signal. A logic high level signals the port is in an overcurrent situation

6.7.2 USB2

The following table shows the internal connections:

ST6 (Top)			ST4			LS1088A	
Pin	Signal		Pin	Signal		Pin	Name
1	Vbus+	→	B128	USB2-VBUS	→	C7	USB2_VBUS
2	D-	↔	T128	USB2-D-	↔	C6	USB2_D_M
3	D+	↔	T127	USB2-D+	↔	D6	USB2_D_P
4	GND						
5	SSRX-	→	T112	USB2-SSRX+	→	C3	USB2_RX_P
6	SSRX+	→	T113	USB2-SSRX-	→	C4	USB2_RX_M
7	GND						
8	SSTX-	←	T116	USB2-SSTX-	←	D2	USB2_TX_M
9	SSTX+	←	T115	USB2-SSTX+	←	D1	USB2_TX_P
J5							
Pin	Signal						
4	ENABLE	←	B127	USB2-EN	←	L4	USB2_DRVVBUS
3	FAULT#	→	B126	USB2-OC	→	M4	USB2_PWRFAULT
		→	B125	USB2-UID	→	D5	USB2_ID

Table 6-19 USB Host-Only Port 2 pin assignment

USB port 2 can be individually enabled and has a separate overcurrent signal.



USB2_PWRFAULT is a high-active signal. A logic high level signals the port is in an overcurrent situation

6.7.3 USB3

USB port 3 is not a native USB port of the CPU but converted from UART1 by means of a FT232RQ chip.

USB3 is available on an USB mini connector type B.

The port is used as the debug port of the LS1088A.

Part Reference:	ST5
Manufacturer:	Würth Elektronik
Type:	651 005 161 21
Used with:	Mini USB type B cables



The following table shows the internal connections:

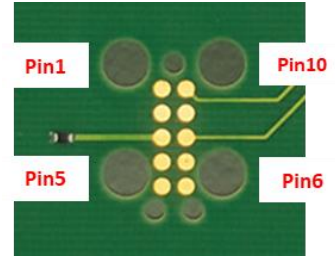
ST5		ST4		LS1088A	
Pin	Signal	Pin	Signal	Pin	Name
1	Vbus+	B37	UART1-RXD	H2	UART1_SIN
2	D-	B38	UART1-TXD	H1	UART1_SOUT
3	D+				
4	ID				
5	GND				

Table 6-20 USB Host-Only Port 3 pin assignment

6.8 MCU Connector

The connector "MCU" is for production test only.

Part Reference:	MCU
Manufacturer:	Tag-Connect
Type:	TC2050-IDC-FP



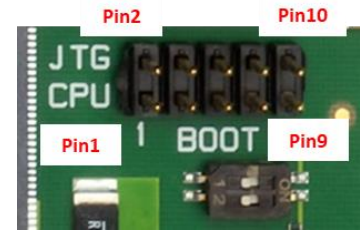
MCU	
Pin	Signal
1	Please contact MicroSys
2	
3	
4	
5	
6	
7	
8	
9	
10	

Table 6-21 MCU Connector Pinout

6.9 JTAG 1 Connector (Processor)

The JTAG signals are available on 2x5 pin header. This TAP connects to processor on module only.

Part Reference:	JTG1
Manufacturer:	any
Type:	HEADER-2.54-180-M-2X5



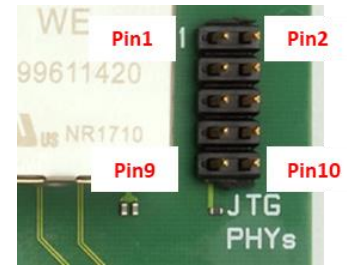
JTG1			ST4			LS1088A	
Pin	Signal		Pin	Signal		Pin	Signal
1	JTMS	→	B102	JTMS	→	G18	TMS
2	HRST#	↔	B111	HRST#	↔	F8	HRESET#
3	+1,8V						
4	TRST#	→	B106	TRST#	→	E19	TRST#
5	JTDO	←	B104	JTDO	←	E20	TDO
6	JTCK	→	B105	JTCK	→	E18	TCK
7	GND						
8	PRST#	→	B110	PRST#	→	F9	PORESET#
9	JTDI	→	B103	JTDI	→	G17	TDI
10	-						

Table 6-22 JTAG Connector Pinout

6.10 JTAG 2 Connector (Carrier Components)

The JTAG signals are available on 2x5 pin header. This TAP connects to parts on carrier only. Interface is 1:1 compatible to Göpel boundary scan controllers.

Part Reference:	JTG2
Manufacturer:	any
Type:	HEADER-2.54-180-M-2X5

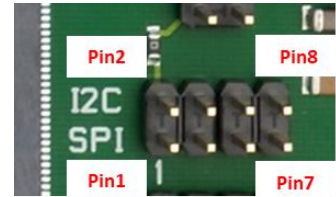


JTG2			Carrier components
Pin	Signal		
1	TCK	→	J22, J23, J31, J36, J41, J42
2	GND	↔	
3	TMS		J22, J23, J31, J36, J41, J42
4	GND	→	
5	TDO	←	TDO → J31
6	GND	→	
7	TDI		TDI → J22 → J23 → J41 → J42 → J36 → J31 (chain)
8	GND	→	
9	TRST#	→	J22, J23, J31, J36, J41, J42
10	-		

Table 6-23 JTAG Connector Pinout

6.11 I2C / SPI Extension (JP1)

Part Reference:	JP1
Manufacturer:	any
Type:	HEADER-2.54-180-M-2X4

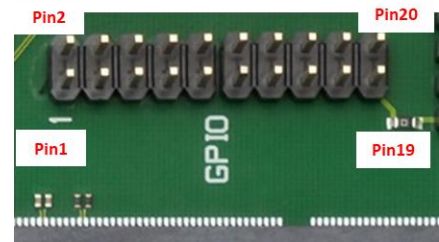


JP1		ST4		LS1088A			
Pin	Signal	Pin	Signal	Pin	Signal		
1	SPI-CLK	←	B69	SPI-CLK	←	U2	SPI-CLK-18
2	+3.3V						
3	SPI-MISO	→	B72	SPI-MISO	→	U3	SPI-MISO-18
4	I2CE-SDA	↔	B74	I2C2-SDA	↔		
5	SPI-MOSI	←	B71	SPI-MOSI	←	V3	SPI-MOSI-18
6	I2CE-SCL	←	B75	I2C2-SCL	←		
7	SPI-CS3#	←	B91	SPI-CS3#	←	V1	SPI-CS3-18#
8	GND						

Table 6-24 I2C / SPI Extension Connector Pinout

6.12 GPIO Extension (JP2)

Part Reference:	JP2
Manufacturer:	any
Type:	HEADER-2.54-180-M-2X10



UART2 is available on the following extension connector including hardware handshaking with RTS/CTS. The I/O range is LVTTTL.

UART1 handshaking RTS/CTS is available on the following extension connector. The I/O range is LVTTTL.



For RS232 or RS485 additional transceivers are necessary. They are not implemented on the SBC-LS1088A-TSN system.

JP2			ST4			LS1088A	
Pin	Signal		Pin	Signal		Pin	Signal
1	UART2-TXD	←	B33	UART2-TXD	←	L2	UART2-TXD
2	UART2-RXD	→	B32	UART2-RXD	→	K1	UART2-RXD
3	UART2-RTS#	←	B35	UART2-RTS#	←	L1	UART2-RTS#
4	UART2-CTS#	→	B34	UART2-CTS	→	M2	UART2-CTS
5	UART1-RTS#	←	B40	UART1-RTS#	←	J2	UART1-RTS#
6	UART1-CTS#	→	B39	UART1-CTS#	→	J1	UART1-CTS#
7	GPIO-10	↔			↔		nc
8	GPIO-11	↔			↔		nc
9	GPIO-8	↔			↔		nc
10	GPIO-9	↔			↔		nc
11	GPIO-6	↔			↔		nc
12	GPIO-7	↔			↔		nc
13	GPIO-4	↔			↔		nc
14	GPIO-5	↔			↔		nc
15	GPIO-2	↔			↔		nc
16	GPIO-3	↔	B123	GPIO-3-18	↔	A19	GPIO2_10
17	GPIO-0	↔	B122	GPIO-0-18	↔	D20	GPIO2_11
18	GPIO-1	↔	B121	GPIO-1-18	↔	C20	GPIO2_12
19	+3.3V						
20	GND						

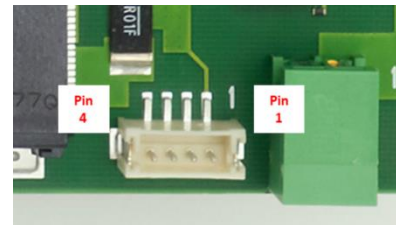
Table 6-25 I2C / SPI Extension Connector Pinout

6.13 Fan Connector (PWE)

The SBC-LS1088A-TSN provides a fan connector marked with „PWE“.

In case a fan is necessary MicroSys recommends to use a 5V rated fan.

Part Reference:	PWE
Manufacturer:	Würth Elektronik
Type:	679 304 124 022
Mates with:	648 004 113 322



Pin:	Description
1	+5V
2	GND
3	GND
4	+VIN

Table 6-26 FAN connector pinout (PWE)

7 Switches, Buttons and Jumpers

7.1 Boot Device Switch

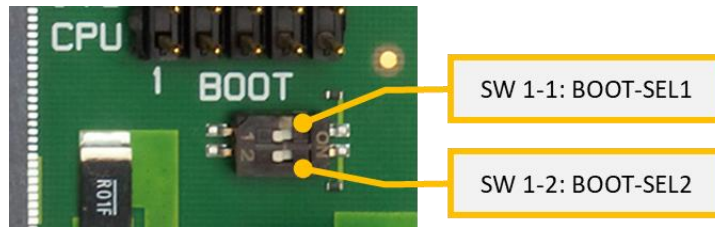


Figure 7-1 Boot Device Switch

The boot device can be selected by the switch “SW1”.

The boot device switches implement a maximum of four possible boot devices. The following boot devices are supported by the LS1088A:





Setting	SW 1-1	SW 1-2	Boot device	Features	Boot location
	OFF	OFF	SPI Flash		module
	OFF	ON	NAND Flash		module
	ON	OFF	SD/MMC	SD/MMC Bus width: 8 bit SPI-CS0# [PIN-B70] is <u>NOT</u> accessible	carrier board
	ON	ON	SD/MMC	SD/MMC Bus width: 4 bit SPI-CS0# [PIN-B70] is <u>NOT</u> accessible	carrier board

Table 7-1 Boot device settings



NOTE SW1 inverts the logic levels of the BOOT-SELx pins. By setting the switch to ON the corresponding pin is actually pulled low (grounded).

The following table shows the internal connections of the BOOT-SEL pins:

SW1			ST4			Microcontroller	
Switch	Signal		Pin	Signal		Pin	Name
1-1	BOOT-SEL1	→	T134	BOOT-SEL1	→	61	PTD4
1-2	BOOT-SEL2	→	T133	BOOT-SEL2	→	62	PTD5

Table 7-2 BOOT-SELx pin assignment

7.2 Board Configuration Switch

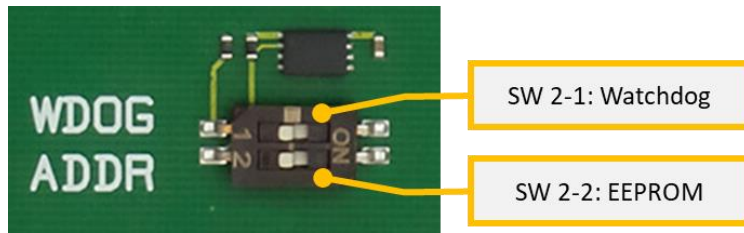


Figure 7-2 Board Configuration Switch

The board configuration switch influences the behavior of the watchdog and the I²C address of the EEPROM on I²C Bus1:

Setting	SW 2-1	SW 2-2	Description
	OFF	-	Watchdog disabled
	ON	-	Watchdog active
	-	OFF	EEPROM J25: address 0x57
	-	ON	EEPROM J25: address 0x55

Table 7-3 Configuration switch settings

7.3 Reset Button

Pressing the reset switch “SW3” triggers a Hard Reset.

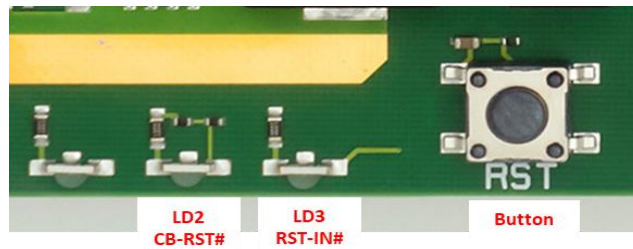


Figure 7-3 Reset Button

SW3 is connected to the reset input of a MAX6751KA29 chip via additional logic. The resulting open drain reset signal is then inverted and fed to the microcontroller.

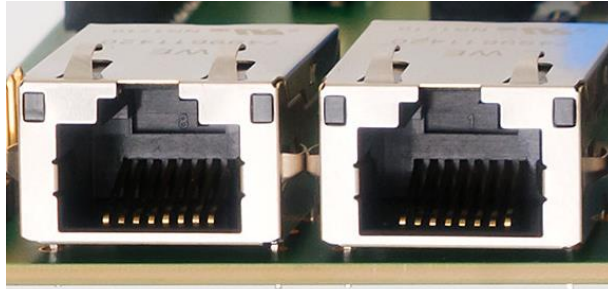
The following table shows the internal connections:

SW3			J17		ST4		Microcontroller	
Pin	Signal		Pin		Pin	Signal	Pin	Name
1 & 3	+3,3V							
2 & 4	RST-BTN (\$39166)	→	1					
			7	→	T136	RST-IN#	→	52 PTC7

Table 7-4 Reset button pinout

8 LEDs

8.1 RJ45 LEDs 10Gb



The following table summarizes the RJ45 LEDs for 10Gb of the

Figure 8-1 RJ 45 LEDs

SBC-LS1088A-TSN:

Part Reference	Source	Signal Name	Function
LAN9	J22	LED-10G1-0	Left Yellow LED: off
LAN9	J22	LED-10G1-1	Right Green LED: configurable Default: 3 blinks – 1000Mbps / 2 blinks – 100 Mbps / 1 blink – 10 Mbps / 0 blinks – no link Right Yellow LED: off
		LED-10G1-2	
LAN10	J23	LED-10G2-0	Left Yellow LED: off
LAN10	J23	LED-10G2-1	Right Green LED: configurable Default: 3 blinks – 1000Mbps / 2 blinks – 100 Mbps / 1 blink – 10 Mbps / 0 blinks – no link Right Yellow LED: off
		LED-10G2-2	

Table 8-1 Indicator LEDs

8.2 RJ45 LEDs QSGMII

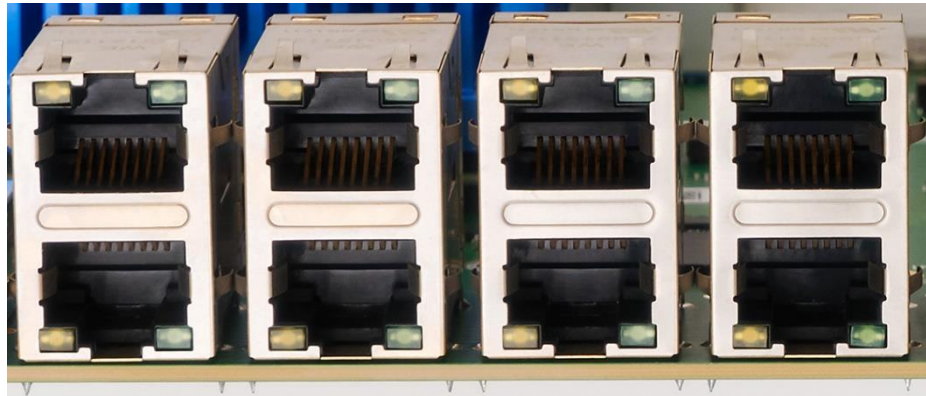


Figure 8-2 RJ 45 LEDs

The following table summarizes the RJ45 LEDs for QSGMII/SGMII of the SBC-LS1088A-TSN:

Part Reference	Source	Signal Name	Function
LAN7-A	J42 P0_LED0	LAN5-LED0	Green LED: configurable Default: 3 blinks – 1000Mbps / 2 blinks – 100 Mbps / 1 blink – 10 Mbps / 0 blinks – no link
LAN7-A	J42 P0_LED1	LAN5-LED1	Yellow LED: off
LAN7-B	J42 P1_LED0	LAN6-LED0	Green LED: configurable Default: On = Link / Off = no Link / Blink = Activity
LAN7-B	J42 P1_LED1	LAN6-LED1	Yellow LED: off
LAN8-A	J42 P2_LED0	LAN7-LED0	Green LED: configurable Default: 3 blinks – 1000Mbps / 2 blinks – 100 Mbps / 1 blink – 10 Mbps / 0 blinks – no link
LAN8-A	J42 P2_LED1	LAN7-LED1	Yellow LED: off
LAN8-B	J42 P3_LED0	LAN8-LED0	Green LED: configurable Default: On = Link / Off = no Link / Blink = Activity
LAN8-B	J42 P3_LED1	LAN8-LED1	Yellow LED: off
LAN5-A	J41 P0_LED0	LAN1-LED0	Green LED: configurable Default: 3 blinks – 1000Mbps / 2 blinks – 100 Mbps / 1 blink – 10 Mbps / 0 blinks – no link
LAN5-A	J41 P0_LED1	LAN1-LED1	Yellow LED: off
LAN5-B	J41 P1_LED0	LAN2-LED0	Green LED: configurable Default: On = Link / Off = no Link / Blink = Activity
LAN5-B	J41 P1_LED1	LAN2-LED1	Yellow LED: off
LAN6-A	J41 P2_LED0	LAN3-LED0	Green LED: configurable Default: 3 blinks – 1000Mbps / 2 blinks – 100 Mbps / 1 blink – 10 Mbps / 0 blinks – no link

Part Reference	Source	Signal Name	Function
LAN6-A	J41 P2_LED1	LAN3-LED1	Yellow LED: off
LAN6-B	J41 P3_LED0	LAN4-LED0	Green LED: configurable Default: On = Link / Off = no Link / Blink = Activity
LAN6-B	J41 P3_LED1	LAN4-LED1	Yellow LED: off

Table 8-2 Indicator LEDs

8.3 RJ45 LEDs TSN



Figure 8-3 RJ 45 LEDs

The following table summarizes the RJ45 LEDs of the SBC-LS1088A-TSN:

Part Reference	Source	Signal Name	Function
LAN1-A	J8	TSN1-LED0	Green LED: configurable Default: 3 blinks – 1000Mbps / 2 blinks – 100 Mbps / 1 blink – 10 Mbps / 0 blinks – no link
LAN1-A	J8	TSN1-LED2	Yellow LED: off
LAN1-B	J9	TSN5-LED0	Green LED: configurable Default: On = Link / Off = no Link / Blink = Activity
LAN1-B	J9	TSN5-LED2	Yellow LED: off
LAN2-A	J10	TSN2-LED1	Green LED: configurable Default: 3 blinks – 1000Mbps / 2 blinks – 100 Mbps / 1 blink – 10 Mbps / 0 blinks – no link
LAN2-A	J10	TSN2-LED2	Yellow LED: off
LAN2-B	J11	TSN6-LED1	Green LED: configurable Default: On = Link / Off = no Link / Blink = Activity

Part Reference	Source	Signal Name	Function
LAN2-B	J11	TSN6-LED2	Yellow LED: off
LAN3-A	J12	TSN3-LED0	Green LED: configurable Default: 3 blinks – 1000Mbps / 2 blinks – 100 Mbps / 1 blink – 10 Mbps / 0 blinks – no link
LAN3-A	J12	TSN3-LED2	Yellow LED: off
LAN3-B	J13	TSN7-LED0	Green LED: configurable Default: On = Link / Off = no Link / Blink = Activity
LAN3-B	J13	TSN7-LED2	Yellow LED: off
LAN4-A	J14	TSN4-LED1	Green LED: configurable Default: 3 blinks – 1000Mbps / 2 blinks – 100 Mbps / 1 blink – 10 Mbps / 0 blinks – no link
LAN4-A	J14	TSN4-LED2	Yellow LED: off
LAN4-B	J15	TSN8-LED1	Green LED: configurable Default: On = Link / Off = no Link / Blink = Activity
LAN4-B	J15	TSN8-LED2	Yellow LED: off

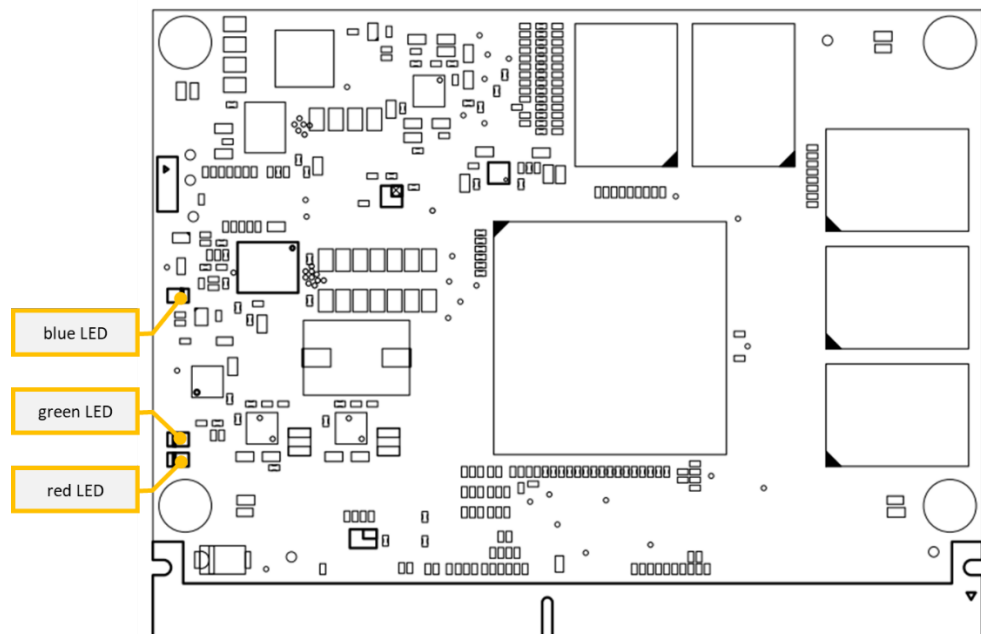
Table 8-3 Indicator LEDs

8.4 Power And Reset LEDs

LEDs are located on module.

Part Reference	Source	Signal Name	Function
LD1	PWR	VEXT	Power (VEXT) On
LD2	ST4	CB-RST#	Carrier board reset active
LD3	J17 / SW3	RST-IN#	<ul style="list-style-type: none"> • Power on the carrier is not ok • watchdog reset is active • manual reset is triggered

Table 8-4 Indicator LEDs - Carrier board



Colour	Function
Green	LED ON: Power-up sequence of the module is finished, power is good LED OFF: Power fail
Red	LED ON: Module reset is active LED OFF: Reset is inactive
Blue	General Purpose LED

Table 8-5 Indicator LEDs – Module

8.5 RGB LEDs

The SBC-LS1088A-TSN provides a RGB LED driver controlling four RGB LEDs.



I²C address 0x68 is existing twice on I2C-1 bus.

Therefore, the so-called “All Call I2C address” of the TLC59116IRHBR RGB LED driver has to be disabled before GP input pins of the MAX7325 port expander can be read correctly. This can be achieved by setting the default value 1 of Bit 0 in MODE1 register to 0.

The following table shows how the LEDs are mapped to the driver outputs:

Part Reference	LED Driver Output	LED Output Register
LD4	LED0	0x14
	LED1	
	LED2	
	LED3 is not connected	
LD7	LED4	0x15
	LED5	
	LED6	
	LED7 is not connected	
LD6	LED8	0x16
	LED9	
	LED10	
	LED11 is not connected	
LD5	LED12	0x17
	LED13	
	LED14	
	LED15 is not connected	

Table 8-5 RGB LEDs – Carrier

9 Software

9.1 U-Boot

The SBC-LS1088A-TSN uses an U-Boot as standard boot loader, which is always integrated in both the board's NAND and QSPI Flash memories on delivery.

Additionally, there's an U-Boot version available to be placed on microSD card, if both other boot options should fail for some reason.

Either boot option can be selected by the Boot Device Switch (see chapter 7).

9.2 Operating System Support

MicroSys Electronics GmbH offers Linux and Microware OS-9 RTOS support for the board.

Other Operating Systems are available on request only.

If you should have ordered a Starter Kit, the most recent Linux will already be installed in the board's flash, so you can start to develop and test your application right away.

9.3 Flash Layout



The flash layout may be subject to change in the future.

9.3.1 NAND Flash

Start	End	Definition	Size
0x0000_0000	0x000F_FFFF	PBL + SPL + U-boot	1MB
0x0010_0000	0x0013_FFFF	Environment	256kB
0x0014_0000	0x0015_FFFF	FMAN Microcode	128kB
0x0016_0000	0x001F_FFFF	reserved	640kB
0x0020_0000	NAND_SIZE-1	free	

Table 9-1 NAND Flash layout

9.3.2 SD Card

1 block = 512 byte

Start block	End block	Definition
0000	0007	reserved
0008	2047	U-boot
2048	2079	Environment
2080	2207	FMAN Microcode
2208	8191	reserved
8192	SDCARD-SIZE-1	free

Table 9-2 SD Card layout

9.3.3 QSPI Flash

Start	End	Definition	Size
0x0000_0000	0x0000_FFFF	RCW + PBL	64kB
0x0001_0000	0x0003_FFFF	FMAN Microcode	192kB
0x0004_0000	0x000F_FFFF	reserved	768kB
0x0010_0000	0x001F_FFFF	U-Boot	1MB
0x0020_0000	0x0023_FFFF	Environment	256kB
0x0024_0000	SPI-SIZE-1	free	

Table 9-3 QSPI Flash layout

10 Appendix

10.1 Acronyms

These acronyms are being used within the document; note that this list does not claim to be complete or exhaustive:

<i>CPU</i>	<i>Central Processing Unit</i>
<i>DC</i>	<i>Direct Current</i>
<i>DDR4</i>	<i>Double Data Rate Memory fourth-generation</i>
<i>ESD</i>	<i>Electrostatic Discharge</i>
<i>Gbps</i>	<i>Gigabit per second</i>
<i>GND</i>	<i>Ground</i>
<i>GPL</i>	<i>General Public License</i>
<i>I2C</i>	<i>Inter-Integrated Circuit</i>
<i>JTAG</i>	<i>Joint Test Action Group</i>
<i>LAN</i>	<i>Local Area Network</i>
<i>LED</i>	<i>Light Emitting Diode</i>
<i>LVTTL</i>	<i>Low Voltage Transistor–Transistor Logic</i>
<i>MCU</i>	<i>Microcontroller Unit</i>
<i>PCIe</i>	<i>Peripheral Component Interconnect Express</i>
<i>RGMIIR</i>	<i>Reduced Gigabit Media-independent Interface, Reduced Gigabit Media-independent Interface, Reduced Gigabit Media-independent Interface, Reduced Gigabit Media-independent Interface, Reduced Gigabit Media-independent Interface</i>
<i>RTC</i>	<i>Real Time Clock</i>
<i>SBC</i>	<i>Single Board Computer</i>
<i>SDRAM</i>	<i>Synchronous Dynamic Random Access Memory</i>
<i>SerDes</i>	<i>Serializer/Deserializer, Serializer/Deserializer</i>
<i>SOM</i>	<i>System On Module</i>
<i>UART</i>	<i>Universal Asynchronous Receiver Transmitter</i>
<i>USB</i>	<i>Universal Serial Bus</i>

10.2 Table of Figures

Figure 3-1 System setup example.....	11
Figure 4-1 Block Diagram (MPX-LS1088A Revision 2 on carrier CRX06 Revision 2).....	15
Figure 4-2 Mechanical Dimensions Module	18
Figure 4-3 CRX06 Mechanical Dimensions	19
Figure 4-4 Top connectors	20
Figure 5-1 Reset Structure (carrier CRX06 Revision 2)	24
Figure 7-1 Boot Device Switch.....	56
Figure 7-2 Board Configuration Switch	57
Figure 7-3 Reset Button	58
Figure 8-1 RJ 45 LEDs.....	59
Figure 8-2 RJ 45 LEDs.....	60
Figure 8-3 RJ 45 LEDs.....	61

10.3 Table of Tables

Table 1-1 Symbols	6
Table 1-2 Conventions.....	6
Table 2-1 Safety and Handling Precautions.....	7
Table 2-2 Functional coverage.....	9
Table 4-1 Pinout PWR	21
Table 5-1 Reset signal overview	25
Table 5-2 Voltage monitoring limits (carrier).....	25
Table 5-3 Clock distribution.....	27
Table 5-4 Hard wired boot signals.....	28
Table 5-5 NAND Flash pin assignments	29
Table 5-6 QSPI Flash pin assignment.....	30
Table 5-7 I ² C1 bus map	31
Table 5-8 I ² C-1 pin assignment.....	32
Table 5-9 I ² C2 bus map	32
Table 5-10 I ² C-2 pin assignment	33
Table 6-1 Connector reference overview	34
Table 6-2 LAN / DTSEC / SerDes / usage	35
Table 6-3 LAN Gigabit Ethernet connector pairs.....	36
Table 6-4 SerDes 1 pin assignment.....	37
Table 6-5 SerDes 6 pin assignment	37
Table 6-6 SerDes 2 pin assignment	38
Table 6-7 SerDes 3 pin assignment	39
Table 6-8 Port 4 pin assignment	40
Table 6-9 Port 0-3 pin assignment	41
Table 6-10 Port 4-7 pin assignment	41
Table 6-11 LAN / MDIO1 / Addressing.....	42

Table 6-12 LAN / MDIO2 / Addressing 42

Table 6-13 PCIe SerDes assignment 43

Table 6-14 PCIPWR 44

Table 6-15 mPCIe Slot pinout 44

Table 6-16 PCIe Slot SerDes 4 assignment 45

Table 6-17 microSD card slot pin assignment 46

Table 6-18 USB Host-Only Port 1 pin assignment 47

Table 6-19 USB Host-Only Port 2 pin assignment 48

Table 6-20 USB Host-Only Port 3 pin assignment 49

Table 6-21 MCU Connector Pinout 50

Table 6-22 JTAG Connector Pinout 51

Table 6-23 JTAG Connector Pinout 52

Table 6-24 I2C / SPI Extension Connector Pinout 53

Table 6-25 I2C / SPI Extension Connector Pinout 54

Table 6-26 FAN connector pinout (PWE) 55

Table 7-1 Boot device settings 56

Table 7-2 BOOT-SELx pin assignment 56

Table 7-3 Configuration switch settings 57

Table 7-4 Reset button pinout 58

Table 8-1 Indicator LEDs 59

Table 9-1 NAND Flash layout 66

Table 9-2 SD Card layout 66

Table 9-3 QSPI Flash layout 66

Table 11-1 Document history 70

11 History

Date	Version	Change Description
2017-10-25	1.0	Release Version for carrier CRX06 Revision 1
2018-07-16	2.0	Changes to carrier CRX06-R2
2019-08-08	2.1	Generate LS1088A from LS1046A

Table 11-1 Document history