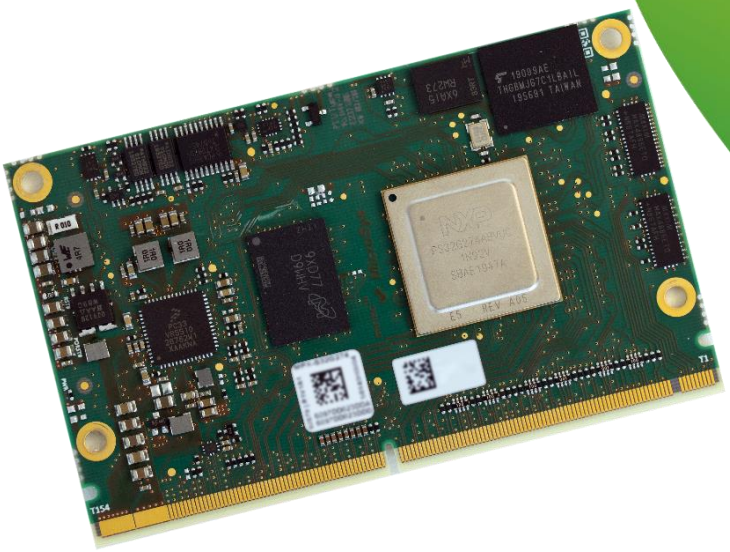

# miriac MPX-S32G274A

## User Manual (HW Revision 2)

**V2.3**

# Table of Contents

# 1 General Notes



## 1.1 Warranty

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# 1.5 Symbols, Conventions and Abbreviations

## 1.5.1 Symbols

Throughout this document, the following symbols will be used:

| | |
|---|---|
|   | Information marked with this symbol MUST be obeyed to avoid the risk of severe injury, health danger, or major destruction of the unit and its environment |
|   | Information marked with this symbol MUST be obeyed to avoid the risk of possible injury, permanent damage or malfunction of the unit. |
|   | Information marked with this symbol gives important hints upon details of this manual, or in order to get the best use out of the product and its features. |

*Table 1 Symbols*

## 1.5.2 Conventions

| Symbol | Explanation |
|---|---|
| # / xxx_B | denotes a low active signal |
| ← | denotes the signal flow in the direction shown |
| → | denotes the signal flow in the direction shown |
| ↔ | denotes the signal flow in both directions |
| → | denotes the signal flow in the direction shown with additional logic / additional ICs in the signal path |
| I/O / INOUT | denotes a bidirectional pin |
| Input | denotes an input pin |
| Output | denotes an output pin |
| matched | denotes the according signal to be routed impedance controlled and length matched |
| Pin 1 | refers to the numeric pin of a component package |
| Pin a1 | refers to the array position of a pin within a component package |
| xxx- / xxx_N | denotes the negative signal of a differential pair |
| xxx+ / xxx_P | denotes the positive signal of a differential pair |
| xxx | denotes an optional not mounted or fitted part |

*Table 2 Conventions*

## 1.6 Safety and Handling Precautions

| | |
|---|---|
|  | **DO NOT exceed the rated maximum values for the power supply! This may result in severe permanent damage to the unit, as well as possible serious injury.**<br>**ALWAYS keep the unit dry, clean and free of foreign objects. Otherwise, irreparable damage may occur.** |
|  | **Parts of the unit may become hot during operation. Take care not to touch any parts of the circuitry during operation to avoid burns and operate the unit in a well-ventilated location. Provide an appropriate cooling solution as required.** |
|  | **Electrostatic discharge (ESD) can damage the unit. Always take the necessary ESD precautions.**<br>**Many pins on the module connector are directly connected to the SOC or other ESD sensitive devices.**<br>**Make or break ANY connection ONLY while the unit is switched OFF.**<br>**Otherwise, permanent damage to the unit may occur, which is not covered by warranty.** |
|  | **There is no separate SHIELD connection.**<br>**The module's mounting holes are <u>not</u> connected to GND**<br>**Take this into account when handling and mounting the unit.** |

*Table 3 Safety and Handling Precautions*

# 2 Short Description

The miriac MPX-S32G274A is a member of the MPX module family based on NXP's S32G274A network processor (SoC).

MicroSys Electronics GmbH offers a Development Kit which uses the key features of the module. The customer can:

- …test the operation of the MPX-S32G274A module
- …evaluate the main interfaces of the S32G274A SoC
- …test the provided software
- …start developing

# 3 System Description

## 3.1 Block Diagram

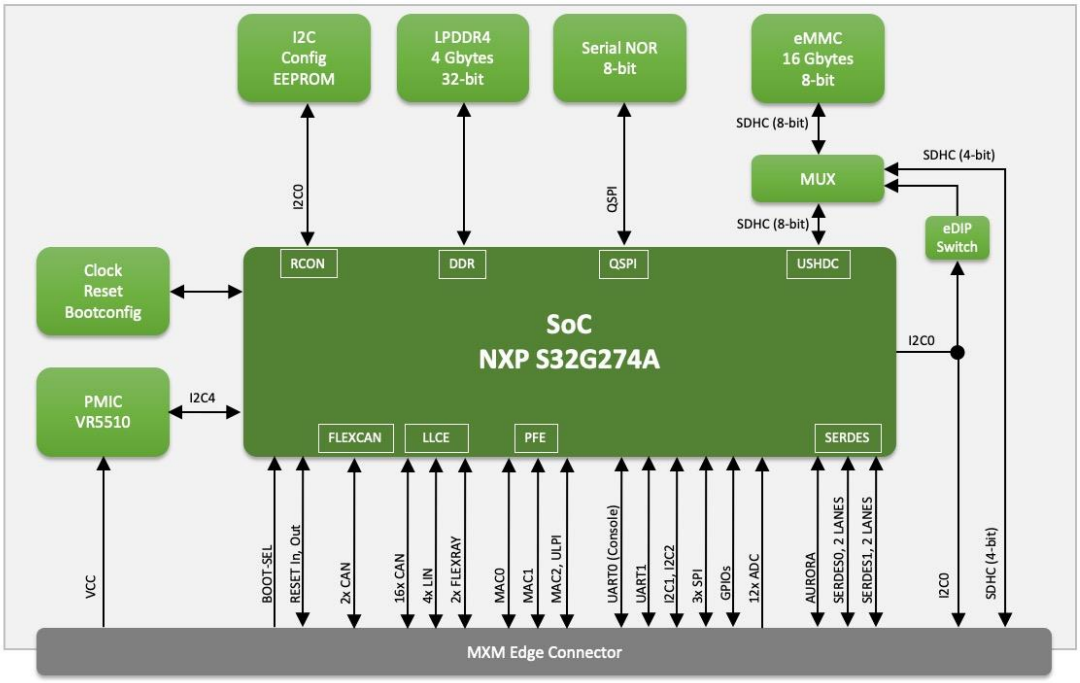


*Figure 3-1 Block Diagram*

## 3.2 System Components

- S32G274A SoC (4x Arm Cortex-A53 plus triple Cortex-M7 lockstep cores)
- 4GB LPDDR4 SDRAM
- Serial NOR flash as boot or storage device
- 16GB eMMC flash as boot or storage device
- Clock generators for SOC and interface clocks
- I²C EEPROM
- I²C temperature sensor
- I²C RTC
- Voltage regulators for onboard voltages

## 3.3 Ordering Information

Ordering information can be found on the following website

[miriac MPX-S32G274A]

or contact your local sales representative.

## 3.4 Power Consumption

The MPX-S32G274A is supplied by a single input power rail.

The typical power consumption values for the module are determined on a CRX-S32G carrier running U-Boot (idle) at room temperature with heatsink:

- S32G274A
- Cortex-A53 core frequency 1000 MHz
- 400 MHz bus clock
- 4 GBytes of LPDDR4 memory + ECC (1600 MHz)

| Nominal Input Power | Power Dissipation |
|---|---|
| 9V | 2.88 W |
| 12V | 2.95 W |
| 18V | 3.06 W |
| 24V | 3.36 W |
| 30V | 3.49 W |

*Table 4 Typical power consumption at U-Boot prompt*

The typical power consumption values for the module over junction temperature are determined on a CRX-S32G carrier running Linux based on BSP 31. Input voltage 12V with 4 times RJ45 1G Ethernet connected as well as console over USB.

Linux Stress: stressapptest (https://github.com/stressapptest/stressapptest) (start parameters: -W -s 60, all cores)

Linux Idle: command prompt

| $T_i$ [°C] from internal probe | Power dissipation idle [W] | Power dissipation stress [W] |
|---|---|---|
| -25 | 5,6 | 6,7 |
| -20 | 5,6 | 6,6 |
| 0 | 5,4 | 6,5 |
| 15 | 5,5 | 6,6 |
| 25 | 5,4 | 6,6 |
| 50 | 5,6 | 6,7 |

*Table 5 Typical power consumption running module with Linux*

## 3.5 Cooling

In chapter 3.4 the typical power consumption of the MPX-S32G274A module was specified. With this information a cooling method needs to be designed which considers the final use case. If desired, MicroSys Electronics GmbH can support

you with your cooling concept. Please ask your sales representative or send an email inquiry to support@microsys.de.

| Component | Temperature (max.) | Power Dissipation (max.) |
|---|---|---|
| SoC | $T_J$ = 125° C | 5.1 W |
| LPDDR4 | $T_C$ = 95° C | 0.4 W |
| eMMC | $T_C$ = 115° C | 0.62 W |

*Table 6 Maximum junction/case temperatures*


**Do not run the module without a heatsink or appropriate cooling concept**

# 4 Technical Description

## 4.1 Pinouts


**The signal direction is from the module's view. For example, PCIE0_TX0_N, pin T90, is an output from the module and an input to peripheral devices on the carrier.**

The following table gives an overview of the 314 pins of the module's edge finger. For a detailed connector description see chapter 5.1. The pins will be described in chapter 4.10 and the following sections.

The signal names in the following two tables do not show all available options for each pin. Pin multiplexing can only be implemented in combination with the vendor's datasheet.

### 4.1.1 Module Connector – Top Pins

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|---|---|---|---|
| T1 | GND | --- | --- |
| T2 | SD_CLK | --- | ✓ |
| T3 | GND | --- | --- |
| T4 | SD_CMD | --- | ✓ |
| T5 | GND | --- | --- |
| T6 | SD_D0 | --- | ✓ |
| T7 | SD_D1 | --- | ✓ |
| T8 | SD_D2 | --- | ✓ |
| T9 | SD_D3 | --- | ✓ |
| TK1 | VCC_SDHC_1V8/3V3 | --- | --- |
| TK2 | PMIC_FCCU1_OUT | --- | --- |
| T10 | GND | --- | --- |
| T11 | GND | --- | --- |
| T12 | RGMII2_MDC/DSPI0_CS7 | ✓ | ✓ |
| T13 | RGMII2_MDIO | ✓ | ✓ |
| T14 | GND | --- | --- |
| T15 | RGMII2_RXD3/USB_D7 | ✓ | ✓ |
| T16 | RGMII2_RXD2/USB_D6 | ✓ | ✓ |
| T17 | RGMII2_RXD1/USB_D5 | ✓ | ✓ |
| T18 | RGMII2_RXD0/USB_D4 | ✓ | ✓ |
| T19 | GND | --- | --- |
| T20 | RGMII2_RXDV/USB_D3 | ✓ | ✓ |

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|---|---|---|---|
| T21 | RGMII2_RX_CLK/USB_D2 | ✓ | ✓ |
| T22 | GND | --- | --- |
| T23 | RGMII2_TXD3/USB_D1 | ✓ | ✓ |
| T24 | RGMII2_TXD2/USB_D0 | ✓ | ✓ |
| T25 | RGMII2_TXD1/USB_NXT | ✓ | ✓ |
| T26 | RGMII2_TXD0/USB_STP | ✓ | ✓ |
| T27 | GND | --- | --- |
| T28 | RGMII2_TX_EN/USB_DIR | ✓ | ✓ |
| T29 | RGMII2_TX_CLK/USB_CLK | ✓ | ✓ |
| T30 | GND | --- | --- |
| T31 | RGMII1_MDC | ✓ | ✓ |
| T32 | RGMII1_MDIO | ✓ | ✓ |
| T33 | GND | --- | --- |
| T34 | RGMII1_RXD3 | ✓ | ✓ |
| T35 | RGMII1_RXD2 | ✓ | ✓ |
| T36 | RGMII1_RXD1 | ✓ | ✓ |
| T37 | RGMII1_RXD0 | ✓ | ✓ |
| T38 | GND | --- | --- |
| T39 | RGMII1_RXDV | ✓ | ✓ |
| T40 | RGMII1_RX_CLK | ✓ | ✓ |
| T41 | GND | --- | --- |
| T42 | RGMII1_TXD3 | ✓ | ✓ |
| T43 | RGMII1_TXD2 | ✓ | ✓ |
| T44 | RGMII1_TXD1 | ✓ | ✓ |
| T45 | RGMII1_TXD0 | ✓ | ✓ |
| T46 | GND | --- | --- |
| T47 | RGMII1_TX_EN | ✓ | ✓ |
| T48 | RGMII1_TX_CLK | ✓ | ✓ |
| T49 | GND | --- | --- |
| T50 | RGMII0_MDC | ✓ | ✓ |
| T51 | RGMII0_MDIO | ✓ | ✓ |
| T52 | GND | --- | --- |
| T53 | RGMII0_RXD3 | ✓ | ✓ |
| T54 | RGMII0_RXD2 | ✓ | ✓ |
| T55 | RGMII0_RXD1 | ✓ | ✓ |
| T56 | RGMII0_RXD0 | ✓ | ✓ |

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|---|---|---|---|
| T57 | GND | --- | --- |
| T58 | RGMII0_RXDV | ✓ | ✓ |
| T59 | RGMII0_RX_CLK | ✓ | ✓ |
| T60 | GND | --- | --- |
| T61 | RGMII0_TXD3 | ✓ | ✓ |
| T62 | RGMII0_TXD2 | ✓ | ✓ |
| T63 | RGMII0_TXD1 | ✓ | ✓ |
| T64 | RGMII0_TXD0 | ✓ | ✓ |
| T65 | GND | --- | --- |
| T66 | RGMII0_TX_EN | ✓ | ✓ |
| T67 | RGMII0_TX_CLK | ✓ | ✓ |
| T68 | GND | --- | --- |
| T69 | PCIE1_RX0_N | --- | --- |
| T70 | PCIE1_RX0_P | --- | --- |
| T71 | GND | --- | --- |
| T72 | PCIE1_RX1_N | --- | --- |
| T73 | PCIE1_RX1_P | --- | --- |
| T74 | GND | --- | --- |
| T75 | PCIE0_RX0_N | --- | --- |
| T76 | PCIE0_RX0_P | --- | --- |
| T77 | GND | --- | --- |
| T78 | PCIE0_RX1_N | --- | --- |
| T79 | PCIE0_RX1_P | --- | --- |
| T80 | GND | --- | --- |
| T81 | CLK_OUT_N | --- | --- |
| T82 | CLK_OUT_P | --- | --- |
| T83 | GND | --- | --- |
| T84 | PCIE1_TX0_N | --- | --- |
| T85 | PCIE1_TX0_P | --- | --- |
| T86 | GND | --- | --- |
| T87 | PCIE1_TX1_N | --- | --- |
| T88 | PCIE1_TX1_P | --- | --- |
| T89 | GND | --- | --- |
| T90 | PCIE0_TX0_N | --- | --- |
| T91 | PCIE0_TX0_P | --- | --- |
| T92 | GND | --- | --- |

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|---|---|---|---|
| T93 | PCIE0_TX1_N | --- | --- |
| T94 | PCIE0_TX1_P | --- | --- |
| T95 | GND | --- | --- |
| T96 | AUR_CLK_N | --- | --- |
| T97 | AUR_CLK_P | --- | --- |
| T98 | GND | --- | --- |
| T99 | AUR_TX2_N | --- | --- |
| T100 | AUR_TX2_P | --- | --- |
| T101 | GND | --- | --- |
| T102 | AUR_TX0_N | --- | --- |
| T103 | AUR_TX0_P | --- | --- |
| T104 | GND | --- | --- |
| T105 | AUR_TX1_N | --- | --- |
| T106 | AUR_TX1_P | --- | --- |
| T107 | GND | --- | --- |
| T108 | AUR_TX3_N | --- | --- |
| T109 | AUR_TX3_P | --- | --- |
| T110 | GND | --- | --- |
| T111 | PB02 | ✓ | ✓ |
| T112 | PB07 | ✓ | ✓ |
| T113 | PB08 | ✓ | ✓ |
| T114 | PB15 | ✓ | ✓ |
| T115 | PC00 | ✓ | ✓ |
| T116 | GND | --- | --- |
| T117 | +VREF1 | --- | --- |
| T118 | +VREF2 | --- | --- |
| T119 | +VREF3 | --- | --- |
| T120 | +VREF4 | --- | --- |
| T121 | GND | --- | --- |
| T122 | PCIE0_CLKIN_N | --- | --- |
| T123 | PCIE0_CLKIN_P | --- | --- |
| T124 | GND | --- | --- |
| T125 | NMI | --- | --- |
| T126 | PMIC_RST# | --- | --- |
| T127 | RSTIN# | --- | --- |
| T128 | RST# | --- | --- |

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|---|---|---|---|
| T129 | GND | --- | --- |
| T130 | SEL_CLK_RC/EP# | --- | --- |
| T131 | RCW_SEL# | --- | --- |
| T132 | MUX_SEL# | --- | --- |
| T133 | VCC_RTC | --- | --- |
| T134 | +3V3_EXT | --- | --- |
| T135 | I2C_SCL_PROG | --- | --- |
| T136 | I2C_SDA_PROG | --- | --- |
| T137 | GND | --- | --- |
| T138 | GND | --- | --- |
| T139 | GND | --- | --- |
| T140 | GND | --- | --- |
| T141 | GND | --- | --- |
| T142 | GND | --- | --- |
| T143 | GND | --- | --- |
| T144 | GND | --- | --- |
| T145 | GND | --- | --- |
| T146 | +VIN | --- | --- |
| T147 | +VIN | --- | --- |
| T148 | +VIN | --- | --- |
| T149 | +VIN | --- | --- |
| T150 | +VIN | --- | --- |
| T151 | +VIN | --- | --- |
| T152 | +VIN | --- | --- |
| T153 | +VIN | --- | --- |
| T154 | +VIN | --- | --- |

*Table 7 Module connector: top pins*

### 4.1.2 Module Connector – Bottom Pins

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|---|---|---|---|
| B1 | ADC_CH_11 | --- | --- |
| B2 | ADC_CH_10 | --- | --- |
| B3 | GND | --- | --- |
| B4 | ADC_CH_09 | --- | --- |
| B5 | ADC_CH_08 | --- | --- |
| B6 | GND | --- | --- |
| B7 | ADC_CH_07 | --- | --- |
| B8 | ADC_CH_06 | --- | --- |
| B9 | GND | --- | --- |
| BK1 | PMIC_STBY# | --- | --- |
| BK2 | PMIC_VDD_OK | --- | --- |
| B10 | ADC_CH_05 | --- | --- |
| B11 | ADC_CH_04 | --- | --- |
| B12 | GND | --- | --- |
| B13 | ADC_CH_03 | --- | --- |
| B14 | ADC_CH_02 | --- | --- |
| B15 | GND | --- | --- |
| B16 | ADC_CH_01 | --- | --- |
| B17 | ADC_CH_00 | --- | --- |
| B18 | GND | --- | --- |
| B19 | CAN00_RX | --- | ✓ (INPUT) |
| B20 | CAN00_TX | --- | ✓ |
| B21 | GND | --- | --- |
| B22 | CAN01_RX | --- | ✓ (INPUT) |
| B23 | CAN01_TX | --- | ✓ |
| B24 | GND | --- | --- |
| B25 | CAN02_RX | --- | ✓ (INPUT) |
| B26 | CAN02_TX | --- | ✓ |
| B27 | GND | --- | --- |
| B28 | CAN03_RX | --- | ✓ (INPUT) |
| B29 | CAN03_TX | --- | ✓ |
| B30 | GND | --- | --- |
| B31 | CAN04_RX | ✓ | ✓ (INPUT) |
| B32 | CAN04_TX | ✓ | ✓ |

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|---|---|---|---|
| B33 | GND | --- | --- |
| B34 | CAN05_RX | ✓ | ✓(INPUT) |
| B35 | CAN05_TX | ✓ | ✓ |
| B36 | GND | --- | --- |
| B37 | CAN06_RX | ✓ | ✓(INPUT) |
| B38 | CAN06_TX | ✓ | ✓ |
| B39 | GND | --- | --- |
| B40 | CAN07_RX | ✓ | ✓(INPUT) |
| B41 | CAN07_TX | ✓ | ✓ |
| B42 | GND | --- | --- |
| B43 | CAN08_RX | ✓ | ✓(INPUT) |
| B44 | CAN08_TX | ✓ | ✓ |
| B45 | GND | --- | --- |
| B46 | CAN09_RX | ✓ | ✓(INPUT) |
| B47 | CAN09_TX | ✓ | ✓ |
| B48 | GND | --- | --- |
| B49 | CAN10_RX | ✓ | ✓(INPUT) |
| B50 | CAN10_TX | ✓ | ✓ |
| B51 | GND | --- | --- |
| B52 | CAN11_RX | ✓ | ✓(INPUT) |
| B53 | CAN11_TX | ✓ | ✓ |
| B54 | GND | --- | --- |
| B55 | CAN12_RX | ✓ | ✓(INPUT) |
| B56 | CAN12_TX | ✓ | ✓ |
| B57 | GND | --- | --- |
| B58 | CAN13_RX | ✓ | ✓(INPUT) |
| B59 | CAN13_TX | ✓ | ✓ |
| B60 | GND | --- | --- |
| B61 | CAN14_RX | ✓ | ✓(INPUT) |
| B62 | CAN14_TX | ✓ | ✓ |
| B63 | GND | --- | --- |
| B64 | CAN15_RX | ✓ | ✓(INPUT) |
| B65 | CAN15_TX | ✓ | ✓ |
| B66 | GND | --- | --- |
| B67 | PA15_DSPI0_SOUT | ✓ | ✓ |
| B68 | PA13_DSPI0_SCK | ✓ | ✓ |

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|---|---|---|---|
| B69 | PA14_DSPI0_SIN | ✓ | ✓ |
| B70 | PB09_DSPI0_CS1 | ✓ | ✓ |
| B71 | PB10_DSPI0_CS2 | ✓ | ✓ |
| B72 | GND | --- | --- |
| B73 | PA06_DSPI1_SOUT | ✓ | ✓ |
| B74 | PA08_DSPI1_SCK | ✓ | ✓ |
| B75 | PF15_DSPI1_SIN | ✓ | ✓ |
| B76 | PA07_DSPI1_CS0 | ✓ | ✓ |
| B77 | GND | --- | --- |
| B78 | PA11_DSPI5_SOUT | ✓ | ✓ |
| B79 | PA09_DSPI5_SCK | ✓ | ✓ |
| B80 | PA10_DSPI5_SIN | ✓ | ✓ |
| B81 | PA12_DSPI5_CS0 | ✓ | ✓ |
| B82 | JTAG_TCK | --- | ✓ |
| B83 | JTAG_TDO | --- | ✓ |
| B84 | JTAG_TDI | --- | ✓ |
| B85 | JTAG_TMS | --- | ✓ |
| B86 | JCOMP | --- | --- |
| B87 | GND | --- | --- |
| B88 | PF03_CLKOUT0 | --- | ✓ |
| B89 | PF04_CLKOUT1 | --- | ✓ |
| B90 | GND | --- | --- |
| B91 | FLXR0A_RX_D | ✓ | ✓ |
| B92 | FLXR0A_TX_D | ✓ | ✓ |
| B93 | FLXR0A_TXEN# | ✓ | ✓ |
| B94 | GND | --- | --- |
| B95 | FLXR0B_RX_D | ✓ | ✓ |
| B96 | FLXR0B_TX_D | ✓ | ✓ |
| B97 | FLXR0B_TXEN# | ✓ | ✓ |
| B98 | GND | --- | --- |
| B99 | PB12_FXCAN2_RX | ✓ | ✓ |
| B100 | PB11_FXCAN2_TX | ✓ | ✓ |
| B101 | GND | --- | --- |
| B102 | PB14_FXCAN3_RX | ✓ | ✓ |
| B103 | PB13_FXCAN3_TX | ✓ | ✓ |
| B104 | GND | --- | --- |

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|---|---|---|---|
| B105 | LIN0_RX | --- | ✓(INPUT) |
| B106 | LIN0_TX | ✓ | ✓ |
| B107 | GND | --- | --- |
| B108 | LIN1_RX | ✓ | ✓(INPUT) |
| B109 | LIN1_TX | ✓ | ✓ |
| B110 | GND | --- | --- |
| B111 | LIN2_RX | ✓ | ✓(INPUT) |
| B112 | LIN2_TX | ✓ | ✓ |
| B113 | GND | --- | --- |
| B114 | LIN3_RX | --- | ✓(INPUT) |
| B115 | LIN3_TX | ✓ | ✓ |
| B116 | GND | --- | --- |
| B117 | PCIE1_CLKC_N | --- | --- |
| B118 | PCIE1_CLKC_P | --- | --- |
| B119 | GND | --- | --- |
| B120 | PCIE0_CLKC_N | --- | --- |
| B121 | PCIE0_CLKC_P | --- | --- |
| B122 | GND | --- | --- |
| B123 | PMIC_FSOUT# | --- | --- |
| B124 | PMIC_FIN | --- | --- |
| B125 | VDD_OTP | --- | --- |
| B126 | PMIC_PWRON1 | --- | --- |
| B127 | PMIC_PSYNC | --- | --- |
| B128 | PMIC_FOUT/AMUX | --- | --- |
| B129 | GND | --- | --- |
| B130 | PC09_UART0_TX | ✓ | ✓ |
| B131 | PC10_UART0_RX | ✓ | ✓ |
| B132 | GND | --- | --- |
| B133 | PB01_I2C0_SCL | ✓ | ✓ |
| B134 | PB00_I2C0_SDA | ✓ | ✓ |
| B135 | PB03_I2C1_SCL | ✓ | ✓ |
| B136 | PB04_I2C1_SDA | ✓ | ✓ |
| B137 | PB05_I2C2_SCL | ✓ | ✓ |
| B138 | PB06_I2C2_SDA | ✓ | ✓ |
| B139 | GND | --- | --- |
| B140 | GND | --- | --- |

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|---|---|---|---|
| B141 | GND | --- | --- |
| B142 | GND | --- | --- |
| B143 | GND | --- | --- |
| B144 | GND | --- | --- |
| B145 | GND | --- | --- |
| B146 | GND | --- | --- |
| B147 | GND | --- | --- |
| B148 | +VIN | --- | --- |
| B149 | +VIN | --- | --- |
| B150 | +VIN | --- | --- |
| B151 | +VIN | --- | --- |
| B152 | +VIN | --- | --- |
| B153 | +VIN | --- | --- |
| B154 | +VIN | --- | --- |
| B155 | +VIN | --- | --- |
| B156 | +VIN | --- | --- |

*Table 8 Module connector: bottom pins*

## 4.2 Power Structure

The MPX-S32G274A module is supplied by a single 9-30V supply. Onboard voltages are generated by the PMIC VR5510.

For RTC backup buffering an additional supply from the carrier is necessary.

The module itself does not provide any supply voltage to the carrier but it has some reference voltages that show the voltage level of the respective interface on the module. If necessary, the carrier must track the reference voltages and generate a copy which can carry higher loads.

The following diagram shows the structure of the power supplies:

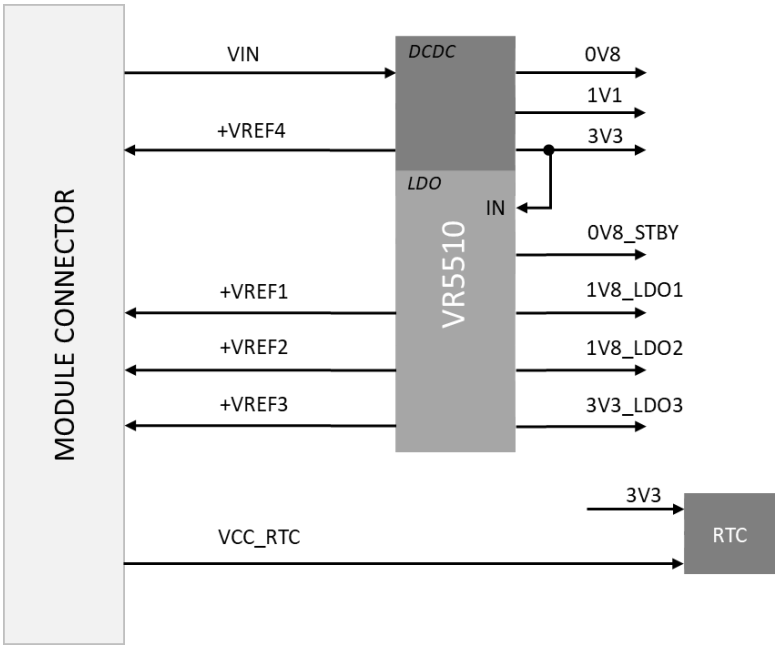


*Figure 4-1 Power supplies: structure*

The following table shows the internal connections:

| Module Connector | | | |
|---|---|---|---|
| **Pin** | **Signal** | **I/O Range** | **Description** |
| T146-T154 / B148-B156 | VIN | 9-30V | Module supply input |
| T117 | +VREF1 | 1.8V | Reference voltage output |
| T118 | +VREF2 | 1.8V | Reference voltage output |
| T119 | +VREF3 | 3.3V | Reference voltage output |
| T120 | +VREF4 | 3.3V | Reference voltage output |
| T133 | VCC_RTC | 0.9V-5.5V | Optional backup supply |
| T134 | +3V3_EXT | 3.3V | Optional boot EEPROM programming supply input |
| B125 | VDD_OTP | N/A | Do not connect |

*Table 9 Module connector: power pin assignments*

## 4.3 Reset Structure

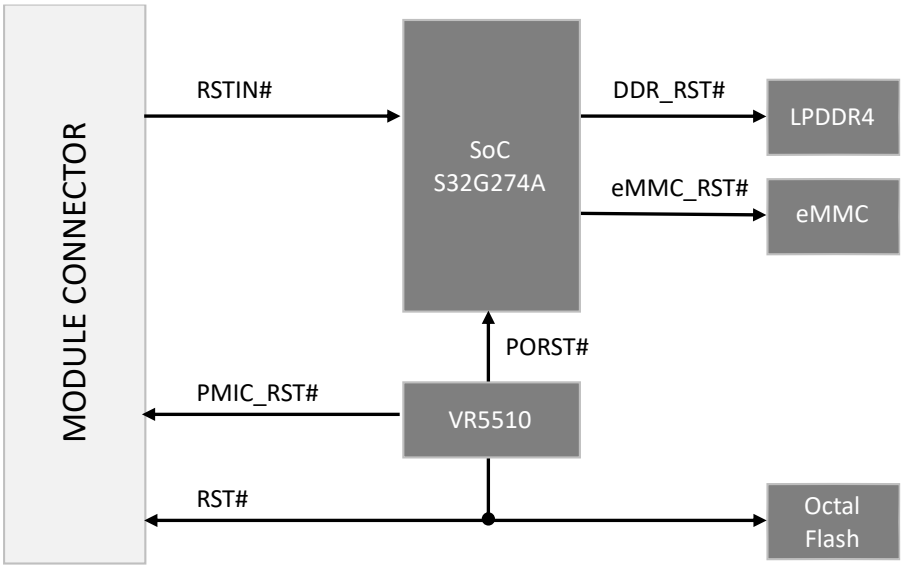


*Figure 4-2 Reset Structure*

The reset structure of the MPX-S32G274A module is shown in Figure 4-2. The board resets are controlled by the system power management chip (PMIC) VR5510.

When the onboard voltages of the module are within their limits, the power good signal in combination with the RSTIN# signal will release the PORST# of the SoC. The PMIC_RST# controls both the SoC and peripheral devices. PMIC_RST# and RST# are identical signals. The only difference is that RST# could be disconnected by a zero-ohm resistor.

The S32G274A provides dedicated reset signals for eMMC and LPDDR4 memories.

| Signal Name | Function | Type |
|---|---|---|
| RSTIN# | System Global Reset Input | 100R series resistance / 10nF / 4k7 Pullup |
| RST# | System Global Reset Output | Open Drain |
| PMIC_RST# | System Global Reset Output | Open Drain |
| PORST# | Power-On Reset for SoC | |
| DDR_RST# | Reset for LPDDR Memory | |
| EMMC_RST# | Reset for eMMC Memory | |

*Table 4-3 Reset signal overview*

## 4.4 Clock Structure

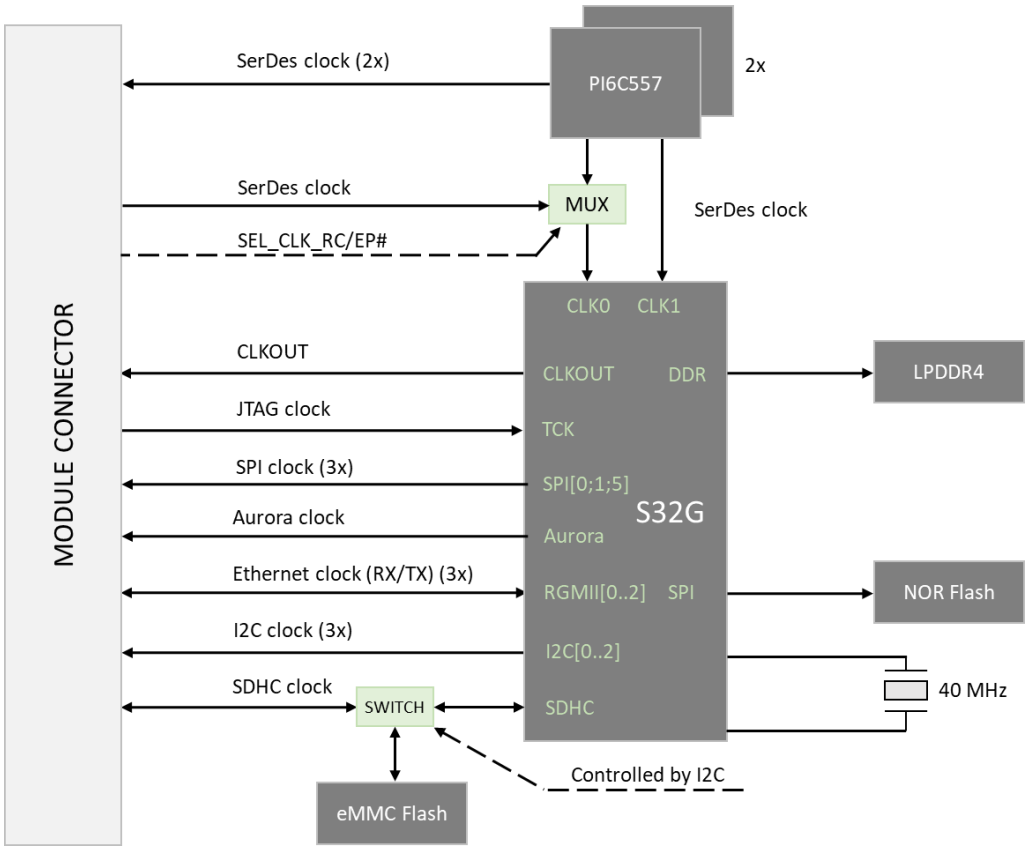


*Figure 4-3 Clock Structure*

The S32G274A offers two SerDes channels with four lanes in total which can be configured as PCIe or SGMII. In order to be compliant with the NXP documentation they are referred to as “PCIE0” and “PCIE1”.

Each SerDes channel requires a clock which can be configured as 100MHz or 125MHz clock depending on PCIe or SGMII use.

| J12 (PI6C557) | | | S32G274A “PCIE0” channel | | | | |
|---|---|---|---|---|---|---|---|
| **Pin** | **Signal** | | **Pin** | **Signal** | **I/O Range** | **Signal conditioning** | **Frequency** |
| 15 | CLK0+ | → | AB15 | PCIE0_CLK_P | HCSL | SR: 33R<br>PD: 49R9 | 100/125 MHz |
| 14 | CLK0- | → | AC15 | PCIE0_CLK_N | HCSL | SR: 33R<br>PD: 49R9 | 100/125 MHz |

| J12 (PI6C557) | | | Module Connector | | | | |
|---|---|---|---|---|---|---|---|
| Pin | Signal | | Pin | Signal | I/O Range | Signal conditioning | Frequency |
| 11 | CLK1+ | → | B121 | PCIE0_CLKC_P | HCSL | SR: 33R<br>PD: 49R9 | 100/125 MHz |
| 10 | CLK1- | → | B120 | PCIE0_CLKC_N | HCSL | SR: 33R<br>PD: 49R9 | 100/125 MHz |

*Table 10 PCIE0 clock: pin assignments*

Channel 0 can also be configured as a PCIe Endpoint. In this case the SoC can be fed with an external clock from the carrier:

| S32G274A | | | Module Connector | | | | |
|---|---|---|---|---|---|---|---|
| Ball | Signal | | Pin | Signal | I/O Range | Signal conditioning | Frequency |
| AB15 | PCIE0_CLK_P | ← | T123 | PCIE0_CLKIN_P | HCSL | | 100 MHz |
| AC15 | PCIE0_CLK_N | ← | T122 | PCIE0_CLKIN_N | HCSL | | 100 MHz |

*Table 11 PCIe clock for endpoint configuration*

Channel 1 is fed from J16:

| J16 (PI6C557) | | | Module Connector | | | | |
|---|---|---|---|---|---|---|---|
| Pin | Signal | | Pin | Signal | I/O Range | Signal conditioning | Frequency |
| 15 | CLK0+ | → | B121 | PCIE1_CLKC_P | HCSL | SR: 33R<br>PD: 49R9 | 100/125 MHz |
| 14 | CLK0- | → | B120 | PCIE1_CLKC_N | HCSL | SR: 33R<br>PD: 49R9 | 100/125 MHz |

| J16 (PI6C557) | | | Module Connector | | | | |
|---|---|---|---|---|---|---|---|
| Pin | Signal | | Pin | Signal | I/O Range | Signal conditioning | Frequency |
| 11 | CLK1+ | → | AB16 | PCIE1_CLK_P | HCSL | SR: 33R<br>PD: 49R9 | 100/125 MHz |
| 10 | CLK1- | → | AC16 | PCIE1_CLK_N | HCSL | SR: 33R<br>PD: 49R9 | 100/125 MHz |

*Table 12 PCIE1 clock: pin assignments*

The following table shows the available clocks configured as primary interface on the MPX-S32G274A:

| S32G274A | | | Module Connector | | | | |
|---|---|---|---|---|---|---|---|
| **Ball** | **Signal** | | **Pin** | **Signal** | **I/O Range** | **Signal conditioning** | **Frequency** |
| E19 | SD0_CLK | → | T2 | SD_CLK | +VREF3 | SR: 22R | t.b.d |
| U12 | DSPI0_SCK | → | B68 | PA13_DSPI0_SCK | +VREF3 | | t.b.d |
| U10 | DSPI1_SCK | → | B74 | PA08_DSPI1_SCK | +VREF3 | | t.b.d |
| B8 | DSPI5_SCK | → | B79 | PA09_DSPI5_SCK | +VREF3 | | t.b.d |
| E7 | I2C0_SCL | → | B133 | PB01_I2C0_SCL | +VREF3 | PU: 2k7 | 400 kHz |
| C6 | I2C1_SCL | → | B135 | PB03_I2C1_SCL | +VREF3 | PU: 4k7 | 400 kHz |
| A6 | I2C2_SCL | → | B137 | PB05_I2C2_SCL | +VREF3 | PU: 4k7 | 400 kHz |
| AC13 | CLKOUT_P | → | T82 | CLK_OUT_P | +VREF1 | SR: 0R | |
| AB13 | CLKOUT_N | → | T81 | CLK_OUT_N | +VREF1 | SR: 0R | |
| AC11 | AUR_CLK_P | ← | T97 | AUR_CLK_P | +VREF1 | | t.b.d. |
| AB11 | AUR_CLK_N | ← | T96 | AUR_CLK_N | +VREF1 | | t.b.d. |
| W9 | TCK | ← | B82 | JTAG_TCK | +VREF3 | PD: 10k | t.b.d. |
| V20 | RGMII0_TX_CLK | → | T67 | RGMII0_TX_CLK | +VREF1 | SR: 10R | 125 MHz |
| V21 | RGMII0_RX_CLK | ← | T59 | RGMII0_RX_CLK | +VREF1 | SR: 10R | 125 MHz |
| Y21 | RGMII0_MDC | → | T50 | RGMII0_MDC | +VREF1 | SR: 10R | < 10 MHz. |
| P20 | RGMII1_TX_CLK | → | T48 | RGMII1_TX_CLK | +VREF1 | SR: 10R | 125 MHz |
| R21 | RGMII1_RX_CLK | ← | T40 | RGMII1_RX_CLK | +VREF1 | SR: 10R | 125 MHz |
| V23 | RGMII1_MDC | → | T31 | RGMII1_MDC | +VREF1 | SR: 10R | < 10 MHz |
| N19 | RGMII2_TX_CLK | → | T29 | RGMII2_TX_CLK | +VREF2 | SR: 10R | 125 MHz |
| P21 | RGMII2_RX_CLK | ← | T21 | RGMII2_RX_CLK | +VREF2 | SR: 10R | 125 MHz |
| M19 | RGMII2_MDC | → | T12 | RGMII2_MDC | +VREF2 | SR: 10R | < 10 MHz |

*Table 13 Clock: pin assignments*

## 4.5 Boot Mode Configuration

The MPX-S32G274A module offers several different boot modes to choose from. The settings can be done via the electronic DIP switch J8 on the module and two signals on the module connector in case the FUSE_SEL fuse is not blown.

The S32G274A can retrieve the boot configuration (abbreviated: BOOT_CFG) either from fuses or from a serial EEPROM. This latter mode is called “Serial RCON” mode. “Parallel RCON” mode is not supported by the MPX-S32G274A module.

*FUSE_SEL = 0*

| BOOTMOD0 (ball W10) | BOOTMOD1 (ball W11) | Ethernet boot config | Boot Mode |
|---|---|---|---|
| 0 | 0 | No Ethernet | Serial Boot |
| 0 | 1 | SGMII | Serial Boot |
| 1 | 0 | | RCON |
| 1 | 1 | | Reserved |

*Table 14 Boot mode settings (no fuse)*

*FUSE_SEL = 1*

| BOOTMOD0 (ball W10) | BOOTMOD1 (ball W11) | Ethernet boot config | Boot Mode |
|---|---|---|---|
| 0 | 0 | | Fuses |
| 0 | 1 | | |
| 1 | 0 | | Serial Boot |
| 1 | 1 | | Reserved |

*Table 15 Boot mode settings (fuses)*

In Serial RCON mode the BOOT_CFG bits are mapped to the EEPROM.

BOOT_CFG1[7:5] configures the boot devices:

| BOOT_CFG1[7:5] | Boot Source | Description | Boot Location |
|---|---|---|---|
| *000* | QuadSPI Boot | Quad/Hyper/Octal Flash (see BOOT_CFG[4:2]) | Module |
| *010* | SD Boot | SD Card | Carrier |
| *011* | eMMC Boot | eMMC | Module |

*Table 16 Boot devices*

## 4.6 LEDs

There are four LEDs on the bottom side of the MPX-S32G274A module. The side-looker LEDs are placed near the edge of the PCB.

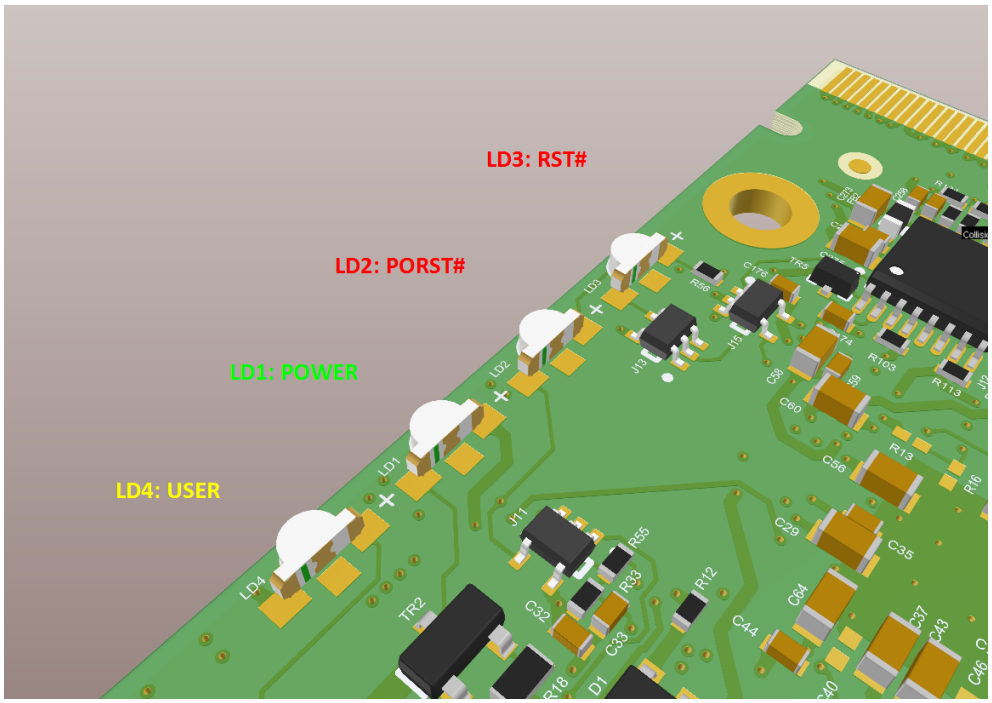


*Figure 4-4 LEDs*

| Reference | Colour | Function | |
|---|---|---|---|
| LD1 | Green | LED ON: | Power-up sequence of the module is finished, power is good |
| | | LED OFF: | Power fail |
| LD2 | Red | LED ON: | SoC Power-on-reset is active |
| | | LED OFF: | Reset is inactive |
| LD3 | Red | LED ON: | Peripheral reset is active |
| | | LED OFF: | Reset is inactive |
| LD4 | Yellow | LED ON: | User defined function |
| | | LED OFF: | User defined function |

*Table 17 LED: pin description*

## 4.7 RTC

The Real-Time Clock (RTC) is implemented with an NXP PCF85263ATL chip:

- I²C clock frequency up to 400 kHz
- Operating temperature -40°C to 85°C
- Slave address according to Table 29

The RTC is supplied by 3.3V (reference voltage: +VREF4). Backup voltage is optional and needs to be provided from the carrier if buffering is desired. The following table shows the internal connection:

| Module Connector | | | |
|---|---|---|---|
| **Pin** | **Signal** | **I/O Range** | **Description** |
| T133 | VCC_RTC | 0.9V – 5.5V | Battery backup voltage provided by the carrier |

*Table 18 RTC: backup voltage*

The RTC's interrupt output is connected to the GPIO Expander:

| GPIO Expander | | | PCF85263ATL | | | |
|---|---|---|---|---|---|---|
| **Pin** | **Signal** | | **Pin** | **Signal** | **I/O Range** | **Signal conditioning** |
| 8 | RTC_IRQA# | ← | 9 | INTA# | +VREF3 | PU: 4k7 |
| 7 | RTC_IRQB# | ← | 4 | INTB# | +VREF3 | PU: 4k7 |

*Table 19 RTC: IRQs*

## 4.8 Temperature sensor

The S32G274A has an integrated temperature diode which is connected to a TMP451 temperature sensor from Texas Instruments.

- I²C clock frequency up to 400 kHz
- Operating temperature -40°C to 125°C
- Slave address according to Table 29
- Local temperature monitoring (TMP451's internal temperature)
- Remote temperature monitoring (S32G274A's temperature diode)
- Two interrupts for adjusting two temperature thresholds

| | Ambient: 0°C / +70°C | Ambient: -40°C / +125°C |
|---|---|---|
| **Local Temperature (of the sensor itself)** | Max. ± 1°C | Max. ± 2°C |
| **Remote Temperature (of the SoC internal diode)** | Max. ± 1°C | Max. ± 4°C |

*Figure 4-5 Temperature sensor: accuracy*

The temperature sensor provides two interrupts which are connected to the GPIO Expander:

| GPIO Expander | | | TMP451 | | | |
|---|---|---|---|---|---|---|
| **Pin** | **Signal** | | **Pin** | **Signal** | **I/O Range** | **Signal conditioning** |
| 12 | THERM_ALERT# | ← | 6 | ALERT#/THERM2 | +VREF3 | PU: 4k7 |
| 11 | THERM_FAULT# | ← | 4 | THERM# | +VREF3 | PU: 4k7 |

*Table 20 Temperature sensor: IRQs*

## 4.9 GPIO Expander

The scope of functions on the S32G274A is extended by a GPIO expander FXL6408:

- I²C clock frequency up to 400 kHz
- Slave address according to Table 29
- One interrupt out signaling pin state changes

It has 8 GPIOs which are used as follows:

| GPIO Expander | | | | | | |
|---|---|---|---|---|---|---|
| **Pin** | **Signal** | | | **Pin** | **Signal** | **Signal conditioning** |
| 12 | GPIO0 | ← | J19 | 6 | THERM_ALERT# | PU: 10k |
| 11 | GPIO1 | ← | J19 | 4 | THERM_FAULT# | PU: 10k |
| 8 | GPIO2 | ← | J21 | 9 | RTC_IRQA# | PU: 10k |
| 7 | GPIO3 | ← | J21 | 4 | RTC_IRQB# | PU: 10k |
| 6 | GPIO4 | ← | LD4 | | USER_LED | PU: 10k |
| 5 | GPIO5 | ← | --- | --- | HW_REV2 | See Table 22 |
| 4 | GPIO6 | ← | --- | --- | HW_REV1 | |
| 3 | GPIO7 | ← | --- | --- | HW_REV0 | |

*Table 21 GPIO Expander: Pin description*

| HW_REV2 | HW_REV1 | HW_REV0 | Description |
|---|---|---|---|
| 0 | 0 | 0 | Hardware Revision 1 |
| 0 | 0 | 1 | Hardware Revision 2 |
| 0 | 1 | 0 | Hardware Revision 3 |
| 0 | 1 | 1 | Hardware Revision 4 |
| 1 | 0 | 0 | Hardware Revision 5 |
| 1 | 0 | 1 | Hardware Revision 6 |
| 1 | 1 | 0 | Hardware Revision 7 |
| 1 | 1 | 1 | Hardware Revision 8 |

*Table 22 GPIO Expander: Hardware Revision*

| S32G274A | | | GPIO Expander | | |
|---|---|---|---|---|---|
| **Ball** | **Signal** | | **Pin** | **Signal** | **Signal conditioning** |
| Y7 | PC13 | ← | 1 | EXPD_IRQ# | PU: 10k |

*Table 23 GPIO Expander: IRQ*

## 4.10 Serial Boot EEPROM (RCON)

In chapter 4.5 the boot modes were described. Two EEPROMs are installed on the module to store the settings for Serial RCON mode. Serial RCON mode always uses I2C0 on address 0x50 to load the board configuration.

The second EEPROM is accessible on address 0x56.

The addresses of the two EEPROMs can be swapped, thus each EEPROM can be used to load the board configuration. Swapping is achieved with the RCW_SEL# signal from the carrier.

According to Table 16 more than two boot devices are supported. J4 is classified as primary EEPROM to store the boot configuration for SD card boot mode and it can also be write protected (see chapter 4.11). J14 is the secondary EEPROM used for any other boot configuration than SD card boot mode. J14 is not write protected. The code can be loaded by the user, stored in the EEPROM and selected via the carrier.


**If the FUSE_SEL fuse is blown the SoC will always boot from fuses (FUSE_SEL = 1).**

| FUSE_SEL | MUX_SEL# | SD / eMMC MUX (SEL_EMMC_SDHC#) | RCW_SEL# | Description | |
|---|---|---|---|---|---|
| **0** | 0 | SD card | 0 | Boot from J14 configuration | |
| | | | 1 | Boot from J4 configuration | |
| | 1 | DIP Switch:<br>• SD-Card<br>• eMMC | 0 | Boot from J14 configuration | |
| | | | 1 | Boot from J4 configuration | |
| **1** | 0 | SD card | **X** | **FUSES** | SD-Card |
| | 1 | DIP Switch:<br>• SD-Card<br>• eMMC | | | • SD-Card<br>• eMMC<br>• SPI NOR |

*Table 24 Boot configuration*

## 4.11 Electronic DIP Switch

The electronic DIP switch replaces mechanical DIP switches which can be serviced by a human operator only. The electronic DIP switch is accessed via I2C interface instead (slave address according to Table 29) and provides six persistent output signals to configure the module.

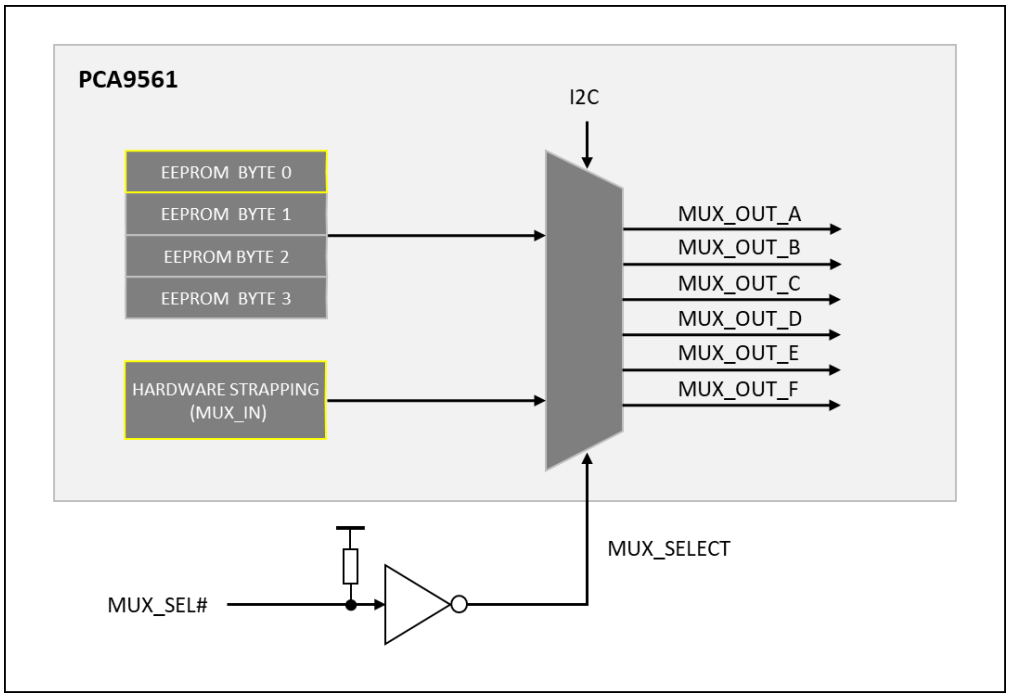


*Figure 4-6 Electronic DIP Switch: Structure*

At power up the values at MUX_OUT_x pins are either loaded from EEPROM Byte0 or MUX_IN hardware strapping inputs depending on the MUX_SELECT input pin of the PCA9561.

| MUX_SEL# | MUX_SELECT | |
|---|---|---|
| 1 (DEFAULT) | 0 | MUX_OUT = EEPROM BYTE 0 |
| 0 | 1 | MUX_OUT = MUX_IN |

*Table 25 Electronic DIP Switch: MUX_OUT after POR*

Initial EEPROM programming is done during production test and can be overridden via I2C.

| DIP Switch | | | Module Connector | | | |
|---|---|---|---|---|---|---|
| Pin | Signal | | Pin | Signal | I/O Range | Signal conditioning |
| 11 | MUX_SELECT | ← | T132 | MUX_SEL# | +3V3_EXT | PU: 10k |

*Table 26 Electronic DIP Switch: MUX_SELECT*

| MUX _OUT_ | Signal Name | MUX _IN | | Description |
|---|---|---|---|---|
| A | CLKGEN1_100M/125M# | 1 | 1 | PCIE0_CLK_P/N = 100 MHz (SoC PLL)<br>PCIE0_CLKC_P/N = 100 MHz (ST1: B120 / B121) |
| | | | 0 | PCIE0_CLK_P/N = 125 MHz (SoC PLL)<br>PCIE0_CLKC_P/N = 125 MHz (ST1: B120 / B121) |
| B | CLKGEN2_100M/125M# | 1 | 1 | PCIE1_CLK_P/N = 100 MHz (SoC PLL)<br>PCIE1_CLKC_P/N = 100 MHz (ST1: B117 / B118) |
| | | | 0 | PCIE1_CLK_P/N = 125 MHz (SoC PLL)<br>PCIE1_CLKC_P/N = 125 MHz (ST1: B117 / B118) |
| C | RCON_EEPROM_WP | 1 | 1 | Serial RCON EEPROM J4 write-protected |
| | | | 0 | Serial RCON EEPROM J4 unprotected |
| D | SEL_EMMC_SDHC# | 0 | 1 | Multiplexer: eMMC selected |
| | | | 0 | Multiplexer: SD card selected |
| E | PA02_BOOTMOD1 | 1 | 1 | Bootmode Pin 1 (J1: W10) = 1 |
| | | | 0 | Bootmode Pin 1 (J1: W10) = 0 |
| F | PA03_BOOTMOD2 | 0 | 1 | Bootmode Pin 2 (J1: W11) = 1 |
| | | | 0 | Bootmode Pin 2 (J1: W11) = 0 |

*Table 27 Electronic DIP Switch: MUX_IN / MUX_OUT*

## 4.12 Interface Description

In the following chapters the interfaces of the MPX-S32G274A module are described.


**Due to pin multiplexing there may be limitations regarding the availability of certain interfaces. Nevertheless, different pinouts are possible.**

### 4.12.1 Definition of “Primary Interfaces”

The terms “primary”, “secondary”, … do not imply any priority. The connector’s pin names are derived from the primary functions defined by MicroSys.

Primary interfaces can be also be configured for other interfaces. Nevertheless, high speed interfaces are optimized in layout, signals are length and often group matched. Multiplexing information for each pin can be found in the manufacturer’s datasheet, some signals are used onboard (see chapter 10.6).

### 4.12.2 JTAG

The JTAG chain of the MPX-S32G274A includes the S32G274A processor only. The JTAG port is directly connected to the MXM module connector. The JTAG interface can also be configured as GPIO.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

Some debuggers require a 10k pullup on TDI and TDO pins. These are not assembled on the module and may be provided externally for debugging.

### 4.12.3 AURORA

The Aurora port is a trace port consisting of 4 LVDS data pairs and a LVDS clock pair. The signals are available on the module connector as primary interface with no multiplexing options.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

### 4.12.4 ADC

The ADC converter contained in the S32G274A processor has 12 multiplexed single-ended channels. They can be accessed via the MXM module connector and do not share their pins with other interfaces.

The pins are listed in the Appendix in chapter 10.4 and 10.5.


**There is no protection on any ADC line against over-voltage or wrong polarity. Refer to the S32G274A datasheet for maximum ratings.**

### 4.12.5 CAN

The S32G274A has 4 FlexCANs and 16 LLCE CANs. Due to pin multiplexing there are limitations.

The MPX-S32G274A module realizes 18 CAN ports as primary interfaces on the module connector, two FlexCANs and 16 LLCE CANs. The ports support CAN2.0 version B and CAN FD protocols at data rates up to 8Mb/s. CAN transceivers are not installed on the module.

The CAN interfaces can also be configured as GPIO.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

### 4.12.6 RGMII

The S32G274A provides MACs for three RGMII interfaces, each RGMII port has a dedicated MDIO interface.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

RGMII2 is also shared with an ULPI interface for USB PHYs:

| Module Connector | RGMII | ULPI |
|---|---|---|
| T15 | RGMII2_RXD3 | USB_D7 |
| T16 | RGMII2_RXD2 | USB_D6 |
| T17 | RGMII2_RXD1 | USB_D5 |
| T18 | RGMII2_RXD0 | USB_D4 |
| T20 | RGMII2_RXDV | USB_D3 |
| T21 | RGMII2_RX_CLK | USB_D2 |
| T23 | RGMII2_TXD3 | USB_D1 |
| T24 | RGMII2_TXD2 | USB_D0 |
| T25 | RGMII2_TXD1 | USB_NXT |
| T26 | RGMII2_TXD0 | USB_STP |
| T28 | RGMII2_TX_EN | USB_DIR |
| T29 | RGMII2_TX_CLK | USB_CLK |

*Table 28 RGMII2 / ULPI pin multiplexing options*

### 4.12.7 ULPI (USB)

The MPX-S32G274A does not have a USB PHY but a ULPI interface. The ULPI signals are not available as primary interface on the module connector but they are shared with RGMII signals. For more details please see chapter 4.12.6.

The ULPI interface can also be configured as GPIO.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

### 4.12.8 I2C

The MPX-S32G274A module offers five I²C busses which run at up to 400kHz.

I2C3 is not available as primary interface.

I2C4 is explicitly used for the power management chip on the module.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

I2C0 map:

| Device | | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | Addr |
|---|---|---|---|---|---|---|---|---|---|---|
| GPIO Expander | FXL6408 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1/0 | 0x43 |
| Temperature Sensor | TMP451AIDQF (slave address) | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1/0 | 0x4C |
| | TMP451 (General Call reset address) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | -/0 | 0x00 |
| DIP Switch | PCA9561PW | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1/0 | 0x4D |
| EEPROM | AT24C01C-SSHM | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1/0 | 0x50 |
| RTC | PCF85263ATL | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1/0 | 0x51 |
| EEPROM | BR24G128NUX-3 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1/0 | 0x54 |
| EEPROM | AT24C01C-SSHM | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1/0 | 0x56 |

*Table 29 I2C0: bus map*

I2C1 map:

| Device | | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | Addr |
|---|---|---|---|---|---|---|---|---|---|---|
| --- | --- | - | - | - | - | - | - | - | - | - |

*Table 30 I2C1: bus map*

I2C2 map:

| Device | | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | Addr |
|---|---|---|---|---|---|---|---|---|---|---|
| --- | --- | - | - | - | - | - | - | - | - | - |

*Table 31 I2C2: bus map*


**I2C 3 is available by multiplexing functions. Primary interface is FlexCAN3.**

I2C4 map:

| Device | | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | Addr |
|---|---|---|---|---|---|---|---|---|---|---|
| PMIC | VR5510 Main logic | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1/0 | 0x20 |
| PMIC | VR5510 Fail-safe logic | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1/0 | 0x21 |

*Table 32 I2C4: bus map*

### 4.12.9 QSPI (Flash)

The MPX-S32G274A uses the QSPI port A to connect a serial NOR lash (8-bit bus).

The following table shows the internal connections:

| S32G274A | | | SPI NOR Flash MT35XU512ABA1G12 | | |
|---|---|---|---|---|---|
| **Ball** | **Signal** | | **Pin** | **Signal** | **I/O Range** |
| G21 | QSPI1_A_CS0# | → | C2 | CS# | 1.8V |
| K20 | QSPI1_A_SCK | → | B2 | CLK | 1.8V |
| K23 | QSPI_A_DQS | ← | C3 | DQS | |
| | | | B3, E5, C1 | GND | |
| L18 | QSPI1_A_DATA0 | ↔ | D3 | D0 | 1.8V |
| L19 | QSPI1_A_DATA1 | ↔ | D2 | D1 | 1.8V |
| L20 | QSPI1_A_DATA2 | ↔ | C4 | D2 | 1.8V |
| K22 | QSPI1_A_DATA3 | ↔ | D4 | D3 | 1.8V |
| K19 | QSPI1_A_DATA4 | ↔ | D5 | D4 | 1.8V |
| J23 | QSPI1_A_DATA5 | ↔ | E3 | D5 | 1.8V |
| H23 | QSPI1_A_DATA6 | ↔ | E2 | D6 | 1.8V |
| K18 | QSPI1_A_DATA7 | ↔ | E1 | D7 | 1.8V |
| | | | B4, E4, D1 | +1.8V | |
| | | | A5 | ECS | PU 1.8V |

*Table 33 QSPI NOR Flash: pin assignments*

### 4.12.10 SPI

The MPX-S32G274A has 6 SPI and 4 LLCE SPI interfaces. Due to pin multiplexing there are limitations.

Three SPI interfaces (and no LLCE SPIs) are available as primary interfaces on the module connector.

SPI1 and SPI5 provide one chip select each, whereas SPI0 has two chip selects.

The SPI interfaces can also be configured as GPIO.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

### 4.12.11 UART

The UART of the MPX-S32G274A module is used as debug console. It provides TTL levels and needs to be converted to RS-232 or USB on the carrier, for example.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

See chapter 4.12.12 for the LINFlexD controller which also supports UART mode.

### 4.12.12 LIN

The MPX-S32G274A has 3 LINFlex controllers which can be either configured for LIN or UART mode. Moreover, there are 4 LLCE LIN interfaces routed as primary interfaces to the module connector.

The LINFlexD controllers' pins are not available as primary interfaces on the connector but shared with other interfaces due to pin multiplexing.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

### 4.12.13 FlexRay

The MPX-S32G274A has 1 LLCE FlexRay interface with dual channels as primary interface and another shared FlexRay interface due to pin multiplexing.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

### 4.12.14 SDHC

The MPX-S32G274A module has an SDHC interface with 8 data bits.

It is either routed to an onboard eMMC memory (8-bit) or to the module connector (4-bit). The multiplexing is controlled by I2C via an electronic DIP Switch (see chapter 4.11).

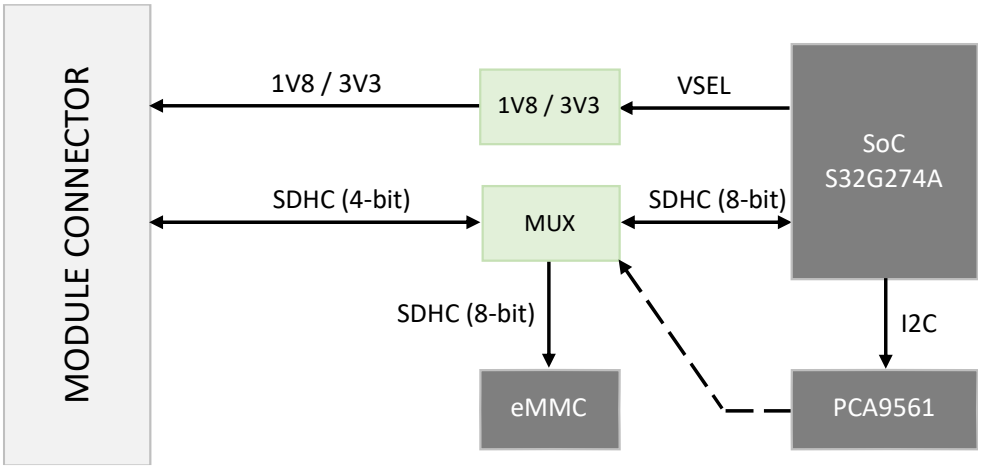


*Figure 4-7 SDHC routing*

Voltage is controlled by SD0_VSELECT from the SoC:

| S32G274A Ball | Signal | Signal Conditioning | Function | |
|---|---|---|---|---|
| G19 | SD0_VSELECT | PD: 10k | **0** | 3.3V |
| | | | **1** | 1.8V |

*Table 34 SDHC voltage select*

“VCC_SDHC_1V8/3V3“ is a reference voltage which indicates the level of the supply voltage of the SDHC interface:

| J23 | | | Module Connector | | | |
|---|---|---|---|---|---|---|
| **Ball** | **Signal** | | **Pin** | **Signal** | **I/O Range** | **Signal conditioning** |
| B2 | VCC_SDHC_1V8/3V3 | → | TK1 | VCC_SDHC_1V8/3V3 | 1.8V / 3.3V | |

### 4.12.15 SerDes

The S32G274A offers two SerDes channels with four lanes in total which can be configured as PCIe or SGMII. In order to be consistent with the NXP documentation they are referred to as “PCIE0” and “PCIE1”.

Each SerDes channel requires a clock which can be configured as 100MHz or 125MHz clock depending on PCIe or SGMII use. More information on SerDes clocks can be obtained from chapter 4.4.

SerDes 0 (“PCIE0”):

| Lane 0 | Lane 1 | Clock |
|---|---|---|
| PCIe x2 | | 100 MHz |
| PCIe x1 | SGMII 1.25 Gbps | 100 MHz |
| SGMII 1.25 Gbps | SGMII 1.25 Gbps | 125 MHz (100 MHz) |

*Table 35 SerDes 0: working modes*

SerDes 1 (“PCIE1”):

| Lane 0 | Lane 1 | Clock |
|---|---|---|
| PCIe x2 | | 100 MHz |
| PCIe x1 | SGMII 1.25 Gbps | 100 MHz |
| SGMII 1.25 Gbps | SGMII 1.25 Gbps | 125 MHz (100 MHz) |
| SGMII 3.125 Gbps | N/A | 125 MHz |

*Table 36 SerDes 1: working modes*

The MPX-S32G274A generates four clock pairs. Two of them are routed to the carrier (“CLKC”) and the other two to the SerDes PLLs of the SoC (“CLKM”). For each SerDes “CLKC” and “CLKM” have the same frequency and can be controlled via an electronic DIP switch.

The S32G274A can also be used as a PCIe endpoint. In this case, SerDes 0 (“PCIE0”) receives its clock pair from the carrier. In order to control the multiplexer on the module, “SEL_CLK_RC/EP#” needs to be driven low.

However, root complex (RC) or endpoint (EP) mode is determined via software.

| Pin | Signal | Signal Conditioning | Function | |
|---|---|---|---|---|
| T130 | SEL_CLK_RC/EP# | PU: 10k | **0** | S32G274A is endpoint (clock from carrier) |
| | | | **1** | S32G274A is root complex (clock from module) |

*Table 37 SerDes: root complex / endpoint*

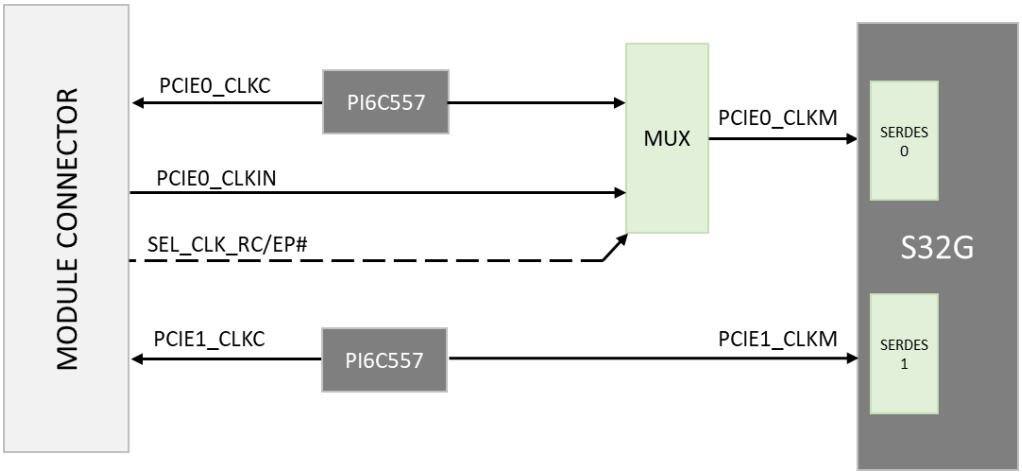


*Figure 4-8 SerDes: clock routing*

# 5 Mechanical Description

## 5.1 Edge Connector

The MPX-S32G274A module has 314 edge finger contacts. Appropriate sockets on the carrier provide 314 pins with 0.5mm pitch and accept edge cards with a thickness of 1.2mm.

## 5.2 Previous Numbering Scheme

The numbering scheme is adopted from other MPX modules which used to have 310 edge fingers only. The reason for this was that you could previously choose from a broad variety of connectors on the market including 310-pin and 314-pin types.

NOTE

**310-pin connectors are obsolete now, the numbering scheme has remained the same.**

## 5.3 Current Numbering Scheme

The differences between 310-pin and 314-pin connectors are four key “pins” that do not carry signals on 310-pin connectors. They are physically not present.

These key pins are, however, available on 314-pin connectors and on the MPX-S32G274A module carry signals. See Figure 5-1 for details:

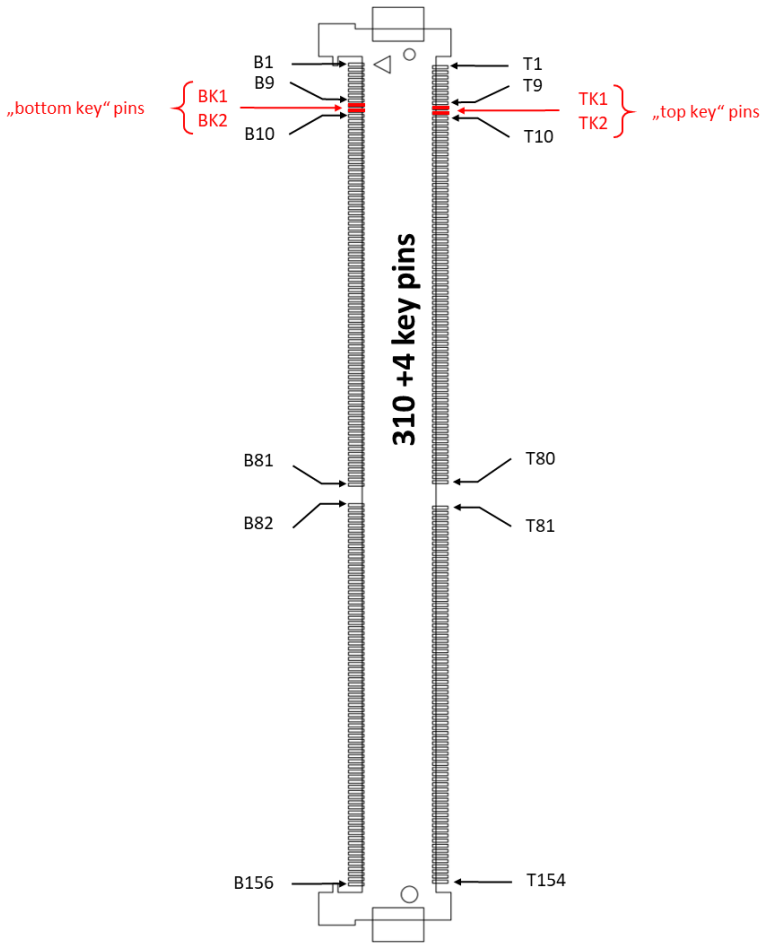


*Figure 5-1 MXM Connector: pin definition*

ATTENTION

**The original connector pinout definition was based on MM70-314-310B1-1-R300 which is now OBSOLETE.**

**314-pin connectors have pins between B9/B10 and T9/T10 which are now connected on the module! They are called “top key” and “bottom key” pins TK1, TK2, BK1, BK2.**

## 5.4 Pin-Layout

The module has 314 pins, 310 pins and 4 pins previously used as key “pins” (see chapter 5.2).

The pin layout is asymmetric, so the pins are unequally distributed among top and bottom side edge fingers.

| Side | Pin Count | Pin Labels |
|---|---|---|
| Bottom | 158 | “B1”, … ”B9”, **”BK1“**, **”BK2“**, ”B10“, … ”B155”, “B156” |
| Top | 156 | “T1”, … ”T9”, **”TK1“**, **”TK2“**, ”T10“, … “T153”, “T154“ |

*Table 38 Connector pin naming scheme*

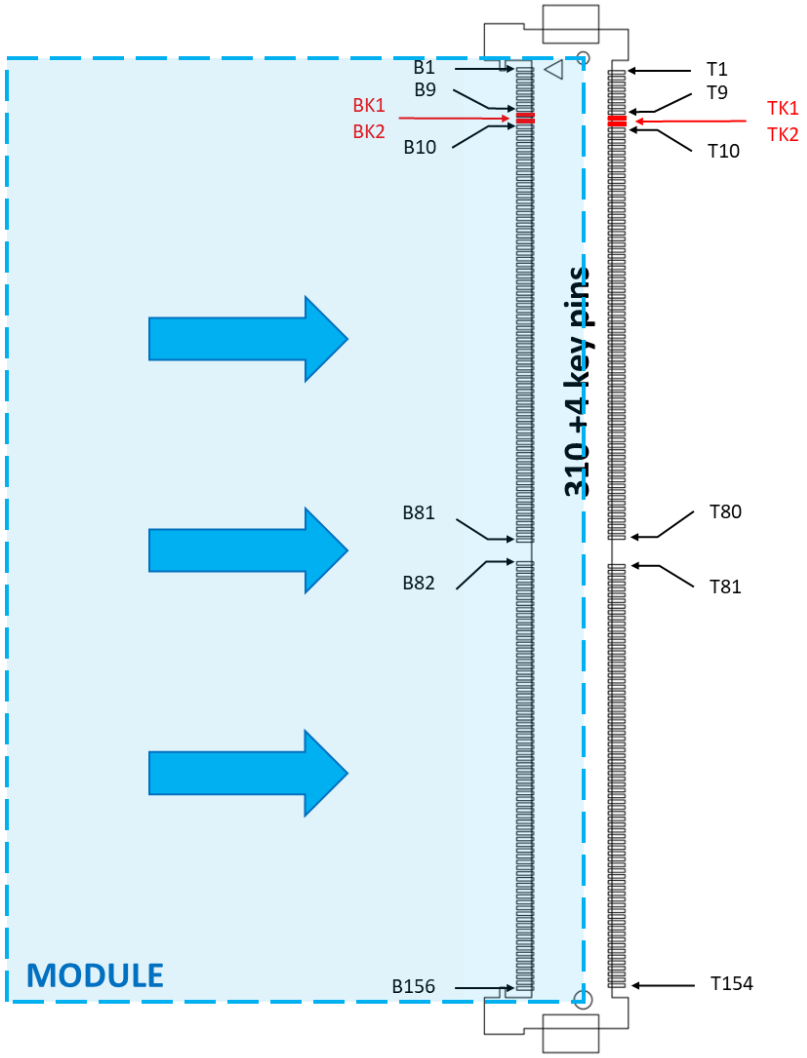


*Figure 5-2 Connector orientation*

The module connector is usually used for MXM3 graphic cards commonly found in notebooks. MicroSys changed the pin layout so that all 314 physically available pins can be used.

Alternatives - there are several connectors on the market that can be used if there are no conflicts with the mechanical dimensions of the module. The connectors usually have deviating mechanical pads thus drop-in replacements may require a combined PCB footprint. Please check the manufacturers' datasheets for details.

The recommended connectors for the MPX-S32G274A are:

| Manufacturer | Ordercode | Board-to-board height | Plating | Comment |
|---|---|---|---|---|
| JAE | MM70-314B1-2-R300 | 3mm | 0.3µm min. gold plating over Ni | 314 pins |
| Foxconn | AS0B826-S55B-7H | 2,7mm | 10µm gold plating | |
| Foxconn | AS0B826-S78B-7H | 5mm | 10µm gold plating | |
| Aces | 91782-3140M-001 | 5mm | 3µm gold plating | |
| Yamaichi | CNU113-314-2201-VE | 5mm | 0.3µ" AU | |

*Table 39 Connector Types: Ordering Information*

## 5.5 Mounting/Unmounting

The mounting or unmounting of the module should only be made in a static free area with full ESD precautions, i.e. as a minimum, a grounded dissipative work surface of sufficient size and a grounded skin contact wrist strap are necessary. Make sure that all parts, the carrier, the module and the heatsink are placed on the same static free area to avoid any discharges between them during assembly.

To mount the MPX-S32G274A module, make sure that the carrier is disconnected from any power or other IO interfaces. Both connector surfaces of the module must be clean as well as the carrier connector should be checked for bent or dirty contacts. Check the module and the carrier for foreign or loose parts, which do not belong to the boards. The screws should have clean threads and be tightened with a maximum torque of 30Ncm.

Insert or remove the MPX-S32G274A module at an angle of about 25° as shown in the following figure.

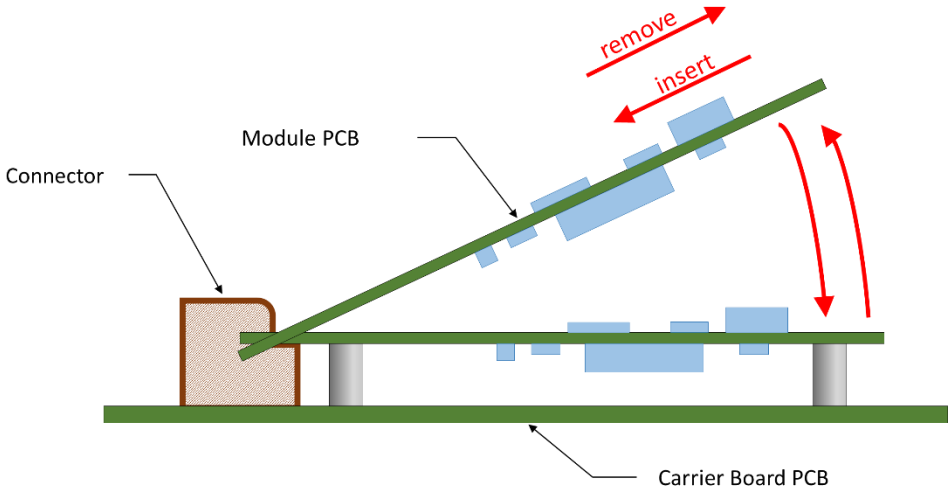


*Figure 5-3 Module (un)mounting*

The thermal conduction between heatsink and SoC is achieved using a thermal pad. Make sure that this thermal pad has the correct thickness and is placed over the SoC package before mounting the heatsink.

For the removal of the module, first unplug all connections to the system. Remove the inner screws, then the outer ones. The thermal pad may cause the heatsink to stick to the module, so take care when pulling them apart to avoid damaging any part of the module. Lift the module to about 25° and remove it from the connector. Store the parts on a static free area.

## 5.6 Board Outline

The following drawing shows the mechanical outline (82x50mm) of the MPX-S32G274A module:

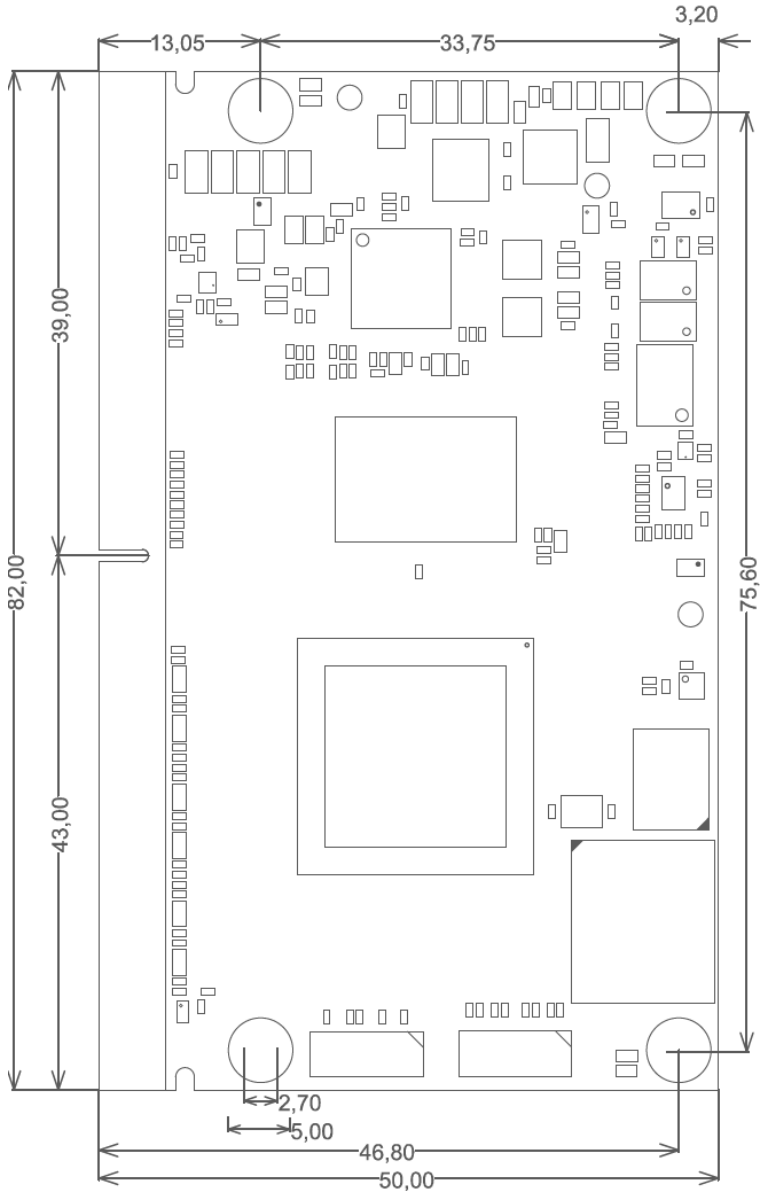


*Figure 5-4 Board dimensions*

The mounting holes require M2.5 screws.

NOTE

**For 3D data files please contact MicroSys.**

## 5.7 Height

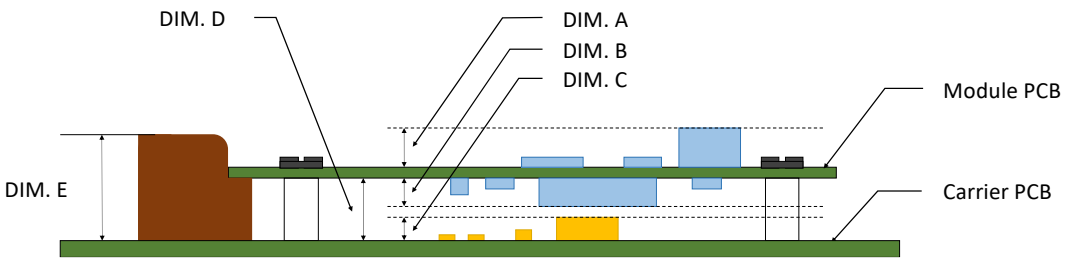


*Figure 5-5 Construction height for parts*

| | Definition | Value |
|---|---|---|
| DIM. A | Module top side parts | 3.10 mm |
| DIM. B | Module bottom side parts | 1.40 mm |
| DIM. C | Carrier parts under the module | DIM. D minus DIM. B |
| DIM. D | Board-to-board height | Depends on connector type |
| DIM. E | Connector product height | Depends on connector type |

*Table 40 Construction height overview*

## 5.8 Thickness

The PCB thickness of the MPX-S32G274A module is 1.2mm ± 10%.

## 5.9 Component Layout - Top Side

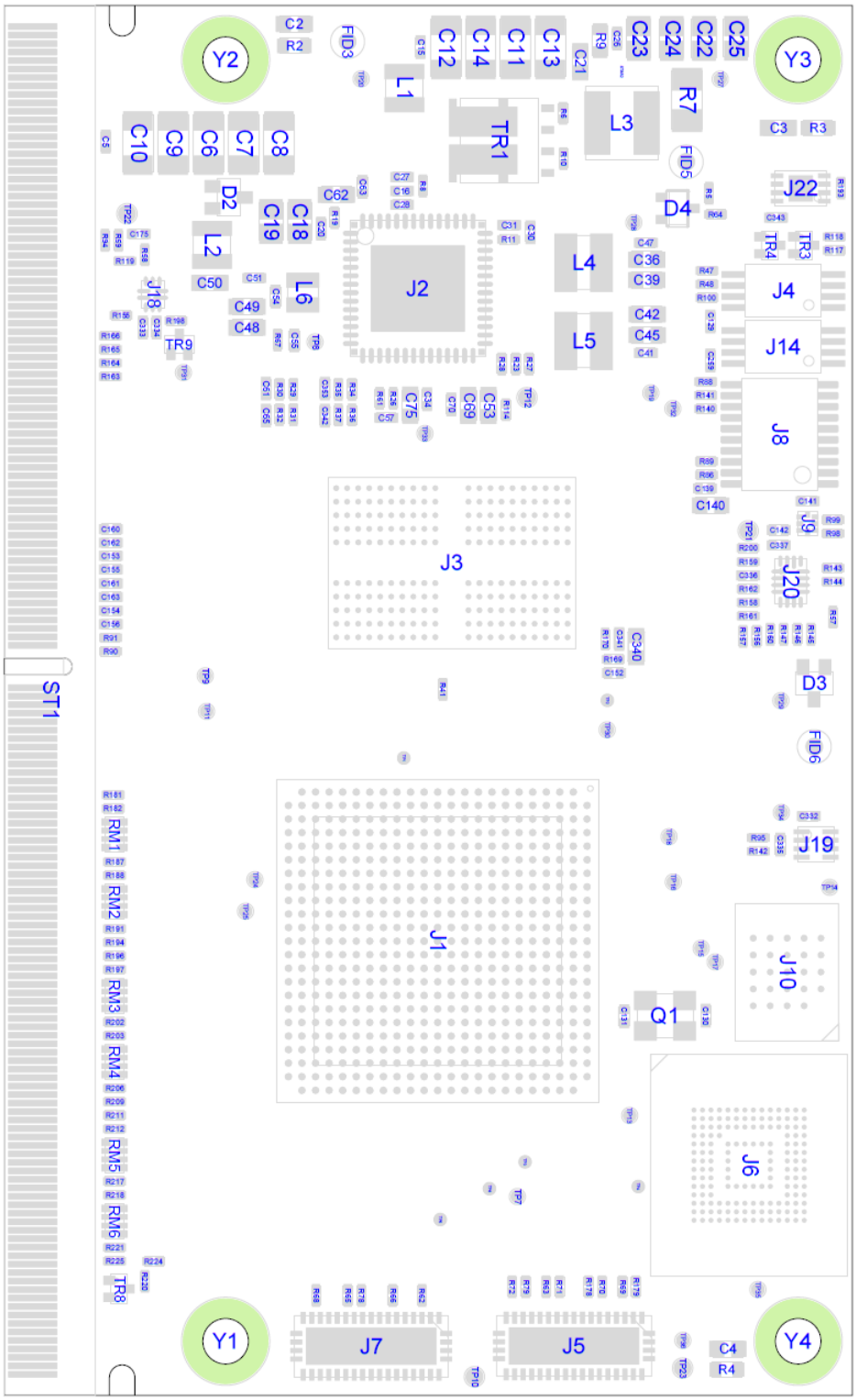


*Figure 5-6 Top Components*

The following table defines the main components on the top side:

| Part Reference | Type | Function |
|---|---|---|
| ST1 | Edge Connector | Connection to carrier |
| J1 | S32G274A | SoC |
| J2 | PMIC | Regulator, power management |
| J3 | LPDDR4 | Memory |
| J4 | Primary Serial RCON | EEPROM |
| J6 | eMMC | Memory |
| J8 | | Electronic DIP switch |
| J10 | Serial NOR Flash | Memory |
| J14 | Secondary Serial RCON | EEPROM |
| J19 | TMP451 | Temperature sensor |
| J20 | | GPIO Expander |
| J22 | | EEPROM |

*Table 41 Top side components*

## 5.10 Component Layout – Bottom Side

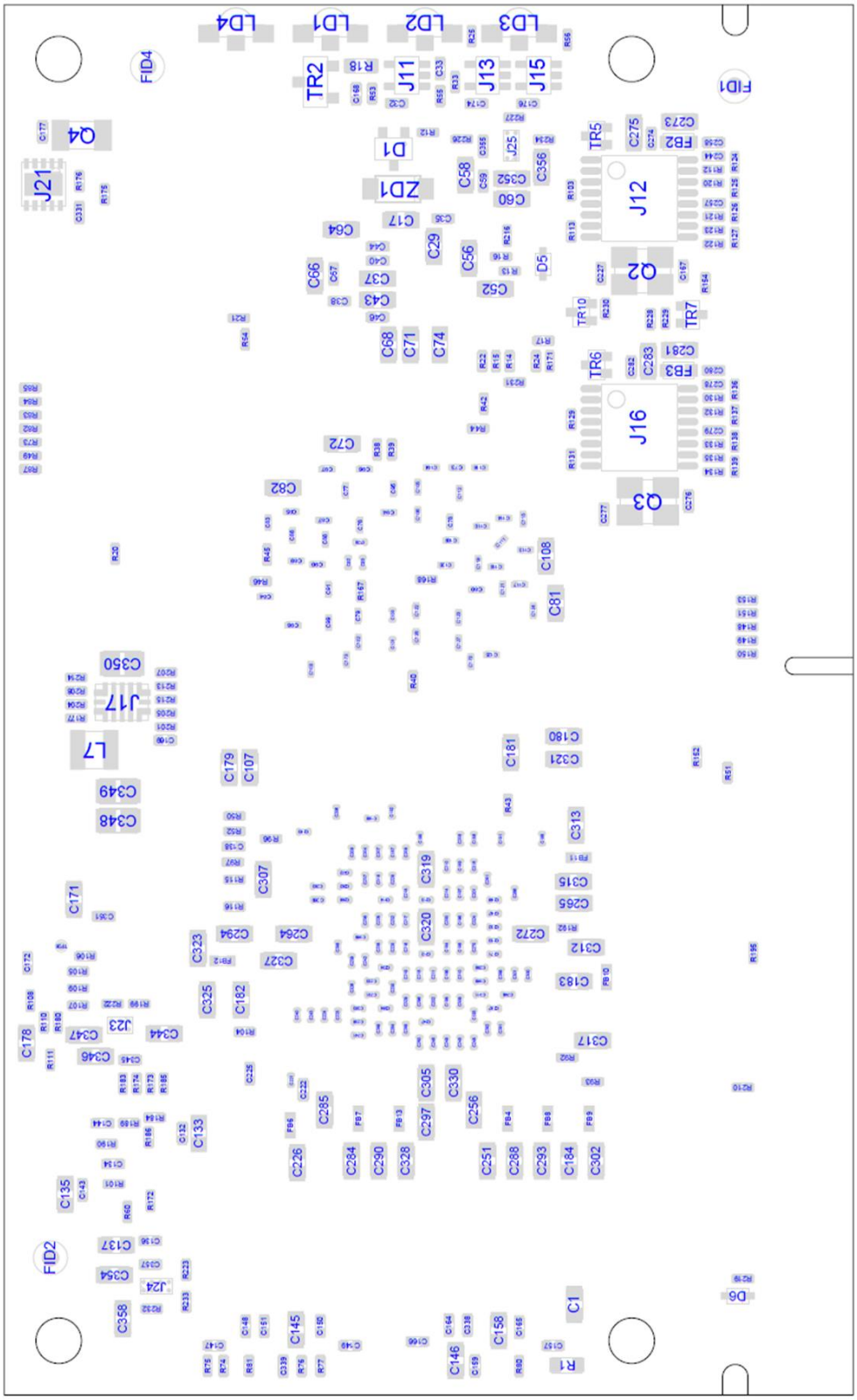


*Figure 5-7 Bottom components*

| Part Reference | Type | Function |
|---|---|---|
| J12 | PI6C557 | Clock Generator |
| J16 | PI6C557 | Clock Generator |
| J21 | PCF85263ATL | RTC |
| LD1, LD2, LD3, LD4 | Side Looker LED | Reset, Power, User LED |

*Table 42 Components on bottom*

# 6 Software

## 6.1 U-Boot

The MPX-S32G274A uses U-Boot as the standard bootloader. The current version of U-Boot is pre-programmed in the boards QSPI Flash memory.

Additionally, there is a U-Boot version available for the SD card if that interface is implemented on the carrier. The standard MicroSys carrier (CRX-S32G) has an SD card interface.

Basically, the bootloader carries out the following tasks:

- Pin configuration
- SoC configuration
- Clock configuration
- LPDDR4 configuration and timing

## 6.2 Operating System

MicroSys Electronics GmbH offers Linux support for the module. Please refer to the MicroSys Software Enablement Guide for more details.

Other Operating Systems are available on request only.

# 7 Safety Requirements And Protective Regulations

## 7.1 EMC

The System on Module MPX-S32G274A is designed to meet requirements for electromagnetic compatibility. Nevertheless, there are several factors which in the target system may require measures against interference.

Active components, especially SoCs of the latest generation not only operate with high frequencies but also drive very fast signal rise times.

At least the following measures shall be applied:

- Provide sufficient block capacitors in the supply voltages
- Keep all clock lines short in order to prevent interference with other signals
- Shield clock lines with ground planes or keep as much distance as possible to other signals
- Provide filtering for all external signals
- Provide an EMI proof housing for final system

## 7.2 ESD

For technical reasons there is no ESD protection on the MPX-S32G274A. Please provide sufficient protection on the carrier and/or system level.

## 7.3 Reliability

The SoM MPX-S32G274A is available for operation in extended temperature range.

Please note that steady high temperature operation reduces lifetime of all electronic components. Make sure that no component on the module ever exceeds its maximum specified temperature during operation or storage. A reasonable cooling concept can dramatically increase the lifetime of the system.

The MPX-S32G274A is designed to withstand a high level of vibration and shock since there are no heavy and no overhanging components on the module. If desired, MicroSys Electronics GmbH can support you with your shock and vibration concept. Please ask your sales representative or send an email inquiry to support@microsys.de.

Relevant components on the module are chosen with values for a high level of derating.

## 7.4 Climatic conditions

The relative humidity during operation or storage of the module may not exceed 10% to 90%, non-condensing.

## 7.5 RoHS

All components on the MPX-S32G274A are RoHS compliant, also a RoHS compliant soldering process is used for manufacturing.

# 8 General notes

Customers responsibility for chip errata:

It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of.

The manufacturer’s advice should be followed.

If desired, MicroSys Electronics GmbH can support you with your lifecycle management regarding chip errata. Please ask your sales representative or send an email inquiry to support@microsys.de.

# 9 History

| Date | Version | Change Description |
|---|---|---|
| 2019-12-06 | 1.0 | Preliminary Version |
| 2020-04-30 | 1.1 | Tidied up and added initial typical power consumption. |
| 2020-05-18 | 1.2 | 310-pin JAE obsolete; added alternatives |
| 2020-11-11 | 2.0 | Hardware Revision 2, Initial Release Version<br>- Changed input supply range<br>- Added TK1, TK2, BK1, BK2 pins on former KEY pins<br>- Renamed “MACx” pins to “RGMIIx” pins<br>- I2C address of serial RCON changed to 0x56<br>- Revised chapter “interface description”<br>- Changed supply voltage for SDHC interface |
| 2021-06-15 | 2.1 | Swapped “PC11” and “PC12” on connector pins “B19”/”B20” |
| 2022-04-12 | 2.2 | Added pullup in chapter 10.5 for pin B85 (JTAG_TMS)<br>Added data for power consumption over Tj in chapter 3.4 |
| 2022-08-17 | 2.3 | Added JTAG pullup requirements in chapter 4.12.2 |
| | | |

*Table 43 Document history*

# 10 Appendix

## 10.1 Acronyms

These acronyms are being used within the document; note that this list does not claim to be complete or exhaustive:

*ADC* ..... *Analog-to-Digital Converter*
*CAN* ..... *Controller Area Network*
*ESD* ..... *Electrostatic Discharge*
*GPL* ..... *General Public License*
*I²C* ..... *Inter-Integrated Circuit*
*JTAG* ..... *Joint Test Action Group*
*LED* ..... *Light Emitting Diode*
*LIN* ..... *Local Interconnect Network*
*LPDDR* ..... *Low Power Double Data Rate memory*
*MCU* ..... *Microcontroller Unit*
*PD* ..... *Pull-Down Resistor*
*PU* ..... *Pull-Up Resistor*
*RGMII* ..... *Reduced Gigabit Media Independent Interface*
*RTC* ..... *Real-Time clock*
*SDHC* ..... *Secure Digital Host Controller*
*SerDes* ..... *Serializer Deserializer*
*SPI* ..... *Serial Peripheral Interface*
*UART* ..... *Universal Asynchronous Receiver Transmitter*
*ULPI* ..... *UTMI+ Low Pin Interface*
*USB* ..... *Universal Serial Bus*

## 10.2 Table of Figures

## 10.3 Table of Tables

## 10.4 Pin Definitions – Top

***OUT = Output from module***

***IN = Input to module***

| Pin | Name | Ball | GPIO | Group | Direction | Supply Voltage | PU/PD | PU/PD Value | Series R/C |
|---|---|---|---|---|---|---|---|---|---|
| T1 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T2 | SD_CLK | E19 | PC14 | SDHC | OUT | **VCC_SDHC_1V8/3V3** | --- | --- | 22R |
| T3 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T4 | SD_CMD | F21 | PC15 | SDHC | INOUT | **VCC_SDHC_1V8/3V3** | --- | --- | 22R |
| T5 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T6 | SD_D0 | G22 | PD01 | SDHC | INOUT | **VCC_SDHC_1V8/3V3** | --- | --- | 0R |
| T7 | SD_D1 | E20 | PD02 | SDHC | INOUT | **VCC_SDHC_1V8/3V3** | --- | --- | 0R |
| T8 | SD_D2 | H19 | PD03 | SDHC | INOUT | **VCC_SDHC_1V8/3V3** | --- | --- | 0R |
| T9 | SD_D3 | H20 | PD04 | SDHC | INOUT | **VCC_SDHC_1V8/3V3** | --- | --- | 0R |
| TK1 | VCC_SDHC_1V8/3V3 | --- | --- | Power / SDHC | | --- | --- | --- | --- |
| TK2 | PMIC_FCCU1_OUT | J2-31 | --- | CTRL | OUT | **+VREF4 (3V3)** | PU | 5k11 | --- |
| T10 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T11 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T12 | RGMII2_MDC/DSPI0_CS7 | M19 | PF00 | RGMII | OUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T13 | RGMII2_MDIO | L22 | PF01 | RGMII | INOUT | **+VREF1 (1V8)** | PU | 10k | 0R |
| T14 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T15 | RGMII2_RXD3/USB_D7 | N23 | PH00 | RGMII / ULPI | IN / INOUT | **+VREF1 (1V8)** | --- | --- | 10R |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| T16 | RGMII2_RXD2/USB_D6 | M21 | PL14 | RGMII / ULPI | IN / INOUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T17 | RGMII2_RXD1/USB_D5 | N21 | PL13 | RGMII / ULPI | IN / INOUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T18 | RGMII2_RXD0/USB_D4 | N20 | PL12 | RGMII / ULPI | IN / INOUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T19 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T20 | RGMII2_RXDV/USB_D3 | M23 | PE01 | RGMII / ULPI | IN / INOUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T21 | RGMII2_RX_CLK/USB_D2 | P21 | PE00 | RGMII / ULPI | IN / INOUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T22 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T23 | RGMII2_TXD3/USB_D1 | L21 | PD15 | RGMII / ULPI | OUT / INOUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T24 | RGMII2_TXD2/USB_D0 | P23 | PD14 | RGMII / ULPI | OUT / INOUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T25 | RGMII2_TXD1/USB_NXT | N22 | PL11 | RGMII / ULPI | OUT / IN | **+VREF1 (1V8)** | --- | --- | 10R |
| T26 | RGMII2_TXD0/USB_STP | P22 | PL10 | RGMII / ULPI | OUT / OUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T27 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T28 | RGMII2_TX_EN/USB_DIR | L23 | PL09 | RGMII / ULPI | OUT / IN | **+VREF1 (1V8)** | --- | --- | 10R |
| T29 | RGMII2_TX_CLK/USB_CLK | N19 | PL08 | RGMII / ULPI | OUT / IN | **+VREF1 (1V8)** | --- | --- | 10R |
| T30 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T31 | RGMII1_MDC | V23 | PD12 | RGMII | OUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T32 | RGMII1_MDIO | R19 | PD13 | RGMII | INOUT | **+VREF1 (1V8)** | PU | 10k | 0R |
| T33 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T34 | RGMII1_RXD3 | U21 | PE13 | RGMII | IN | **+VREF1 (1V8)** | --- | --- | 10R |
| T35 | RGMII1_RXD2 | N18 | PE12 | RGMII | IN | **+VREF1 (1V8)** | --- | --- | 10R |
| T36 | RGMII1_RXD1 | P18 | PE11 | RGMII | IN | **+VREF1 (1V8)** | --- | --- | 10R |
| T37 | RGMII1_RXD0 | P19 | PE10 | RGMII | IN | **+VREF1 (1V8)** | --- | --- | 10R |
| T38 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T39 | RGMII1_RXDV | R23 | PE09 | RGMII | IN | **+VREF1 (1V8)** | --- | --- | 10R |
| T40 | RGMII1_RX_CLK | R21 | PE08 | RGMII | IN | **+VREF1 (1V8)** | --- | --- | 10R |
| T41 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| T42 | RGMII1_TXD3 | T21 | PE07 | RGMII | OUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T43 | RGMII1_TXD2 | U22 | PE06 | RGMII | OUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T44 | RGMII1_TXD1 | T22 | PE05 | RGMII | OUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T45 | RGMII1_TXD0 | T23 | PE04 | RGMII | OUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T46 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T47 | RGMII1_TX_EN | U23 | PE03 | RGMII | OUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T48 | RGMII1_TX_CLK | P20 | PE02 | RGMII | OUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T49 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T50 | RGMII0_MDC | Y21 | PF02 | RGMII | OUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T51 | RGMII0_MDIO | V17 | PE15 | RGMII | INOUT | **+VREF1 (1V8)** | PU | 10k | 0R |
| T52 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T53 | RGMII0_RXD3 | W22 | PH09 | RGMII | IN | **+VREF1 (1V8)** | --- | --- | 10R |
| T54 | RGMII0_RXD2 | W21 | PH08 | RGMII | IN | **+VREF1 (1V8)** | --- | --- | 10R |
| T55 | RGMII0_RXD1 | Y23 | PH07 | RGMII | IN | **+VREF1 (1V8)** | --- | --- | 10R |
| T56 | RGMII0_RXD0 | T20 | PH06 | RGMII | IN | **+VREF1 (1V8)** | --- | --- | 10R |
| T57 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T58 | RGMII0_RXDV | W23 | PH05 | RGMII | IN | **+VREF1 (1V8)** | --- | --- | 10R |
| T59 | RGMII0_RX_CLK | V21 | PH04 | RGMII | IN | **+VREF1 (1V8)** | --- | --- | 10R |
| T60 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T61 | RGMII0_TXD3 | U20 | PH03 | RGMII | OUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T62 | RGMII0_TXD2 | U18 | PH02 | RGMII | OUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T63 | RGMII0_TXD1 | T19 | PH01 | RGMII | OUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T64 | RGMII0_TXD0 | U19 | PJ00 | RGMII | OUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T65 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T66 | RGMII0_TX_EN | T18 | PE14 | RGMII | OUT | **+VREF1 (1V8)** | --- | --- | 10R |
| T67 | RGMII0_TX_CLK | V20 | PH10 | RGMII | OUT | **+VREF1 (1V8)** | --- | --- | 10R |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| T68 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T69 | PCIE1_RX0_N | AB22 | --- | SERDES | IN | **+VREF1 (1V8)** | --- | --- | --- |
| T70 | PCIE1_RX0_P | AA22 | --- | SERDES | IN | **+VREF1 (1V8)** | --- | --- | --- |
| T71 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T72 | PCIE1_RX1_N | AC21 | --- | SERDES | IN | **+VREF1 (1V8)** | --- | --- | --- |
| T73 | PCIE1_RX1_P | AB21 | --- | SERDES | IN | **+VREF1 (1V8)** | --- | --- | --- |
| T74 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T75 | PCIE0_RX0_N | AC19 | --- | SERDES | IN | **+VREF1 (1V8)** | --- | --- | --- |
| T76 | PCIE0_RX0_P | AB19 | --- | SERDES | IN | **+VREF1 (1V8)** | --- | --- | --- |
| T77 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T78 | PCIE0_RX1_N | AC18 | --- | SERDES | IN | **+VREF1 (1V8)** | --- | --- | --- |
| T79 | PCIE0_RX1_P | AB18 | --- | SERDES | IN | **+VREF1 (1V8)** | --- | --- | --- |
| T80 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T81 | CLK_OUT_N | AB13 | --- | CLOCK | OUT | **+VREF1 (1V8)** | --- | --- | 0R |
| T82 | CLK_OUT_P | AC13 | --- | CLOCK | OUT | **+VREF1 (1V8)** | --- | --- | 0R |
| T83 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T84 | PCIE1_TX0_N | Y19 | --- | SERDES | OUT | **+VREF1 (1V8)** | --- | --- | 220nF |
| T85 | PCIE1_TX0_P | W19 | --- | SERDES | OUT | **+VREF1 (1V8)** | --- | --- | 220nF |
| T86 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T87 | PCIE1_TX1_N | Y18 | --- | SERDES | OUT | **+VREF1 (1V8)** | --- | --- | 220nF |
| T88 | PCIE1_TX1_P | W18 | --- | SERDES | OUT | **+VREF1 (1V8)** | --- | --- | 220nF |
| T89 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T90 | PCIE0_TX0_N | Y16 | --- | SERDES | OUT | **+VREF1 (1V8)** | --- | --- | 220nF |
| T91 | PCIE0_TX0_P | W16 | --- | SERDES | OUT | **+VREF1 (1V8)** | --- | --- | 220nF |
| T92 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T93 | PCIE0_TX1_N | Y15 | --- | SERDES | OUT | **+VREF1 (1V8)** | --- | --- | 220nF |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| T94 | PCIE0_TX1_P | W15 | --- | SERDES | OUT | **+VREF1 (1V8)** | --- | --- | 220nF |
| T95 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T96 | AUR_CLK_N | AB11 | --- | AURORA | IN | **+VREF1 (1V8)** | --- | --- | 0R |
| T97 | AUR_CLK_P | AC11 | --- | AURORA | IN | **+VREF1 (1V8)** | --- | --- | 0R |
| T98 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T99 | AUR_TX2_N | AB9 | --- | AURORA | OUT | **+VREF1 (1V8)** | --- | --- | --- |
| T100 | AUR_TX2_P | AC9 | --- | AURORA | OUT | **+VREF1 (1V8)** | --- | --- | --- |
| T101 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T102 | AUR_TX0_N | AB8 | --- | AURORA | OUT | **+VREF1 (1V8)** | --- | --- | --- |
| T103 | AUR_TX0_P | AC8 | --- | AURORA | OUT | **+VREF1 (1V8)** | --- | --- | --- |
| T104 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T105 | AUR_TX1_N | AC6 | --- | AURORA | OUT | **+VREF1 (1V8)** | --- | --- | --- |
| T106 | AUR_TX1_P | AB6 | --- | AURORA | OUT | **+VREF1 (1V8)** | --- | --- | --- |
| T107 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T108 | AUR_TX3_N | AC5 | --- | AURORA | OUT | **+VREF1 (1V8)** | --- | --- | --- |
| T109 | AUR_TX3_P | AB5 | --- | AURORA | OUT | **+VREF1 (1V8)** | --- | --- | --- |
| T110 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T111 | PB02 | D7 | PB02 | GPIO | INOUT | **+VREF3 (3V3)** | --- | --- | --- |
| T112 | PB07 | A5 | PB07 | GPIO | INOUT | **+VREF3 (3V3)** | --- | --- | --- |
| T113 | PB08 | F7 | PB08 | GPIO | INOUT | **+VREF3 (3V3)** | --- | --- | --- |
| T114 | PB15 | B5 | PB15 | GPIO | INOUT | **+VREF3 (3V3)** | --- | --- | --- |
| T115 | PC00 | V9 | PC00 | GPIO | INOUT | **+VREF3 (3V3)** | --- | --- | --- |
| T116 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T117 | +VREF1 | --- | --- | POWER | | 1V8 Reference Output | --- | --- | --- |
| T118 | +VREF2 | --- | --- | POWER | | 1V8 Reference Output | --- | --- | --- |
| T119 | +VREF3 | --- | --- | POWER | | 3V3 Reference Output | --- | --- | --- |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| T120 | +VREF4 | --- | --- | POWER | | 3V3 Reference Output | --- | --- | --- |
| T121 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T122 | PCIE0_CLKIN_N | AC15 | --- | SERDES | IN | **+VREF1 (1V8)** | --- | --- | --- |
| T123 | PCIE0_CLKIN_P | AB15 | --- | SERDES | IN | **+VREF1 (1V8)** | --- | --- | --- |
| T124 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T125 | NMI | G6 | --- | CTRL | IN | **+VREF3 (3V3)** | PU | 4k7 | --- |
| T126 | PMIC_RST# | J2-19 | --- | CTRL | OUT | **+VREF4 (3V3)** | PU | 2k2 | --- |
| T127 | RSTIN# | R55-1 | --- | CTRL | IN | **+VREF4 (3V3)** | PU | 4k7 | 100R |
| T128 | RST# | J2-19 | --- | CTRL | OUT | **+VREF4 (3V3)** | PU | 2k2 | --- |
| T129 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T130 | SEL_CLK_RC/EP# | TR9-1 | --- | CTRL | IN | **+VREF4 (3V3)** | PU | 10k | --- |
| T131 | RCW_SEL# | TR3-1<br>J14-2 / J14-3 | --- | CTRL | IN | **+3V3_EXT** | PU | 4k7 | --- |
| T132 | MUX_SEL# | TR4-1 | --- | CTRL | IN | **+3V3_EXT** | PU | 10k | --- |
| T133 | VCC_RTC | --- | --- | POWER | | RTC Backup Supply:<br>Module Input (0.9V - 5.5V) | --- | --- | --- |
| T134 | +3V3_EXT | --- | --- | PRODUCTION | | Programming Voltage:<br>Module Input (3.3V ± 5%) | --- | --- | --- |
| T135 | I2C_SCL_PROG | J9-7 | --- | PRODUCTION | OUT | **+3V3_EXT** | PU | 2k7 | --- |
| T136 | I2C_SDA_PROG | J9-6 | --- | PRODUCTION | INOUT | **+3V3_EXT** | PU | 2k7 | --- |
| T137 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T138 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T139 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T140 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T141 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T142 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| T143 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T144 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T145 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| T146 | +VIN | --- | --- | POWER | | 9-30V | --- | --- | --- |
| T147 | +VIN | --- | --- | POWER | | 9-30V | --- | --- | --- |
| T148 | +VIN | --- | --- | POWER | | 9-30V | --- | --- | --- |
| T149 | +VIN | --- | --- | POWER | | 9-30V | --- | --- | --- |
| T150 | +VIN | --- | --- | POWER | | 9-30V | --- | --- | --- |
| T151 | +VIN | --- | --- | POWER | | 9-30V | --- | --- | --- |
| T152 | +VIN | --- | --- | POWER | | 9-30V | --- | --- | --- |
| T153 | +VIN | --- | --- | POWER | | 9-30V | --- | --- | --- |
| T154 | +VIN | --- | --- | POWER | | 9-30V | --- | --- | --- |

## 10.5 Pin Definitions – Bottom

***OUT = Output from module***

***IN = Input to module***

| Pin | Name | Ball | Target | Group | Direction | Supply Voltage | PU/PD | PU/PD Value | Series R/C |
|---|---|---|---|---|---|---|---|---|---|
| B1 | ADC_CH_11 | C21 | --- | ADC | IN | **+VREF1 (1V8)** | --- | --- | --- |
| B2 | ADC_CH_10 | A20 | --- | ADC | IN | **+VREF1 (1V8)** | --- | --- | --- |
| B3 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B4 | ADC_CH_09 | B20 | --- | ADC | IN | **+VREF1 (1V8)** | --- | --- | --- |
| B5 | ADC_CH_08 | A19 | --- | ADC | IN | **+VREF1 (1V8)** | --- | --- | --- |
| B6 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B7 | ADC_CH_07 | C22 | --- | ADC | IN | **+VREF1 (1V8)** | --- | --- | --- |
| B8 | ADC_CH_06 | D23 | --- | ADC | IN | **+VREF1 (1V8)** | --- | --- | --- |
| B9 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| BK1 | PMIC_STBY# | J2-2 | | CTRL | IN | **+VREF4 (3V3)** | PU | 10k | --- |
| BK2 | PMIC_VDD_OK | J2-4 | | CTRL | OUT | **+VREF4 (3V3)** | --- | --- | --- |
| B10 | ADC_CH_05 | B22 | --- | ADC | IN | **+VREF1 (1V8)** | --- | --- | --- |
| B11 | ADC_CH_04 | B21 | --- | ADC | IN | **+VREF1 (1V8)** | --- | --- | --- |
| B12 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B13 | ADC_CH_03 | D22 | --- | ADC | IN | **+VREF1 (1V8)** | --- | --- | --- |
| B14 | ADC_CH_02 | E23 | --- | ADC | IN | **+VREF1 (1V8)** | --- | --- | --- |
| B15 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| B16 | ADC_CH_01 | E22 | --- | ADC | IN | +VREF1 (1V8) | --- | --- | --- |
| B17 | ADC_CH_00 | F23 | --- | ADC | IN | +VREF1 (1V8) | --- | --- | --- |
| B18 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B19 | CAN00_RX | F15 | PC11 | CAN | IN | +VREF4 (3V3) | --- | --- | --- |
| B20 | CAN00_TX | G11 | PC12 | CAN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B21 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B22 | CAN01_RX | D17 | PJ02 | CAN | IN | +VREF4 (3V3) | --- | --- | --- |
| B23 | CAN01_TX | B11 | PJ01 | CAN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B24 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B25 | CAN02_RX | C15 | PJ04 | CAN | IN | +VREF4 (3V3) | --- | --- | --- |
| B26 | CAN02_TX | D10 | PJ03 | CAN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B27 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B28 | CAN03_RX | D15 | PJ06 | CAN | IN | +VREF4 (3V3) | --- | --- | --- |
| B29 | CAN03_TX | C11 | PJ05 | CAN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B30 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B31 | CAN04_RX | F16 | PJ08 | CAN | IN | +VREF4 (3V3) | --- | --- | --- |
| B32 | CAN04_TX | D12 | PJ07 | CAN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B33 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B34 | CAN05_RX | D16 | PJ10 | CAN | IN | +VREF4 (3V3) | --- | --- | --- |
| B35 | CAN05_TX | B12 | PJ09 | CAN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B36 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B37 | CAN06_RX | E16 | PJ12 | CAN | IN | +VREF4 (3V3) | --- | --- | --- |
| B38 | CAN06_TX | E12 | PJ11 | CAN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B39 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B40 | CAN07_RX | C16 | PJ14 | CAN | IN | +VREF4 (3V3) | --- | --- | --- |
| B41 | CAN07_TX | A11 | PJ13 | CAN | OUT | +VREF3 (3V3) | --- | --- | --- |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| B42 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B43 | CAN08_RX | A15 | PK00 | CAN | IN | **+VREF4 (3V3)** | --- | --- | --- |
| B44 | CAN08_TX | A10 | PJ15 | CAN | OUT | **+VREF3 (3V3)** | --- | --- | --- |
| B45 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B46 | CAN09_RX | D14 | PK02 | CAN | IN | **+VREF4 (3V3)** | --- | --- | --- |
| B47 | CAN09_TX | F11 | PK01 | CAN | OUT | **+VREF3 (3V3)** | --- | --- | --- |
| B48 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B49 | CAN10_RX | F14 | PK04 | CAN | IN | **+VREF4 (3V3)** | --- | --- | --- |
| B50 | CAN10_TX | E11 | PK03 | CAN | OUT | **+VREF3 (3V3)** | --- | --- | --- |
| B51 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B52 | CAN11_RX | B15 | PK06 | CAN | IN | **+VREF4 (3V3)** | --- | --- | --- |
| B53 | CAN11_TX | D11 | PK05 | CAN | OUT | **+VREF3 (3V3)** | --- | --- | --- |
| B54 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B55 | CAN12_RX | F13 | PK08 | CAN | IN | **+VREF4 (3V3)** | --- | --- | --- |
| B56 | CAN12_TX | C10 | PK07 | CAN | OUT | **+VREF3 (3V3)** | --- | --- | --- |
| B57 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B58 | CAN13_RX | E14 | PK10 | CAN | IN | **+VREF4 (3V3)** | --- | --- | --- |
| B59 | CAN13_TX | E10 | PK09 | CAN | OUT | **+VREF3 (3V3)** | --- | --- | --- |
| B60 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B61 | CAN14_RX | C14 | PK12 | CAN | IN | **+VREF4 (3V3)** | --- | --- | --- |
| B62 | CAN14_TX | A9 | PK11 | CAN | OUT | **+VREF3 (3V3)** | --- | --- | --- |
| B63 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B64 | CAN15_RX | B13 | PK14 | CAN | IN | **+VREF4 (3V3)** | --- | --- | --- |
| B65 | CAN15_TX | C9 | PK13 | CAN | OUT | **+VREF3 (3V3)** | --- | --- | --- |
| B66 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B67 | PA15_DSPI0_SOUT | W13 | PA15 | SPI | OUT | **+VREF3 (3V3)** | --- | --- | --- |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| B68 | PA13_DSPI0_SCK | U12 | PA13 | SPI | OUT | +VREF3 (3V3) | --- | --- | --- |
| B69 | PA14_DSPI0_SIN | AA12 | PA14 | SPI | IN | +VREF3 (3V3) | --- | --- | --- |
| B70 | PB09_DSPI0_CS1 | AA10 | PB09 | SPI | OUT | +VREF3 (3V3) | --- | --- | --- |
| B71 | PB10_DSPI0_CS2 | V11 | PB10 | SPI | OUT | +VREF3 (3V3) | --- | --- | --- |
| B72 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B73 | PA06_DSPI1_SOUT | Y9 | PA06 | SPI | OUT | +VREF3 (3V3) | --- | --- | --- |
| B74 | PA08_DSPI1_SCK | U10 | PA08 | SPI | OUT | +VREF3 (3V3) | --- | --- | --- |
| B75 | PF15_DSPI1_SIN | U8 | PF15 | SPI | IN | +VREF3 (3V3) | --- | --- | --- |
| B76 | PA07_DSPI1_CS0 | Y11 | PA07 | SPI | IN | +VREF3 (3V3) | --- | --- | --- |
| B77 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B78 | PA11_DSPI5_SOUT | D8 | PA11 | SPI | OUT | +VREF3 (3V3) | --- | --- | --- |
| B79 | PA09_DSPI5_SCK | B8 | PA09 | SPI | OUT | +VREF3 (3V3) | --- | --- | --- |
| B80 | PA10_DSPI5_SIN | E13 | PA10 | SPI | IN | +VREF4 (3V3) | --- | --- | --- |
| B81 | PA12_DSPI5_CS0 | C7 | PA12 | SPI | IN | +VREF3 (3V3) | --- | --- | --- |
| B82 | JTAG_TCK | W9 | PA04 | JTAG | IN | +VREF3 (3V3) | PD | 10k | --- |
| B83 | JTAG_TDO | AA7 | PA01 | JTAG | OUT | +VREF3 (3V3) | --- | --- | --- |
| B84 | JTAG_TDI | V7 | PA00 | JTAG | IN | +VREF3 (3V3) | --- | --- | --- |
| B85 | JTAG_TMS | U7 | PA05 | JTAG | IN | +VREF3 (3V3) | PU | 10k | --- |
| B86 | JCOMP | W7 | --- | JTAG | IN | +VREF3 (3V3) | PD | 10k | --- |
| B87 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B88 | PF03_CLKOUT0 | V14 | PF03 | CLOCK | OUT | +VREF1 (1V8) | --- | --- | --- |
| B89 | PF04_CLKOUT1 | V13 | PF04 | CLOCK | OUT | +VREF1 (1V8) | --- | --- | --- |
| B90 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B91 | FLXR0A_RX_D | A13 | PL03 | FLEXRAY | IN | +VREF4 (3V3) | --- | --- | --- |
| B92 | FLXR0A_TX_D | A8 | PL02 | FLEXRAY | OUT | +VREF3 (3V3) | --- | --- | --- |
| B93 | FLXR0A_TXEN# | E9 | PL01 | FLEXRAY | OUT | +VREF3 (3V3) | --- | --- | --- |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| B94 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B95 | FLXR0B_RX_D | D13 | PL06 | FLEXRAY | IN | **+VREF4 (3V3)** | --- | --- | --- |
| B96 | FLXR0B_TX_D | C8 | PL05 | FLEXRAY | OUT | **+VREF3 (3V3)** | --- | --- | --- |
| B97 | FLXR0B_TXEN# | A7 | PL04 | FLEXRAY | OUT | **+VREF3 (3V3)** | --- | --- | --- |
| B98 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B99 | PB12_FXCAN2_RX | F8 | PB12 | CAN | IN | **+VREF3 (3V3)** | --- | --- | --- |
| B100 | PB11_FXCAN2_TX | G8 | PB11 | CAN | OUT | **+VREF3 (3V3)** | --- | --- | --- |
| B101 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B102 | PB14_FXCAN3_RX | E6 | PB14 | CAN | IN | **+VREF3 (3V3)** | --- | --- | --- |
| B103 | PB13_FXCAN3_TX | G7 | PB13 | CAN | OUT | **+VREF3 (3V3)** | --- | --- | --- |
| B104 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B105 | LIN0_RX | A12 | PL00 | LIN | IN | **+VREF4 (3V3)** | --- | --- | --- |
| B106 | LIN0_TX | F10 | PK15 | LIN | OUT | **+VREF3 (3V3)** | --- | --- | --- |
| B107 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B108 | LIN1_RX | C13 | PC04 | LIN | IN | **+VREF4 (3V3)** | --- | --- | --- |
| B109 | LIN1_TX | B6 | PC08 | LIN | OUT | **+VREF3 (3V3)** | --- | --- | --- |
| B110 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B111 | LIN2_RX | A14 | PC06 | LIN | IN | **+VREF4 (3V3)** | --- | --- | --- |
| B112 | LIN2_TX | G10 | PC05 | LIN | OUT | **+VREF3 (3V3)** | --- | --- | --- |
| B113 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B114 | LIN3_RX | G13 | PL07 | LIN | IN | **+VREF4 (3V3)** | --- | --- | --- |
| B115 | LIN3_TX | B9 | PC07 | LIN | OUT | **+VREF3 (3V3)** | --- | --- | --- |
| B116 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B117 | PCIE1_CLKC_N | J16-14 | --- | SERDES | OUT | **+VREF4 (3V3)** | PD | 49R9 | 33R |
| B118 | PCIE1_CLKC_P | J16-15 | --- | SERDES | OUT | **+VREF4 (3V3)** | PD | 49R9 | 33R |
| B119 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| B120 | PCIE0_CLKC_N | J12-10 | --- | SERDES | OUT | +VREF4 (3V3) | PD | 49R9 | 33R |
| B121 | PCIE0_CLKC_P | J12-11 | --- | SERDES | OUT | +VREF4 (3V3) | PD | 49R9 | 33R |
| B122 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B123 | PMIC_FSOUT# | J2-14 | --- | CTRL | OUT | +VREF3 (3V3) | PU | 4k7 | 0R |
| B124 | PMIC_FIN | J2-20 | --- | CTRL | IN | +VREF4 (3V3) | PD | 10k | --- |
| B125 | VDD_OTP | J2-27 | --- | PRODUCTION | | for testing only:<br>do not connect | PD | 470k | --- |
| B126 | PMIC_PWRON1 | J2-49 | --- | CTRL | IN | **+VIN** | PU | 5k11 | --- |
| B127 | PMIC_PSYNC | J2-29 | --- | CTRL | IN | +VREF4 (3V3) | PD | 0R | --- |
| B128 | PMIC_FOUT/AMUX | J2-24 | --- | CTRL | OUT | +VREF4 (3V3) | --- | --- | --- |
| B129 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B130 | PC09_UART0_TX | U11 | PC09 | UART | OUT | +VREF3 (3V3) | --- | --- | --- |
| B131 | PC10_UART0_RX | Y12 | PC10 | UART | IN | +VREF3 (3V3) | --- | --- | --- |
| B132 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B133 | PB01_I2C0_SCL | E7 | PB01 | I2C | OUT | +VREF3 (3V3) | PU | 4k7 | --- |
| B134 | PB00_I2C0_SDA | W12 | PB00 | I2C | INOUT | +VREF3 (3V3) | PU | 4k7 | --- |
| B135 | PB03_I2C1_SCL | C6 | PB03 | I2C | OUT | +VREF3 (3V3) | PU | 4k7 | --- |
| B136 | PB04_I2C1_SDA | E8 | PB04 | I2C | INOUT | +VREF3 (3V3) | PU | 4k7 | --- |
| B137 | PB05_I2C2_SCL | A6 | PB05 | I2C | OUT | +VREF3 (3V3) | PU | 4k7 | --- |
| B138 | PB06_I2C2_SDA | G9 | PB06 | I2C | INOUT | +VREF3 (3V3) | PU | 4k7 | --- |
| B139 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B140 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B141 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B142 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B143 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B144 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| B145 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B146 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B147 | ***GND*** | --- | --- | GND | | --- | --- | --- | --- |
| B148 | +VIN | --- | --- | Power | | 9-30V | --- | --- | --- |
| B149 | +VIN | --- | --- | Power | | 9-30V | --- | --- | --- |
| B150 | +VIN | --- | --- | Power | | 9-30V | --- | --- | --- |
| B151 | +VIN | --- | --- | Power | | 9-30V | --- | --- | --- |
| B152 | +VIN | --- | --- | Power | | 9-30V | --- | --- | --- |
| B153 | +VIN | --- | --- | Power | | 9-30V | --- | --- | --- |
| B154 | +VIN | --- | --- | Power | | 9-30V | --- | --- | --- |
| B155 | +VIN | --- | --- | Power | | 9-30V | --- | --- | --- |
| B156 | +VIN | --- | --- | Power | | 9-30V | --- | --- | --- |

## 10.6 Pins not available for pin multiplexing

| Ball | Name | Usage | Comment |
|---|---|---|---|
| PC14 | | SDC / eMMC | GPIO possible in case SEL_EMMC_SDHC# is always low (eMMC cannot be used) |
| PC15 | | SDC / eMMC | GPIO possible in case SEL_EMMC_SDHC# is always low (eMMC cannot be used) |
| PD00 | | SDC / eMMC | GPIO possible in case SEL_EMMC_SDHC# is always low (eMMC cannot be used) |
| PD01 | | SDC / eMMC | GPIO possible in case SEL_EMMC_SDHC# is always low (eMMC cannot be used) |
| PD02 | | SDC / eMMC | GPIO possible in case SEL_EMMC_SDHC# is always low (eMMC cannot be used) |
| PD03 | | SDC / eMMC | GPIO possible in case SEL_EMMC_SDHC# is always low (eMMC cannot be used) |
| PD04 | | SDC / eMMC | GPIO possible in case SEL_EMMC_SDHC# is always low (eMMC cannot be used) |
| PD05 | | SDC / eMMC | N/A |
| PD06 | | SDC / eMMC | N/A |
| PD07 | | SDC / eMMC | N/A |
| PD08 | | SDC / eMMC | N/A |
| PD09 | | SDC / eMMC | N/A |
| PD10 | | SDC / eMMC | N/A |
| | | | |
| PG00 | | QSPI | N/A |
| PG01 | | QSPI | N/A |
| PG02 | | QSPI | N/A |
| PG03 | | QSPI | N/A |
| PG04 | | QSPI | N/A |
| PG05 | | QSPI | N/A |
| PF05 | | QSPI | N/A |
| PF06 | | QSPI | N/A |
| PF07 | | QSPI | N/A |

| | | | |
|---|---|---|---|
| PF08 | | QSPI | N/A |
| PF09 | | QSPI | N/A |
| PF10 | | QSPI | N/A |
| PF11 | | QSPI | N/A |
| PF12 | | QSPI | N/A |
| PF13 | | QSPI | N/A |
| PF14 | | QSPI | N/A |
| | | | |
| PA02 | PA02_BOOTMOD1 | CONFIG | N/A |
| PA03 | PA03_BOOTMOD2 | CONFIG | N/A |
| | | | |
| PB00 | PB00_I2C0_SDA | I2C | N/A |
| PB01 | PB01_I2C0_SCL | I2C | N/A |
| | | | |
| PC01 | PC01_I2C4_SDA_PMIC | I2C | N/A |
| PC02 | PC02_I2C4_SCL_PMIC | I2C | N/A |
| | | | |
| PC03 | PMIC_IRQ# | CONFIG | N/A |
| PC13 | PC13 | N/A | N/A |
| | | | |
| PD11 | PMIC_FS0# | CONFIG | N/A |