

miriac® MPX-S32Z2

Coming soon

- 8 Arm® Cortex®-R52 cores at up to 1 GHz with flexible split/lock configurations: Each Arm Cortex-R52 core includes Arm Neon™ SIMD technology Lockstep Arm® Cortex®-M33 System Manager core
- DSP/ML processor (25 GFLOPS)
- 2 GB 16-bit soldered LPDDR4 RAM at 1600 MT/s



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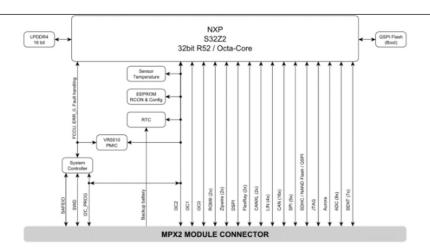
Find out more about our miriac® MPX-S32Z2 below. More information on request.







Block Diagrams (Preliminary)



Features -

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СРИ	
Architecture	Arm® Cortex®-R52
Processor	NXP® S32Z2 CPU: • 8 Arm® Cortex®-R52 cores at up to 1 GHz with flexible split/lock configurations • Each Arm Cortex-R52 core includes Arm Neon™ • SIMD technology Lockstep Arm® Cortex®-M33 SystemManager core • DSP/ML processor (25 GFLOPS)
DRAM	2 GB 16-bit soldered LPDDR4 RAM at 1600 MT/s
Memory	
Flash	512 MB QSPI Flash
Flash Card	Interface for external SD-card (only Interface NOT on board)
Boot Flash	Boot select: QSPI / eMMC / SDHC (only Interface NOT on board)
eMMC	Interface for external and eMMC (only Interface NOT on board)
Ethernet	
RGMII	2x 1GbE
Ю	
13C	3x (with I2C support)
CAN	16x
CAN XL	2x
Zipwire	2x
SENT	7x
SPI	5x
FlexRay	2x
LIN	4x
Analog Inputs (ADCs)	8x
JTAG Debug Interface	Yes
Aurora Interface	Yes
Security / Safety	
Security	Hardware Security Engine (HSE) for secure boot and accelerated security services
Safety	μ controller to monitor voltages

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Operating Condition	
Power Supply Voltage	Single DC power input (+9 V to +30 V)
Mechanical	
Dimensions	82 mm x 50 mm
Connector Type	MXM3.0

Our standard product versions offer what we consider to be the optimum configuration in terms of performance, price, usage and TDP. The product features lists specify the maximum range of functions per interface. However, not all interfaces or functions are always available in parallel. Flexible SERDES multiplexing is one of the reasons for this. In addition, we provide multiple memory expansion options and are also happy to accommodate specific customer wishes. So do not hesitate to contact us directly to discuss your desired configuration.



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