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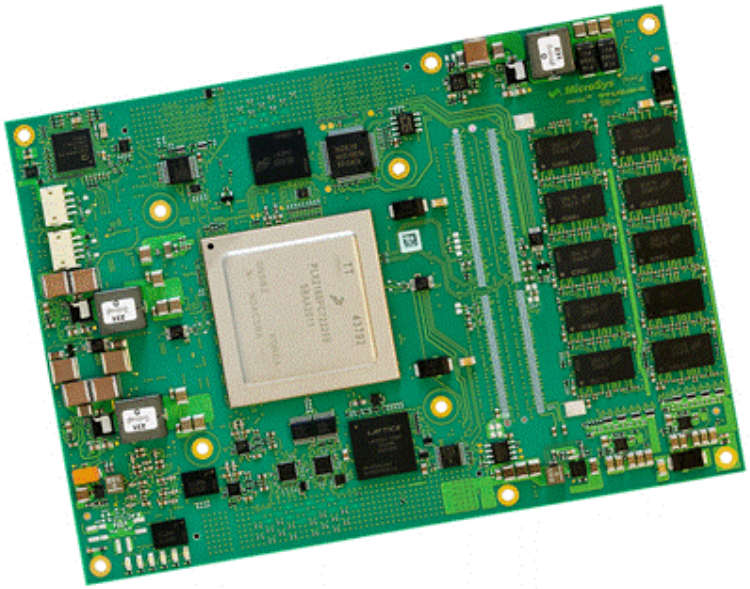

miriac MPX-LX2160A

User Manual (HW Revision 2)

V1.4

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1 General Notes

1.1 Warranty

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1.5 Symbols, Conventions and Abbreviations

1.5.1 Symbols

Throughout this document, the following symbols will be used:

	Information marked with this symbol MUST be obeyed to avoid the risk of severe injury, health danger, or major destruction of the unit and its environment
	Information marked with this symbol MUST be obeyed to avoid the risk of possible injury, permanent damage or malfunction of the unit.
	Information marked with this symbol gives important hints upon details of this manual in order to get the best use out of the product and its features.

Table 1-1 Symbols

1.5.2 Conventions

Symbol	Explanation
# / xxx_B	denotes a low active signal
←	denotes the signal flow in the shown direction
→	denotes the signal flow in the shown direction
↔	denotes the signal flow in both directions
→	denotes the signal flow in the shown direction with additional logic / additional ICs in the signal path
I/O / INOUT	denotes a bidirectional pin
Input	denotes an input pin
Output	denotes an output pin
matched	denotes that the corresponding signal is to be routed impedance controlled and length matched
Pin 1	refers to the numeric pin of a component package
Pin a1	refers to the array position of a pin within a component package
xxx- / xxx_N	denotes the negative signal of a differential pair
xxx+ / xxx_P	denotes the positive signal of a differential pair
xxx	denotes an optional not mounted or not assembled part

Table 1-2 Conventions

2 Introduction

Thank you for choosing the MicroSys MPX-LX2160A System-on-Modue (SoM). This manual should help you get started and achieve the best performance from all of its features.

2.1 Safety and Handling Precautions

	**DO NOT exceed the rated maximum values for the power supply! This may result in severe permanent damage to the unit, as well as possible serious injury.** **ALWAYS keep the unit dry, clean and free of foreign objects. Otherwise, irreparable damage may occur.**
	**Parts of the unit may become hot during operation. Take care not to touch any parts of the circuitry during operation to avoid burns and operate the unit in a well-ventilated location. Provide an appropriate cooling solution as required.**
	**Electrostatic discharge (ESD) can damage the unit. Always take the necessary ESD precautions.** **Many pins on the module connector are directly connected to the CPU or other ESD sensitive devices.** **Make or break ANY connection ONLY while the unit is switched OFF.** **Otherwise, permanent damage to the unit may occur, which is not covered by warranty.**
	**There is no separate SHIELD connection.** **The module's mounting holes are not connected to GND** **Take this into account when handling and mounting the unit.**
	**EXERCISE EXTREME HARE WHEN INSERTING OR REMIVING THE MODULE FROM ITS BOARD-TO-BOARD CONNECTORS. DO NOT TILT OR SHIFT THE MODULE OR THE CONNECTORS WILL BE DAMAGED. ALWAYS INSERT AND REMOVE THE MODULE WITH EQUAL PRESSURE ON BOTH CONNECTORS IN A LINEAR MOTION**

Table 2-1 Safety and Handling Precautions

2.2 Short Description

The LX2160A multicore processor from NXP is a member of the Layerscape family of SoCs with 16 Arm Cortex-A72 cores. It exposes a wide variety of external interfaces, which are explained in detail in the following chapters. The cores feature dedicated L2 Cache for each dual-core cluster, as well as a unified L3 cache.

The Cortex-A72 cores run at a maximum clock speed of 2200 MHz, 2000 MHz or 1800 MHz depending on the speed grade ordered. The core frequency can be clocked down, if needed, to lower the power consumption.

MicroSys Electronics GmbH offers a Development Kit consisting of:

- the MPX-LX2160A module itself,
- and the CRX08 carrier board.

It targets both

- evaluation of the chosen MPX-LX2160A SoM variant
- usage in an industrial application as a high-performance edge computing device, file server, AI edge cluster or other application

This document gives an overview of the board's connectors and how to take the first steps with the initial setup.

2.3 Shipping List

Tbd

3 System Description

3.1 Block Diagram

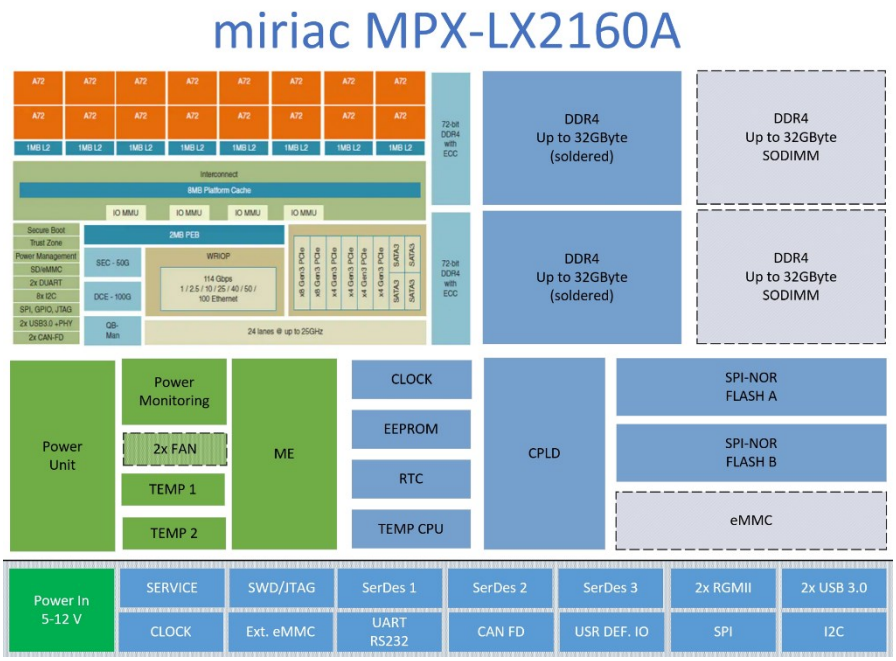


Figure 3-1 Block Diagram

3.2 System Components

- QorIQ Layerscape processor LX2160A or LX2120A or LX2080A
- Microcontroller as monitoring and supervising unit with power management and configuration tasks (ME)
- DDR4 SDRAM
- Clock Generators for CPU and interface clocks
- XSPI flash as boot or storage device
- eMMC flash as boot or storage device
- I²C EEPROM
- I²C temperature sensor
- I²C RTC
- Voltage regulators for onboard generated voltages

3.3 SoC

There are several variants of the LX2160A SoC available from NXP.

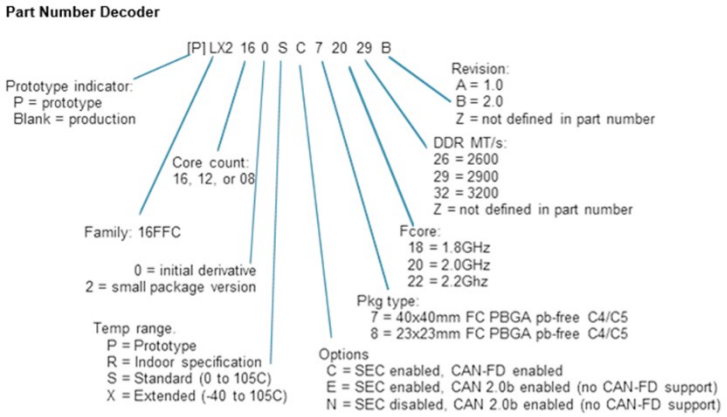


Figure 3-2 LX2160A part numbering system

For availability of different versions ask your local sales representative.

3.4 Power Consumption

The MPX-LX2160A can be supplied by a single input power rail ranging from 5V to 12V. The efficiency of the voltage regulators differs in that range.

Power Measurements, VIN = 12V, CRX-08 Carrier with single RJ45 1G Ethernet for measurement data transfer:

Stress Level	T_{amb} [°C] (steady state climate chamber)	T_j [°C] from internal Probe in Cluster 6/7	P_{total} [w]	$P_{vdd/vddq}$ [w]	P_{remain} [w] (other voltages, 1V2, 1V8, etc.)
idle	-40	3	18,528	9,150	9,378
stress	-40	9	34,124	25,944	8,180
idle	-20	10	18,792	9,128	9,664
Stress	-20	23	34,527	25,709	8,818
idle	0	26	18,984	9,345	9,639
stress	0	40	35,167	25,928	9,239
idle	20	49	19,705	9,963	9,742
stress	20	62	36,100	26,577	9,523
idle	40	75	21,845	11,648	10,197
stress	40	83	38,995	28,725	10,270
idle	50	78	22,113	11,960	10,153
stress	50	94	40,644	30,194	10,450

Table 3-1: Power Consumption over Tj Range

Linux Stress: stressapptest (https://github.com/stressapptest/stressapptest) (start parameters: -M 8192 -s 120, all cores)

Linux idle: without power optimization – based on LSDK 20.12 (U-Boot + AFT), LSDK 20.04 (Linux) without modifications.

3.5 Cooling

The cooling solution needs to be designed with the final use case in mind. If desired, MicroSys Electronics GmbH can support you with your cooling concept. Please ask your sales representative or send an email inquiry to support@microsys.de.

The following maximum component temperatures should not be exceeded.

Commercial temperature grade (0/+70° C) variants:

Component	Temperature (max.)	Description
SoC	105° C	Junction Temperature
SoC	70° C	Junction Temperature during secure fuse programming
DDR	85° C	Case Temperature
Core Regulator	150° C	Junction Temperature

Table 3-2 Commercial grade variants: maximum temperature

Industrial temperature grade (-40/+85° C) variants:

Component	Temperature (max.)	Description
SoC	105° C	Junction Temperature
SoC	70° C	Junction Temperature during secure fuse programming
DDR	95° C	Case Temperature
Core Regulator	150° C	Junction Temperature

Table 3-3 Industrial grade variants: maximum temperature

3.6 Ordering Information

Ordering information can be found on the following website

miriac MPX-LX2160A

or contact your local sales representative.

4 Technical Description

4.1 Connector References

Reference	Function	Ass	Mating Parts
ST1	Module connector Samtec SEAF-50-05.0-L-08-2-A-K-TR	✓	SEAM-50-02.0-L-08-2-A-K-TR
ST2	Module connector Samtec SEAF-50-05.0-L-08-2-A-K-TR	✓	SEAM-50-02.0-L-08-2-A-K-TR
ST3	SODIMM TE-2309409-2		SODIMM module
ST4	SODIMM TE-2309409-2		SODIMM module
ST5	Fan connector Würth Electronic WE-648-104-131-822	✓	WE-648-104-113-322
ST6	Fan connector Würth Electronic WE-648-104-131-822	✓	WE-648-104-113-322
ST7	Programming connector Würth Electronic WE-648-104-131-822	✓	WE-648-104-113-322

Table 4-1 Connector reference overview

The Samtec board-to-board connectors allow for some mounting height adjustment. Not all mated height combinations are permitted, however. The following figure shows mating combinations.

MATED HEIGHTS				
SEAM LEAD STYLE	SEAF LEAD STYLE			
	–05.0	–06.0	–06.5	–07.5
–02.0	7 mm	8 mm	8.5 mm	9.5 mm
–03.0	8 mm	9 mm	9.5 mm	10.5 mm
–03.5	8.5 mm	9.5 mm	10 mm	11 mm
–06.5	11.5 mm	12.5 mm	13 mm	14 mm
–07.0	12 mm	13 mm	13.5 mm	14.5 mm
–09.0	14 mm	15 mm	15.5 mm	16.5 mm
–11.0	16 mm	17 mm	17.5 mm	18.5 mm

Figure 4-1 Samtec – Mated Heights

4.2 Module Connector Pinout and Electrical Characteristics

NOTE

The signal direction is from the module's view. For example TDO (pin ST1:A19) is an output from the module and an input to peripheral devices on the carrier board.

ATTENTION

The following pinout is specific to the MPX-LX2160A module and its variants.

Nevertheless, different variants do not claim to be pin compatible. Individual modules may have deviating assignments for some functions, however power and ground are always assigned to the same pins.

For detailed connector pinning, as well as electrical characteristics (such as series and parallel elements, impedances, signal lengths, etc.) refer to the spreadsheet:

"**Pinning-Modulstecker_R2.xls**"

4.3 Connectors on Module

4.3.1 Fan Connectors [ST5, ST6]

There are 2 identical connectors:

Part:	ST5, ST6
Manufacturer:	Würth Electronic
Type:	WE-648-104-131-822
mating	WE-648-104-113-322

ST5 / ST6			
Pin	**Signal**	**I/O Range**	**Signal Conditioning**
1	GND		
2	VFAN	5/12V	Power supply
3	TACHO	5V	Speed of fan
4	PWM	5V	Controls fan speed

Table 4-2 Fan connector: Pinout and pin assignments

4.3.2 Programming Connector [ST7]

Programming connector for management engine (ME) microcontroller. Production use at MicroSys - do not use unless instructed by MicroSys.

Part:	ST7
Manufacturer:	Würth Electronic
Type:	WE-648-106-131-822
mating	WE-648-104-113-322

ST7			
Pin	**Signal**	**I/O Range**	**Signal Conditioning**
1	GND		
2	SWDIO	3,3V	For production use only – do not connect
3	SWCLK	3,3V	For production use only – do not connect
4	SOUT1	RS232	For production use only – do not connect
5	SIN1	RS232	For production use only – do not connect
6	GND		

Table 4-3 Programming Connector: Pinout and pin assignments

4.4 Management Engine (ME)

The management engine is handled by a Renesas S128 microcontroller R7FS128783A01CFM.

The microcontroller (µC) is responsible for power sequencing and supervision, configuration of on-board supplies, voltage monitoring and safety as well as security aspects.

The microcontroller's firmware can be modified for customer specific applications on request.

4.4.1 System Startup

On application of an input voltage, the µC is the first component to start (once VIN >= 3.0V). The uC runs the initialization and setup for

- Clock Generator
- Temperature Sensor Limits
- Fan Controller
- Checking programmed values of Power Switches for VDD and VDDQ

After a successful setup and check, the uC will start the Power Sequencer which monitors all Power Rails. Next, the VDD and VDDQ are ramped up, so that the SoC is powered. Finally, the CPLD is instructed to select the RCW source and release the PowerOn Reset to the SoC.

The complete System Startup Sequence takes around 240msec.

4.4.2 System Monitoring

The ME is one part of the complex System Monitoring. Others are

- Power Switches for VDD and VDDQ are monitoring their own voltages.
- Power Sequencer checks voltages are in range (see 4.6.1).
- Temperature Sensors are monitoring temperatures against set limits.

The components are all able to shut down the system on their own. The ME collects all information for 'black box recording' of emergency shutdowns.

The SoC fan speed is determined by SoC temperature readings.

All the different voltage, fan and temperature sensors are read by the ME in a cyclic loop. By setting lower limits than those used for a hard shutdown, the ME can react earlier to potential problems and inform the SoC thus allowing it to take evasive action.

4.4.3 XML Configuration

The ME is setting and monitoring the various sensors in the System based on an XML configuration file. This XML file is parsed and included in the Firmware during compilation - this saves memory that would otherwise be consumed in the µC. In a future version of Firmware, it is planned to have an upload option for an externally generated configuration.

Example for setting the SoC Temperature Sensor limits:

```
<!-- Temp Sensor. Local Chip Sensor -->
<sensor name="MON_CPU_L" number="21" interval="1000"
     flags="dont_check"
     record="analog"
     bus="I2C0"
     address="0x48"
     device="sa56004">
     <formula
          raw="(value/0.125)*32.0"
          cooked="(value/32.0)*0.125"/>
     <!-- The limits are set to the ALERT Temperature if mux==0xFF
          T_CRIT will be set 15.0C above ALERT if mux==0xFF
          Otherwise set by Format B mux value -->
     <limits mode="cooked" lower="-20.0" upper="85.0"/>
     <port instance="A">          <!-- Format A = read temp -->
          <pin number="0x00"/>              <!-- Local Temp High Register -->
          <pin number="0x22"/>              <!-- Local Temp Low  Register -->
          <pin number="0x02"/>              <!-- Status Register -->
     </port>
     <port instance="B">          <!-- Format B = setpoint write register -->
          <pin number="0x0B" mux="0xFF"/>    <!-- Local High Setpoint Register = upper -->
          <pin number="0x0C" mux="0xFF"/>    <!-- Local Low  Setpoint Register = lower -->
          <pin number="0x20" mux="0xFF"/>    <!-- Local T_CRIT Setpoint Register = upper+15 -->
     </port>
</sensor>
```

The sensor MON_CPU_L will be read every 1000msec from the I²C device SA56004 at 0x48. The above example sets the Warning temperature to 85°C and Critical Alert to 85+15°C = 100°C. The user can modify these values depending on the chosen cooling solution.

4.4.4 Command Console

As the ME is monitoring a lot of sensors and setting up the surrounding components, a command console has been added to the ME to configure, upload, view and modify the setup. In production systems, the command console is used to upload CPLD images and setup the Power Sequencer.

The command console uses 115200Bd, 8N1, no handshake. Startup messages are kept short to reduce System boot time:

```
MPX-LX2160A MCU
 Coldstart (Power-On-Reset)
  82: PWR_UP_START
  87: PWR_UP_CHECK_VIN
  93: PWR_UP_SWITCH_ON
 112: PWR_UP_ON_DELAY
 117: PWR_UP_VIN_EN
 120: check_limits complete
 156: set PWR_UP_DONE

=>
```

The example above shows a Coldstart. The numbers at the beginning of a line show milliseconds since start of the µC. In this example the Power Up Done is set after 156msec. Then the Power Sequencer ramps all the Power Rails step by step.

`=>` Is the command prompt.

The following examples are showing the values for the Module on a CRX08-R1 and ME version 0.5:

```
=> version

ME Information:
 Manufacturer: MicroSys Electronics GmbH
 Product     : Management Engine MCU on LX2160A
 Version     : 0.5 for MPX-LX2160A
```

4.4.4.1 Command overview and help

```
=> ?
Commands in this monitor

           help: show commands
              ?: show commands
         status: board status
      clock_cfg: show clock generator (Si5332) configuration
      power_off: set power off
       power_on: set power on
      power_cfg: show power switch (ISL68301) configuration
  power_bb_erase: erase power sequencer (ADM1266) BlackBox Log. Usage:
power_seq_erase <key>
       power_bb: show power sequencer (ADM1266) Black Box Log
      power_seq: show power sequencer (ADM1266)
          power: show power
         vdd_on: switch VDD 0.8V on
        vdd_off: switch VDD 0.8V off
          quiet: Don't monitor anything on I2C and PMBUS until hit Return
        monitor: show all controller status
            fan: show fan
           temp: show temperatur
           oszi: Oszilloskop VDD-Pout VDDQ-Pout TP2-Temperature
     cpld_flash: show SPI-NOR Flash information for CPLD
                 Parameter: <load address (default 10000 (hex))>
  cpld_download: download CPLD image via Kermit to SPI-NOR Flash
                 Parameter: <load address (default 10000(hex))>
      cpld_dump: dump CPLD SPI-NOR Flashimage
                 Parameter: <load address (default 10000 (hex))>
     cpld_erase: erase SPI-NOR Flash
     cpld_reset: reset CPLD via PROGRAMN
           cpld: show cpld status
```

```
        version: show versions
      scan_i2c: Scan I2C Busses
write_seq_config: write ADM1266 Sequencer Configuration
    write_seq_fw: write ADM1266 Sequencer Firmware and Configuration
   write_seq_rtc: set ADM1266 RTC Time
    read_seq_rtc: read ADM1266 RTC Time
 config_isl68301: write the default ISL68301 Power Switch Configuration
             rtc: read RTC or set RTC: rtc set year:month:day hour:min:sec
            time: show time & date based on System Start Time
```

4.4.4.2 I²C Bus scanning

It will scan the 3 I²C busses of the µC and show all devices found. This is important for debugging if an I²C chip is dead or a bus not reacting for some reason. The I2C-SYSTEM is the I²C Bus connected to the LX2160A and can also be read from the µC.

```
=> scan_i2c

I2C-MON-CFG:
20 2c 41 48 4a 4c 50 6a
I2C-SYSTEM:
42 48 4a 4c 50 51 55
I2C-PMBUS:
68 69 6a
```

4.4.4.3 Clock Generator Configuration

The Clock Generator is one of the first elements initialized by the ME. The configuration can be read out:

```
=> clock_cfg

Si5332-GM3 Clock Information:
I2C Dev ID : 0x37
I2C Derivate: 0xd0
I2C Ana ID : 0x40
I2C ROM ID : 0x03
Dev PN Base : 0x00
Dev Revision: 0x31
Dev Grade : 0x01
Factory OPN : 0x000002
I2C_ADDR : 0x6a
Status : ACTIVE
PLLRefFreq : 25 MHz
VCOFreq : 2500 MHz
Out0 Freq : 125.000 MHz CMOS on positive output only 50 Ohm. Output Enabled
Out1 Freq : 100.000 MHz HCSL 50 Ohm (int. termination). Output Enabled
Out2 Freq : 0.000 MHz HCSL 50 Ohm (int. termination). Output Disabled
Out3 Freq : 100.000 MHz CMOS on positive output only 50 Ohm. Output Enabled
Out4 Freq : 100.000 MHz HCSL 50 Ohm (int. termination). Output Enabled
Out5 Freq : 100.000 MHz HCSL 50 Ohm (int. termination). Output Enabled
Out6 Freq : 100.000 MHz HCSL 50 Ohm (int. termination). Output Enabled
Out7 Freq : 100.000 MHz HCSL 50 Ohm (int. termination). Output Enabled
Out8 Freq : 100.000 MHz HCSL 50 Ohm (int. termination). Output Enabled
Out9 Freq : 161.132 MHz HCSL 50 Ohm (int. termination). Output Enabled
Out10 Freq : 156.250 MHz HCSL 50 Ohm (int. termination). Output Enabled
Out11 Freq : 156.250 MHz HCSL 50 Ohm (int. termination). Output Enabled
```

Please see 0 for the Clock Structure.

4.4.4.4 Power Switch (VDD and VDDQ)

Read out the Power Switch configuration for the VDD (0.85V) and VDDQ (1.2V) switches.

Two value types can be seen. One is the 'Cyclic updated Sensor' value, which are the values monitored by the ME during runtime. The Register Values are the values read during this command execution.

```
=> power_cfg

ISL68301 Power Switch Information:

ISL Device 0:
 I2C Address          = 0x68
 DEVICE_ID            = 0x49a02f00

Cyclic updated Sensor values:
 VOUT nominal         = 0.849V
 VOUT trim            = 0.000V
 VIN                  = 12.312V
 VOUT                 = 0.848V
 IIN                  = 0.356A
 IOUT                 = 4.546A
 PIN                  = 4.476W
 POUT                 = 3.847W

Register values:
 OPERATION            = 0x80
 ON_OFF_CONFIG        = 0x1e
 VOUT_COMMAND         = 0.849 V
 READ_VOUT            = 0.848 V
 READ_IOUT            = 4.445 A

 VOUT_TRIM            = 0.000 V
 VOUT_MAX             = 0.920 V
 VOUT_OV_FAULT_LIMIT  = 0.934 V
 VOUT_OV_WARN_LIMIT   = 0.917 V
 VOUT_UV_FAULT_LIMIT  = 0.658 V
 VOUT_UV_WARN_LIMIT   = 0.722 V
 VIN_OV_FAULT_LIMIT   = 16.000 V
 VIN_OV_WARN_LIMIT    = 15.500 V
 VIN_UV_FAULT_LIMIT   = 4.500 V
 VIN_UV_WARN_LIMIT    = 4.796 V
 IOUT_OC_FAULT_LIMIT  = 30.000 A
 IOUT_OC_WARN_LIMIT   = 21.000 A
 IOUT_AVG_OC_FAULT_L  = 24.000 A
 READ_TEMPERATURE_1   = 47.750 C
 READ_TEMPERATURE_2   = 0.000 C
 READ_TEMPERATURE_3   = 46.562 C
 FREQUENCY_SWITCH     = 500.000 KHz
 READ_FREQUENCY       = 500.000 KHz

ISL Device 1:
 I2C Address          = 0x69
 DEVICE_ID            = 0x49a02f00

Cyclic updated Sensor values:
 VOUT nominal         = 0.849V
 VOUT trim            = 0.000V
 VIN                  = 12.312V
 VOUT                 = 0.848V
 IIN                  = 0.359A
 IOUT                 = 4.570A
 PIN                  = 4.398W
 POUT                 = 3.843W

Register values:
 OPERATION            = 0x80
 ON_OFF_CONFIG        = 0x1e
 VOUT_COMMAND         = 0.849 V
 READ_VOUT            = 0.849 V
 READ_IOUT            = 4.515 A

 VOUT_TRIM            = 0.000 V
 VOUT_MAX             = 0.920 V
 VOUT_OV_FAULT_LIMIT  = 0.934 V
 VOUT_OV_WARN_LIMIT   = 0.917 V
 VOUT_UV_FAULT_LIMIT  = 0.658 V
 VOUT_UV_WARN_LIMIT   = 0.722 V
 VIN_OV_FAULT_LIMIT   = 16.000 V
```

```
 VIN_OV_WARN_LIMIT   = 15.500 V
 VIN_UV_FAULT_LIMIT  = 4.500 V
 VIN_UV_WARN_LIMIT   = 4.796 V
 IOUT_OC_FAULT_LIMIT = 30.000 A
 IOUT_OC_WARN_LIMIT  = 21.000 A
 IOUT_AVG_OC_FAULT_L = 24.000 A
 READ_TEMPERATURE_1  = 46.187 C
 READ_TEMPERATURE_2  = 0.000 C
 READ_TEMPERATURE_3  = 44.875 C
 FREQUENCY_SWITCH    = 500.000 KHz
 READ_FREQUENCY      = 500.000 KHz

ISL Device 2:
 I2C Address         = 0x6a
 DEVICE_ID           = 0x49a02f00

Cyclic updated Sensor values:
 VOUT nominal        = 1.199V
 VOUT trim           = 0.000V
 VIN                 = 12.312V
 VOUT                = 1.199V
 IIN                 = 0.139A
 IOUT                = 1.105A
 PIN                 = 1.716W
 POUT                = 1.332W

Register values:
 OPERATION           = 0x80
 ON_OFF_CONFIG       = 0x1e
 VOUT_COMMAND        = 1.199 V
 READ_VOUT           = 1.199 V
 READ_IOUT           = 1.109 A

 VOUT_TRIM           = 0.000 V
 VOUT_MAX            = 1.339 V
 VOUT_OV_FAULT_LIMIT = 1.319 V
 VOUT_OV_WARN_LIMIT  = 1.284 V
 VOUT_UV_FAULT_LIMIT = 0.929 V
 VOUT_UV_WARN_LIMIT  = 1.020 V
 VIN_OV_FAULT_LIMIT  = 16.000 V
 VIN_OV_WARN_LIMIT   = 15.500 V
 VIN_UV_FAULT_LIMIT  = 4.500 V
 VIN_UV_WARN_LIMIT   = 4.796 V
 IOUT_OC_FAULT_LIMIT = 30.000 A
 IOUT_OC_WARN_LIMIT  = 27.000 A
 IOUT_AVG_OC_FAULT_L = 28.000 A
 READ_TEMPERATURE_1  = 41.062 C
 READ_TEMPERATURE_2  = 0.000 C
 READ_TEMPERATURE_3  = 39.750 C
 FREQUENCY_SWITCH    = 500.000 KHz
 READ_FREQUENCY      = 500.000 KHz
```

4.4.4.5 Power Sequencer

This shows the state of the state-machine and the actual values of the voltage sensors and signals the Power Sequencer is monitoring.

```
=> power_seq
Device ID n=3 421266
ADM1266 in Normal Mode
Chip Revision 3B
Bootload Revision 0.0.9
Firmware Revision 1.14.3
Status Word: $0000
STATUS_VOUT $00
STATUS_CML $00
ADM_STATUS_MFR_SPEC $04
 PART_LOCKED: device is locked.
No Faults or Warnings in System
ADM1266 at Address 0x41 is refreshed 0 time(s) since power-up
ADM1266 at Address 0x41 saw CRC Error 0 time(s) since power-up
MFR_ID for ADM1266 at Address 0x41 is : Analo2
```

```
MFR_MODEL for ADM1266 at Address 0x41 is : ADM12
MFR_REVISION for ADM1266 at Address 0x41 is : 0.1T
MFR_LOCATION for ADM1266 at Address 0x41 is : San JR
MFR_DATE for ADM1266 at Address 0x41 is : 200717
MFR_SERIAL for ADM1266 at Address 0x41 is : 0001-
User_Data for ADM1266 at Address 0x41 is : CRX08
10, 4294967295.4294967295
0

No Faults or Warnings in System

ADM1266 at Address 0x41 is in 'VDD_good' State

Telemetry
------------------------------------------------------------------------
Rails
------------------------------------------------------------------------
VIN - 11.961 V
VCC5V0 - 0.000 V
VCC3V3 - 3.304 V
VCC3V3SBY - 3.317 V
VCC2V5 - 2.478 V
VCC1V8 - 1.793 V
VDDQ - 1.197 V
VCC1V2 - 3.304 V
DRAMVREF2 - 0.601 V
USBSVDD - 0.805 V
VDD - 0.853 V
VTT1 - 0.603 V
VTT2 - 0.605 V
DRAMVREF1 - 0.599 V
SDOVDD - 1.784 V
SDSVDD - 0.895 V
EVDD - 1.780 V
------------------------------------------------------------------------
Signals
------------------------------------------------------------------------
VDDQ_FAULTn - 1
VDD_FAULT1n - 1
VDD_FAULT2n - 1
SIG_PWRMNG - 1
TEMP_CRITn - 1
STAT_PGOOD - 1
RESET_OUT_SEQn - 1
POWER_FAILn - 1
POWER_GOOD - 1
POR_RESETn - 1

------------------------------------------------------------------------
=>
```

It can be seen above that the Sequencer is in the VDD_good state.

The Sequencer includes a Block Box Logging, to record bad events such as Over Temperature (SYST_Crit Signal) or a Power-Fault of a single power line (not caused by a Power-Off).

```
=> power_bb
No BlackBox Log Entries
```

This is the good state. On Fault all Rails and Signals of the Sequencer are shown with a date/time (the date/time is set with the system RTC time on startup). The time in the Sequencer can be read and set with

```
=> read_seq_rtc
SEQ Time: Tue Feb  9 08:06:46 2021

=> write_seq_rtc
Sequencer RTC set
```

The *write_seq_rtc* sets the time read from the system RTC.

4.4.4.6 Power & Temp & Fan & Monitor & RTC

power is used to view the actual voltage and current readings:

```
=> power

ISL: VIN    VOUT0  IOUT0  VOUT1  IOUT1  VOUT2  IOUT2
     12.296 0.848  4.492  0.848  4.531  1.199  1.107

MCU: 1V2    2V5    SVDD   OVDD   1V8    3V3    VDD
     1.191  2.449  0.884  1.780  1.782  3.284  0.845
```

fan shows the Fan Controller:

```
=> fan

Fan Controller information:
Tacho Cnt 170 = 5782 RPM
PWM Duty 160 = 31%
```

temp shows the temperature readings on the local µC Bus and the LX2160 Bus

```
=> temp

Temperature sensor readings on MONitor Bus
CPU2 sensor :  40.750
      local :  32.500
CPU  sensor :  33.625
      local :  34.625
DRAM sensor :  25.625
      local :  28.125

Temperature sensor readings on SYSTem Bus
CPU1 sensor :  39.250
      local :  36.750
DRAM sensor :  35.625
      local :  37.0
VDD  sensor :  36.500
      local :  37.750
```

monitor will show all the 3 sensors in one.

```
=> monitor
ISL: VIN    VOUT0  IOUT0  VOUT1  IOUT1  VOUT2  IOUT2
     11.921  0.849  4.375  0.849  4.367  1.199  0.998

MCU: 1V2    2V5    SVDD   OVDD   1V8    3V3    VDD
     1.200  2.464  0.902  1.788  1.784  3.293  0.850

Temperature sensor readings on MONitor Bus
CPU2 sensor :  41.0
      local :  32.750
CPU  sensor :  33.875
      local :  34.750
DRAM sensor :  25.875
      local :  28.625
```

```
Temperature sensor readings on SYSTem Bus
CPU1 sensor :  39.625
      local :  36.875
DRAM sensor :  35.750
      local :  37.125
VDD  sensor :  36.625
      local :  38.125

Fan Controller information:
Tacho Cnt 195 = 5041 RPM
PWM Duty 119 = 23%
```

config_isl68301 is a command for production to check and write the Configuration of the 3 main power regulators (2x VDD and 1x VDDQ).

rtc is used to get and set the time of the system RTC.

```
=> rtc
RTC Time: Tue Feb  9 08:18:32 2021

=> rtc set
Usage: rtc set year:month:day hour:min:sec
=> rtc set 21:02:09 08:17:30
RTC Time: Tue Feb  9 08:17:30 2021
```

Time shows the system start time and the calculated actual time base on start time + seconds since start. This command is not reading the system RTC.

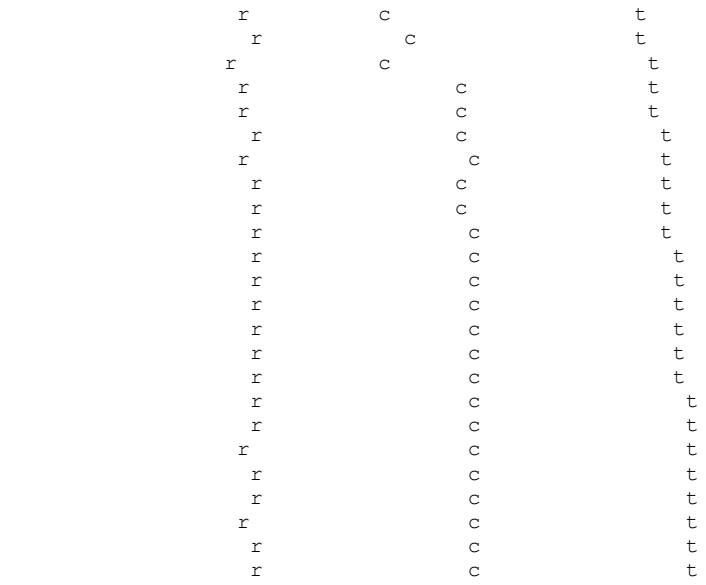
```
=> time
System Start: Tue Feb  9 07:29:25 2021

Actual Time : Tue Feb  9 08:19:06 2021
```

4.4.4.7 Oscilloscope

As the ME is cyclically measuring the two main Power Rails (CPU and DRAM), as well as the CPU temperature, the *oszi* command (German abbreviation for oscilloscope) shows the actual POUT of VDD and VDDQ, plus the temperature.

The cursor position (X axis) is the power in Watts or the temperature in °C. For a better visualisation, VDDQ-POUT is multiplied by 4 on the X axis marked with ‘r’ for RAM, VDD-POUT multiplied by 2 with ‘c’ for CPU and the temperature with x1 marked ‘t’.

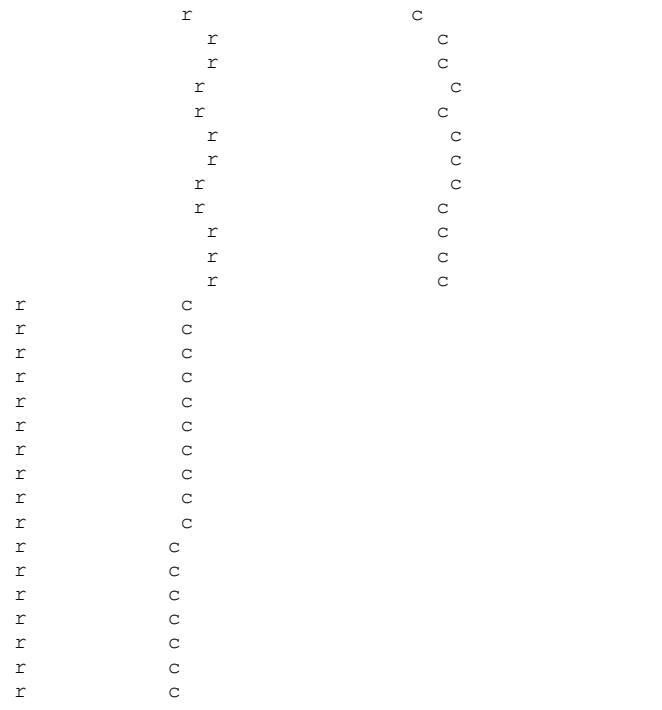
```
=> oszi
Oszi: Core VDD-POUT x2 'c' RAM VDDQ-POUT x4 'r' TP2 Temperature x1 't'
     r         c                                t
     r         c                                t
     r         c                                t
     r         c                                t
     r         c                                t
     r         c                                t
     r         c                                t
     r         c                                t
     r         c                                t
     r         c                                t
     r         c                                t
                   r         c                  t
                    r         c                 t
                    r         c                 t
                   r          c                  t
                   r          c                  t
                   r          c                  t
```

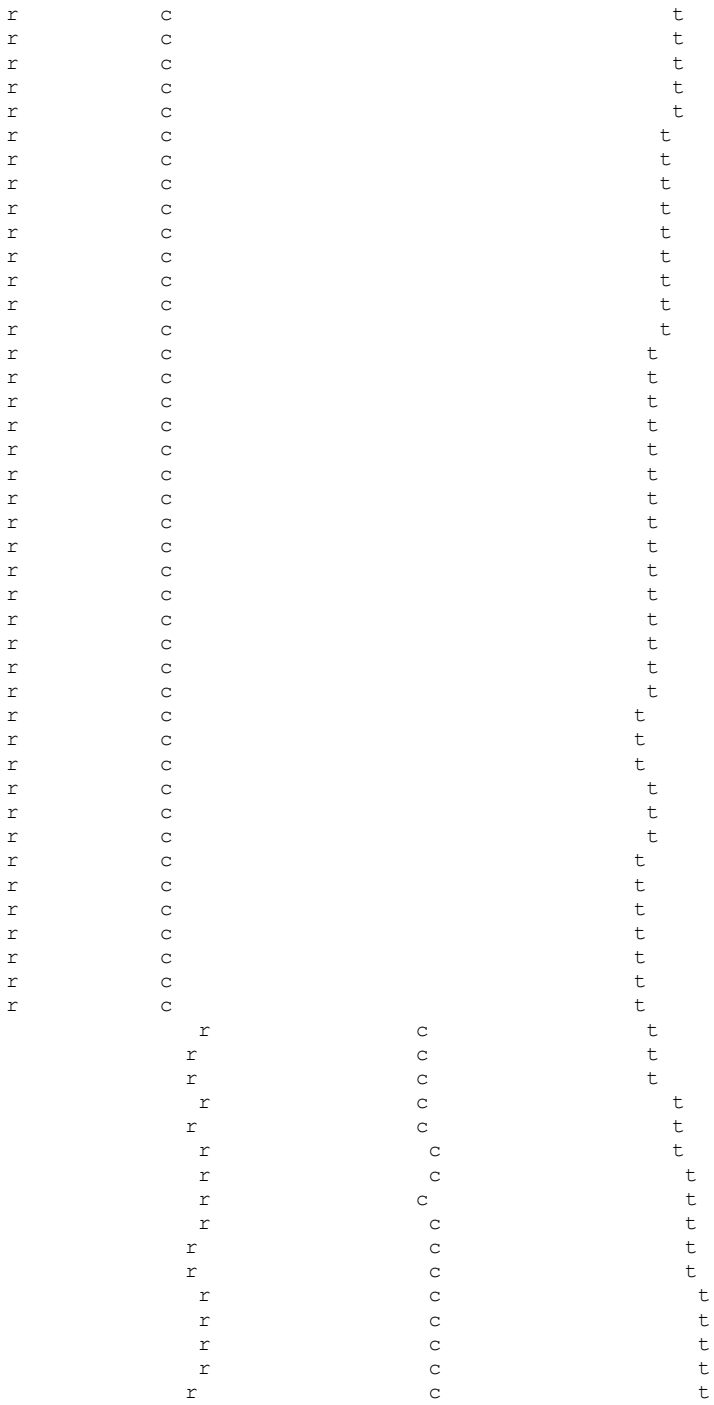


The above output from the oszi command is taken while a *stressapptest -s 1200* is running on the LX2160A. In line 12 above, the power for RAM and CPU immediately jumps and the core temperature will follow with some delay.

In the oszi output below, it can be seen where the *stressapptest* stops all working threads to generate a Power Spike, both positive and negative, for testing the Power Switches. The RAM and CPU loads both drop.

```
2020/09/18-18:17:22(UTC) Log: Seconds remaining: 820
2020/09/18-18:17:32(UTC) Log: Seconds remaining: 810
2020/09/18-18:17:42(UTC) Log: Seconds remaining: 800
2020/09/18-18:17:42(UTC) Log: Pausing worker threads in preparation for
power spike (800 seconds remaining)
2020/09/18-18:17:52(UTC) Log: Seconds remaining: 790
2020/09/18-18:17:57(UTC) Log: Resuming worker threads to cause a power spike
(785 seconds remaining)
2020/09/18-18:18:02(UTC) Log: Seconds remaining: 780
2020/09/18-18:18:12(UTC) Log: Seconds remaining: 770
2020/09/18-18:18:22(UTC) Log: Seconds remaining: 760
```





This is a useful feature for checking the cooling concept.

4.4.4.8 CPLD commands

The CPLD is loaded from an external SPI NOR Flash during startup. The Flash is written via the ME by using the *cpld_download* command which is awaiting an upload of the .bit file using the Kermit protocol.

The other *cpld_** commands are for obtaining the status of the CPLD and to erase or read the Flash Data.

4.4.4.9 Sequencer configuration

The sequencer is programmed with the firmware and configuration during manufacturing. The firmware and config are compiled into the ME firmware and cannot be modified without rebuilding the ME firmware. The commands *power_bb_erase*, *write_seq_fw* and *write_seq_config* are available, but not really usable for Users, as it will just rewrite the power sequencer with the same data.

4.5 CPLD

Additional on-board logic and reset chains are handled by a Lattice MachX03 CPLD,

Type LCMXO3LF-1300C-5BG256I.

The CPLD’s firmware can be modified for customer specific applications on request.

4.6 Power Structure

The MPX-LX2160A module is powered by a single supply. Optionally, the on-module real-time clock can be supplied via a dedicated backup power source if the system time needs to be preserved.

The following diagram shows the structure of the power supplies:

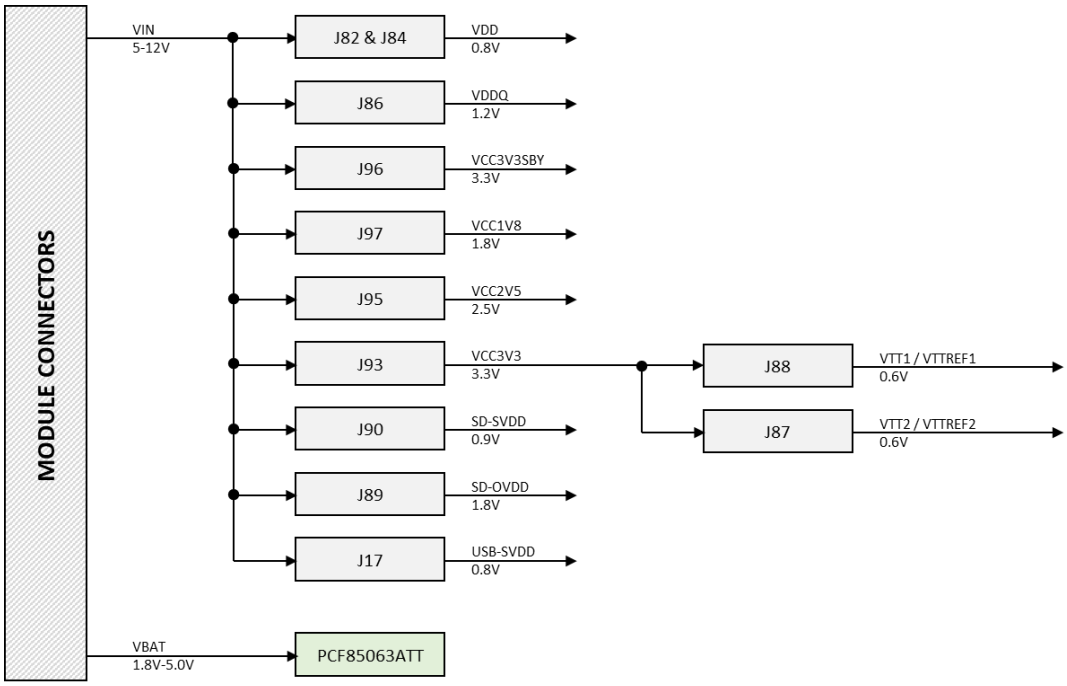


Figure 4 Power supply structure

The power rails are listed in chapter 4.6.1

4.6.1 Power Monitoring

The management controller and power sequencer are monitoring certain on-board voltages and reset the module in case any voltage is out of range:

Name	Voltage	max. Current	Monitoring Range	Comment
VIN	12V		4.56 – 13.46V	SOM Input Voltage
VCC3V3	3.3V	6A	3.01 – 3.53V	
VCC3V3SBY	3.3V	2A	2.09 – 3.82V	Permanent Power
VCC2V5	2.5V	1A	2.20 – 2.72V	
VCC1V8	1.8V	4A	1.50 – 2.00V	
VCC1V2	3.3V (or 1.2, 2.5)	1A	1.10 – 3.53V	CPLD IO Voltage default VCC3V3SBY
VDD	0.775 – 0.85V	53A	0.66 – 0.92V	Core Voltage
VDDQ	1.2V	28A	0.93 – 1.34V	DDR4 Voltage
VTT1	0.6V	3.5A	0.46 – 0.72V	DDR Controller 1 VTT
VTT2	0.6V	3.5A	0.46 – 0.72V	DDR Controller 2 VTT
USBSVDD	0.8V	1.5A	0.73 – 0.95V	
SDSVDD	0.9V	4A	0.78 – 1.04V	
SDOVDD	1.8V	5A	1.63 – 1.97V	
DRAMVREF1	0.6V	40mA	0.49 – 0.75V	VTTREF 1
DRAMVREF2	0.6V	40mA	0.49 – 0.75V	VTTREF 2
EVDD	1.8V	1.5A	1.63 – 1.97V	SDOVDD

Table 4-4 Voltage monitoring limits

4.7 Reset Structure

The module's reset chains are handled by the integrated CPLD. It also handles some aspects of the boot source selection.

The following pins are used to control the module's reset chain:

Module Connector		Description			
Pin	**Signal**	**I/O**	**I/O Range**	**Signal conditioning**	**Function**
ST1: C4	PORESET#	IN	1.8V	CPU 4k7 PU	CPU power on reset, low active
ST1: C5	HRESET#	IN / OUT	1.8V	CPU 4k7 PU	Bidirectional hard reset, low active
ST1: C10	RESET_REQ#	OUT	1.8V	CPU 4k7 PU	Reset request to the CPU driven by the CPLD, low active
ST1: A16	TRST_B	IN	1.8V	CPLD	JTAG reset, low active
ST1: A10	RESIN#	IN	1.8V	CPLD (PU)	Reset input, used to trigger a module reset, low active
ST1: A9	RESET_OUT#	OUT	1.8V	CPLD	Reset output, used to reset peripheral devices on the carrier, low active
ST1: D41	RST_PHY#	OUT	1.8V	CPLD	Reset for Ethernet PHYs, low active
ST2: D21	RST_XSPI#	OUT	1.8V	CPLD	Reset for XSPI flashes, low active
ST2: H21	RST_OUT1_B	OUT	1.8V	CPLD	t.b.d, low active reset
ST2: G21	RST_OUT2_DELAY_B	OUT	1.8V	CPLD	t.b.d, low active reset
ST2: F9	RST_OUT3_B	OUT	1.8V	CPLD	t.b.d, low active reset
ST2: A15	RESET-ME#	IN	3.3V STBY	ME 4k7 PU	Reset input to Management Engine. Used for production and debugging purposes
ST1: C16	POR-RESET#	IN	3.3V STBY	SEQUENCER, 10 PU	Reset input to Power Sequencer. Used for production and debugging purposes

Table 4-5 Reset pins: pin assignments

PORESET# and HRESET# are directly connected to the SoC. Any circuitry on the Carrier must ensure correct rise times and timing.
It is recommended not to use these signals. Use RESIN# and RESET_OUT# instead.

RESET_REQ# is an input to the SoC. It is connected to the module connector for monitoring purposes only.

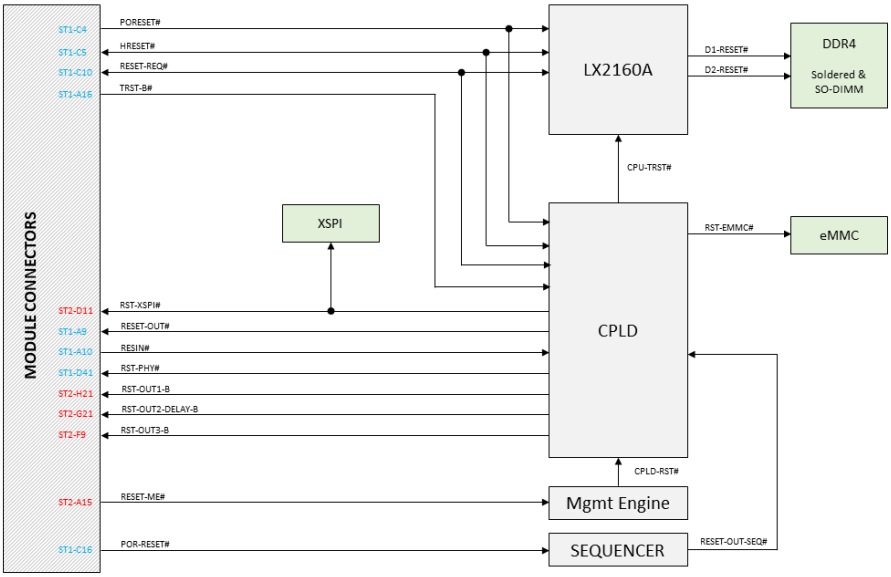


Figure 5 Reset structure

4.8 Clock Structure

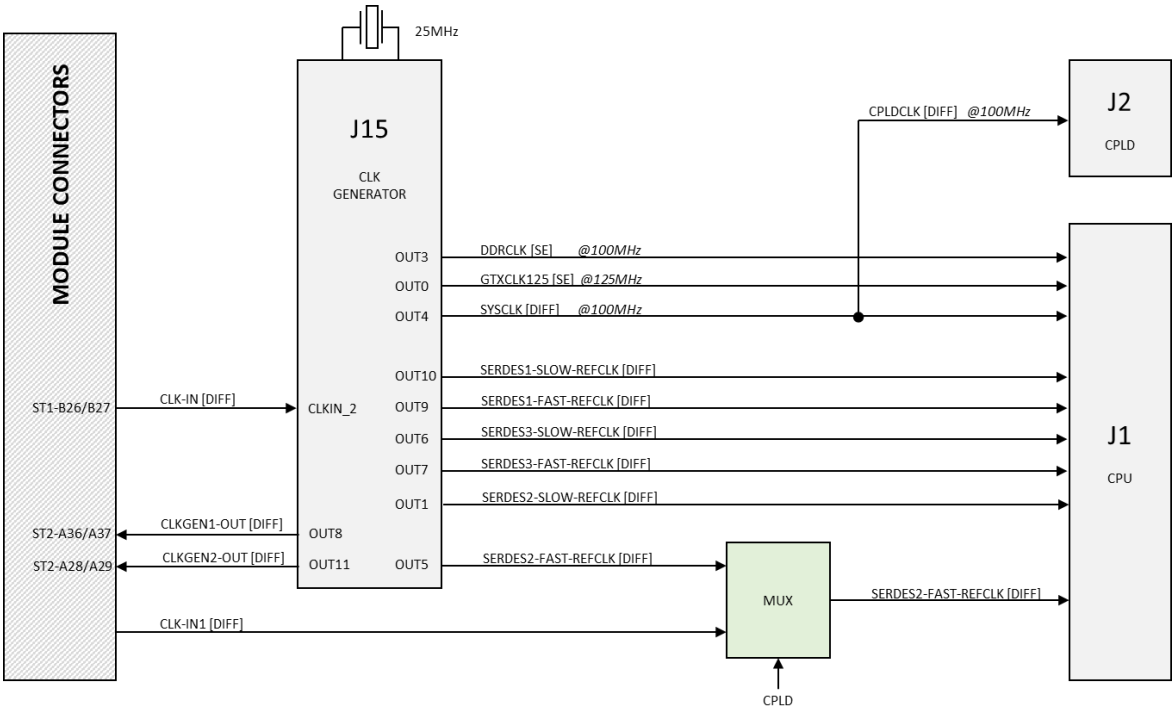


Figure 6 Clock structure

The following table lists the clocks generated on the module:

Part	Function	Frequency
J15	DDRCLK	100 MHz
J15	GTXCLK125	125 MHz
J15	SYSCLK / CPLDCLK	100 MHz
J15	SERDES1_SLOW_REFCLK	100 MHz / 156.25 MHz / 161.1328125MHz
J15	SERDES1_FAST_REFCLK	100 MHz / 156.25 MHz / 161.1328125MHz
J15	SERDES2_SLOW_REFCLK	100 MHz / 156.25 MHz / 161.1328125MHz
J15	SERDES2_FAST_REFCLK	100 MHz / 156.25 MHz / 161.1328125MHz
J15	SERDES3_SLOW_REFCLK	100 MHz / 156.25 MHz / 161.1328125MHz
J15	SERDES3_FAST_REFCLK	100 MHz / 156.25 MHz / 161.1328125MHz
J15	CLKGEN1_OUT	100 MHz / 156.25 MHz / 161.1328125MHz
J15	CLKGEN2_OUT	100 MHz / 156.25 MHz / 161.1328125MHz
Q1	Crystal	25 MHz
Q4	Crystal	32.768 kHz
Q9	Crystal	32.768 kHz
Q13	Crystal	32.768 kHz
J41	FAN RPM Controller	Varying frequency

Part	Function	Frequency
J82, J84	Regulator frequency	500 kHz
J86	Regulator frequency	500 kHz
J96	Regulator frequency	Varying frequency
J97	Regulator frequency	~820 kHz
J95	Regulator frequency	Varying frequency
J93	Regulator frequency	~850 kHz
J89	Regulator frequency	~820 kHz
J90	Regulator frequency	~820 kHz
J17	Regulator frequency	Varying frequency

Table 4-6 Clock frequencies

4.9 Boot Mode Configuration

The MPX-LX2160A module offers the option of booting from different boot devices. As previously mentioned, the boot source selection to the SoC is handled by the CPLD.

The boot source can be selected by means of following pins:

Module Connector			
Pin	**Signal**	**I/O Range**	**Signal conditioning**
ST2: A4	BOOT_SRC_SEL 0	3,3V	CPLD(PU)
ST2: A3	BOOT_SRC_SEL 1	3,3V	CPLD(PU)
ST2: A2	BOOT_SRC_SEL 2	3,3V	CPLD(PU)
ST2: A1	BOOT_SRC_SEL 3	3,3V	CPLD(PU)

Table 4-7 Boot select pins: pin assignments

Currently, five different boot devices are possible depending on BOOT_SRC_SEL[3:0] as defined below:

	SEL3	**SEL2**	**SEL1**	**SEL0**	**Boot Source**	**Description**
0xF	*1*	*1*	*1*	*1*	Flex-SPI Serial-NOR A	default
0xE	*1*	*1*	*1*	*0*	I²C EEPROM	
0xD *0x9* *0x5* *0x1*	*X*	*X*	*0*	*1*	SD Card	
0xB	*1*	*0*	*1*	*1*	eMMC	
0x7	*0*	*1*	*1*	*1*	Flex-SPI Serial-NOR B	Second NOR Flash
0xC *0xA* *0x8* *0x6* *0x4* *0x3* *0x2* *0x0*	*1* *1* *1* *0* *0* *0* *0* *0*	*1* *0* *0* *1* *1* *0* *0* *0*	*0* *1* *0* *1* *0* *1* *1* *0*	*0* *0* *0* *0* *0* *1* *0* *0*	Reserved for future use. (Currently selects SD Card)	(All remaining settings)

Table 4-8 Boot devices: overview

The reserved settings are currently set to SD Card and can change in future configurations.

4.10 Memory DRAM

There are twenty DDR4 memory chips directly soldered to the module. Depending on which parts are assembled, there may be:

- 20x (16 Data + 4 ECC) 8Gbit (512Mbx16) = 16 GBytes of DRAM
- 20x (16 Data + 4 ECC) 16Gbit (1Gbx16) = 32 GBytes of DRAM
- 20x (16 Data+ 4 ECC) 32Gbit (2Gbx16) = 64 GBytes of DRAM

Optionally, two DDR4-SODIMM modules (with ECC support) can be installed for expanding the memory by, up to, 64 GBytes. Meaning 128 GBytes DDR4 is maximum possible configuration.

		Soldered x32 D0..D31	Soldered x32 D32..D64	ECC x8	SO-DIMM
DRAM controller 1	Slot A	2..16 GByte	2..16 GByte	Opt.	
	Slot B				Up to 32GByte
DRAM controller 1	Slot A	2..16 GByte	2..16 GByte	Opt.	
	Slot B				Up to 32GByte

Table 4-9 DRAM assembly options

4.11 Memory eMMC

The MPX-LX2160A module is optionally equipped with 32GB of eMMC Flash on the SDHC2 port of the LX2160A. Different sizes may be available on request/order.

The following table shows the connections and signal levels for the eMMC Flash:

CPU			eMMC Flash THGBMHG8C4LBAU7		
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**
A23	SDHC2_DAT0	↔	A3	SDHC2_DAT0	1,8V
C24	SDHC2_DAT1	↔	A4	SDHC2_DAT1	1,8V
B23	SDHC2_DAT2	↔	A5	SDHC2_DAT2	1,8V
A24	SDHC2_DAT3	↔	B2	SDHC2_DAT3	1,8V
C26	SDHC2_DAT4	↔	B2	SDHC2_DAT4	1,8V
B27	SDHC2_DAT5	↔	B4	SDHC2_DAT5	1,8V
A26	SDHC2_DAT6	↔	B5	SDHC2_DAT6	1,8V
A27	SDHC2_DAT7	↔	B6	SDHC2_DAT7	1,8V
B25	SDHC2_CMD	↔	M5	SDHC2_CMD	1,8V
A25	SDHC2_CLK	→	M6	SDHC2_CLK	1,8V
C25	SDHC2_DS	→	H5	SDHC2_DS	1,8V

Table 4-10 eMMC Flash: pin assignments

4.12 Memory XSPI

The MPX-LX2160A module is equipped with two 1Gb XSPI Flashes, connected to LX2160A's XSPI port. Other densities are available on request/order.

The following table shows the internal connections:

CPU			XSPI Flash MT35XU512ABA1G12-0SIT		
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**
C23	XSPI_A_CS0	→	C2	CS0#	1,8V
D23	XSPI_A_CS1	→	C2	CS1#	1,8V
D22	XSPI_A_SCK	→	B2	CLK	1,8V
E23	XSPI_A_DQS	→	C3	DQS	1,8V
			B3	GND	
F25	XSPI_A_DATA0	↔	D3	D0	1,8V
E24	XSPI_A_DATA1	↔	D2	D1	1,8V
E26	XSPI_A_DATA2	↔	C4	D2	1,8V
E27	XSPI_A_DATA3	↔	D4	D3	1,8V
F27	XSPI_A_DATA4	↔	D5	D4	1,8V
D26	XSPI_A_DATA5	↔	E3	D5	1,8V
E25	XSPI_A_DATA6	↔	E2	D6	1,8V
D24	XSPI_A_DATA7	↔	E1	D7	1,8V
			B4 E4 D1	+1.8V	

Table 4-11 XSPI Flash: pin assignments

4.13 Memory SPI

The MPX-LX2160A module provides a SPI interface with a maximum of four chip selects. The signals are routed to the module connector. SPI3 cannot be used when booting from SD Card.

SoC			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
D3	SPI3_SIN	←		SPI-MISO	1,8V	SR: 0R
C4	SPI3_SOUT	→		SPI-MOSI	1,8V	SR: 0R
B2	SPI3_SCK	→		SPI-CLK	1,8V	SR: 0R
A3	SPI3_PCS0	→		SPI-CS0#	1,8V	SR: 0R
A4	SPI3_PCS1	→		SPI-CS1#	1,8V	SR: 0R
B3	SPI3_PCS2	→		SPI-CS2#	1,8V	SR: 0R
C3	SPI3_PCS3	→		SPI-CS3#	1,8V	SR: 0R

Table 4-12 SPI: pin assignments

4.14 RTC (Real-Time Clock)

The RTC is implemented with an NXP PCF85063ATT RTC chip:

- I²C clock frequency up to 400 kHz
- Operating temperature -40°C to 85°C
- Deviation ~9secs per month, ~108secs per year
- Address see chapter 4.18

If required, the RTC needs to be buffered on the carrier board. The following drawing shows the internal connection:

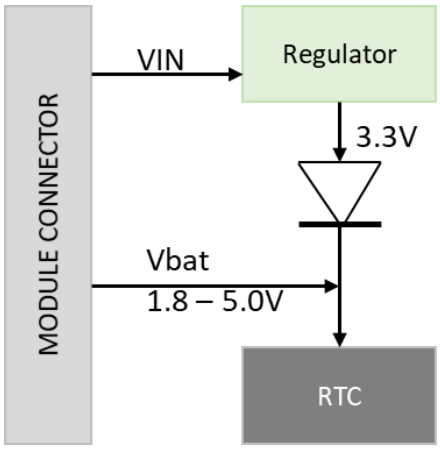


Figure 4-5 RTC: buffering

It is recommended to supply the RTC with a battery voltage of 1.8V to 5.0V. According to the PCF85063ATT's datasheet the RTC will work down to 0.9V (measured at the IC pin).

If used, please protect the battery against charging from the module.

4.15 Serdes clocking

SerDes Protocol (given lane)	Valid Reference Clock Frequency	Valid setting as determined by SRDS_PRTCL_Sn	Valid Setting as Determined by SRDS_PLL_REF_CLK_SEL_Sn	Valid Setting as Determined by SRDS_DIV_*_Sn
High Speed Serial Interfaces				
PCI Express (2.5 Gbps) (doesn't negotiate upwards)	100 MHz [1]	Any PCIe	0 100 MHz	11 2.5 Gbps
	125 MHz [1]		1 125 MHz	
PCI Express (5 Gbps) (can negotiate up to 5 Gbps)	100 MHz[1]	Any PCIe	0 100 MHz	10 5 Gbps
	125 MHz[1]		1 125 MHz	
PCI Express (8 Gbps) (can negotiate up to 8 Gbps) [1]	100 MHz[1]	Any PCIe	0 100 MHz	01 8 Gbps
	125 MHz[1]		1 125 MHz	
PCI Express (16 Gbps) (can negotiate up to 5 Gbps) [1]	100 MHz[1]	Any PCIe	0 100 MHz	00 16 Gbps
	125 MHz[1]		1 125 MHz	
SATA (1.5, or 3, or 6 Gbps)	100 MHz	Any SATA	0 100 MHz	Don't care

Figure 4-6 SerDes Clocks 1

SerDes Protocol (given lane)	Valid Reference Clock Frequency	Valid setting as determined by SRDS_PRTCL_Sn	Valid Setting as Determined by SRDS_PLL_REF_CLK_SEL_Sn	Valid Setting as Determined by SRDS_DIV_*_Sn
	125 MHz		1 125 MHz	
Networking Interfaces				
SGMII (1.25 Gbps)	100 MHz	SGMII @ 1.25 Gbps	0 100 MHz	Don't care
	125 MHz		1 125 MHz	
USXGMII/XFI ,40GE (each lane: 10.3125 Gbaud)	156.25 MHz	USXGMII/XFI, 40GE @ 10.3125 Gbaud	0 156.25 MHz	Don't care
	161.1328 125 MHz		1 161.1328125 MHz	
25GE, 50GE, 100GE (each lane: 25.78125 Gbaud)	161.1328 125 MHz		0 100 MHz	Don't care

1. A spread-spectrum reference clock is permitted for PCI Express. However, if any other high speed interface such as SGMII is used concurrently on the same SerDes bank, spread-spectrum clocking is not permitted.

Figure 4-7 SerDes Clocks 2

4.16 Temperature sensors

The LX2160A features two integrated temperature diodes which are connected to an SA56004 temperature sensor from NXP.

- I²C clock frequency up to 400 kHz
- Operating temperature -40°C to 125°C
- Local temperature monitoring
- Remote temperature monitoring
- Two processor interrupts for adjusting 2 temperature thresholds (WARN, CRIT)
- Address see list in chapter 4.18

	Ambient: 0°C / +70°C	**Ambient: -40°C / +125°C**
Local Temperature (of the sensor itself)	Max. ± 1°C	Max. ± 2°C
Remote Temperature (of the CPU internal diode)	Max. ± 1°C	Max. ± 4°C

Figure 4-8 Temperature sensor: accuracy

The temperature sensors provide two interrupts which are connected to the ME and SoC:

ME			**SA56004**				
Pin	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**	**Measured temperature**
22	*ALERTn*	←	6	ALERT#	3,3V	PU: intern	CPU-Temp 1
			6	ALERT#	3,3V	PU: intern	DRAM
			6	ALERT#	3,3V	PU: intern	VDD-Core Regulator
28	*SYST_CRITn*	←	4	CRIT#	3,3V	PU: intern	CPU-Temp 1
			4	CRIT#	3,3V	PU: intern	DRAM
			4	CRIT#	3,3V	PU: intern	VDD-Core Regulator

Table 4-13 Temperature sensor: IRQs

4.17 LEDs

Colour	Function	
LD1 Green	LED ON:	User LED, to be defined
	LED OFF:	User LED, to be defined
LD2 Green	LED ON:	State Machine Info
	LED OFF:	State Machine Fault or Running from internal Flash
	LED Flasing:	CPLD Running from external Flash
LD3 Green	LED ON:	State Machine Info
	LED OFF:	State Machine Fault or Running from external Flash
	LED Flashing:	CPLD Running from internal FLASH
LD4 Red	LED ON:	Reset / Power-On RCW Active / FAULT
	LED OFF:	State-Machine Runnning
LD5 Green	LED ON:	Power-up sequence of the module is finished, power is good
	LED OFF:	Power fail
LD6 Red	LED ON:	Module reset is active
	LED OFF:	Reset is inactive

Table 4-14 LED: pin description

4.18 I2C Devices – Address List

I2C devices on the module, connected to the LX2160A:

Bus	Address (7-bit)	Device	Function
IIC1	0x10	Synergy S128	System Controller
IIC1	0x48	SA56004ADP	Temperature Sensor, CPU die 2
IIC1	0x4A	SA56004CDP	Temperature Sensor, next to DRAM
IIC1	0x4C	SA56004EDP	Temperature Sensor, next to CPU
IIC1	0x51	PCF85063ATT	RTC
IIC1	0x50	24C01	EEPROM
IIC1	0x55	24C01	EEPROM
~~IIC1~~	~~0x69~~	~~24C01~~	~~EEPROM~~
IIC2	---	no	Shared with SDHC1
IIC3	---	no	Shared with CAN 1
IIC4	---	no	Shared with CAN 2
IIC5	---	no	Shared with SDHC1
IIC6	0x53	SODIMM 1 EEPROM	SPD EEPROM
IIC6	0x51	SODIMM 2 EEPROM	SPD EEPROM

Table 4-15 I2C: address list to SoC

For module variants without SODIMMs (or unpopulated slots), IIC6 remains empty.

4.19 I2C (PMBUS) devices at ME

I2C devices on the module, connected to ME microcontroller:

Bus	Address (7-bit)	Device	Function
MON-CFG	0x20	MAX31790	Fan Controller
MON-CFG	0x41	ADM1266	Power Sequencer
MON-CFG	0x48	SA56004ADP	Temperature Sensor, SoC die 2
MON-CFG	0x4A	SA56004CDP	Temperature Sensor, next to DRAM
MON-CFG	0x4C	SA56004EDP	Temperature Sensor, next to SoC
MON-CFG	0x50	24C01	EEPROM

Table 4-16 I2C: address list to ME (µC)

PMBUS (I2C) devices on the module, connected to ME microcontroller:

Bus	Address (7-bit)	Device	Function
PMBUS	0x68	ISL68301B	0.85V Core voltage 1st part
PMBUS	0x69	ISL68301B	0.85V Core voltage 2nd part
PMBUS	0x6A	ISL68301B	1.2V VDDQ voltage
PMBUS		ST1	External

Table 4-17 PMBUS: address list to ME (µC)

4.20 Carrier Interfaces

The interface between the MPX-LX2160A and its carrier is handled by two high-speed/high-density open-pin-field connectors (ST1, ST2) from Samtec. Each connector has 400 pins.

Pin description: **see separate spreadsheet.**

4.20.1 Module Power Input

Signal	I/O Range	Signal Conditioning
VIN	5V (-5%) up to 12V (+5%)	5 to 12A (depending on input voltage)

Table 4-18 Module Power Input

4.20.2 Power from Module to Carrier

The module provides several reference voltages to the carrier for power sequencing and tracking:

Signal	I/O Range	Signal Conditioning
VCC3V3OUT	3.3V	Maximum current to be drawn: 250mA
VCC1V8OUT	1.8V	Maximum current to be drawn: 250mA
EVDD	1.8V/3.3V	Maximum current to be drawn: 250mA

Table 4-19 Power from module to carrier

4.20.3 Battery Backup

Optionally, the module's RTC can be supplied with a backup voltage:

Signal	I/O Range	Signal conditioning
VBAT	1.8V-5.0V	**Attention:** battery should be protected by diode between battery and connector against charging. Powercap should be protected by serial resistor. Powercap voltage range >3.3V

Table 4-20 Backup supply

4.20.4 SerDes

The MPX-LX2160A module offers 24 SerDes lanes. These lanes can be configured according to the LX2160A reference manual provided by NXP Semiconductor.

SerDes mapping is configurable via RCW.
For more information on possible configurations, please contact MicroSys.

The following tables show the SerDes mapping:

SerDes 1:

	Front Side Left SERDES1 (x8)							
	0	1	2	3	4	5	6	7
	H	G	F	E	D	C	B	A
1	PCIe.1 x4				PCIe.2 x4			
2	SGMII.3	SGMII.4	SGMII.5	SGMII.6	PCIe.2 x4			
3	USXGMII / XFI.3	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	PCIe.2 x4			
4	SGMII.3	SGMII.4	SGMII.5	SGMII.6	SGMII.7	SGMII.8	SGMII.9	SGMII.10
5	PCIe.1 x4				USXGMII / XFI.7	USXGMII / XFI.8	USXGMII / XFI.9	USXGMII / XFI.10
6	USXGMII / XFI.3	USXGMII / XFI.4	SGMII.5	SGMII.6	SGMII.7	SGMII.8	SGMII.9	SGMII.10
7	USXGMII / XFI.3	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	SGMII.7	SGMII.8	SGMII.9	SGMII.10
8	USXGMII / XFI.3	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	USXGMII / XFI.7	USXGMII / XFI.8	USXGMII / XFI.9	USXGMII / XFI.10
9	PCIe.1 x1	SGMII.4	SGMII.5	SGMII.6	PCIe.2 x1	SGMII.8	SGMII.9	SGMII.10
10	PCIe.1 x1 (gen 1,2)	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	PCIe.2 x1 (gen 1,2)	USXGMII / XFI.8	USXGMII / XFI.9	USXGMII / XFI.10
11	PCIe.1 x2		SGMII.5	SGMII.6	PCIe.2 x2		SGMII.9	SGMII.10
12	PCIe.1 x4				PCIe.2 x2		SGMII.9	SGMII.10
13	100GE.1				100GE.2			
14	100GE.1				PCIe.2 x4			
15	50GE.1		50GE.2		PCIe.2 x4			
16	50GE.1		25GE.5	25GE.6	PCIe.2 x4			
17	25GE.3	25GE.4	25GE.5	25GE.6	PCIe.2 x4			
18	USXGMII / XFI.3	USXGMII / XFI.4	25GE.5	25GE.6	USXGMII / XFI.7	USXGMII / XFI.8	USXGMII / XFI.9	USXGMII / XFI.10
19	USXGMII / XFI.3	USXGMII / XFI.4	25GE.5	25GE.6	40GE.2			
20	40GE.1				40GE.2			
21	25GE.3	25GE.4	25GE.5	25GE.6	PCIe.2 x2		25GE.9	25GE.10
22	USXGMII / XFI.3	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	PCIe.2 x2		USXGMII / XFI.9	USXGMII / XFI.10

RCW[SRDS_PRTCL_S1] (decimal)	H Lane 0	G Lane 1	F Lane 2	E Lane 3	D Lane 4	C Lane 5	B Lane 6	A Lane 7	PLL mapping	PLL mapping after gen3/4 speed switch
0	off	off	off	off	off	off	off	off	SSSSSSSS	-
1	PCIe.1 x4				PCIe.2 x4				SSSSSSSS	FFFFFFFF
2	SGMII.3	SGMII.4	SGMII.5	SGMII.6	PCIe.2 x4				SSSSSSSS	SSSSFFFF
3	USXGMII / XFI.3	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	PCIe.2 x4				SSSSFFFF	SSSSFFFF
4	SGMII.3	SGMII.4	SGMII.5	SGMII.6	SGMII.7	SGMII.8	SGMII.9	SGMII.10	SSSSSSSS	N/A
5	PCIe.1 x4				USXGMII / XFI.7	USXGMII / XFI.8	USXGMII / XFI.9	USXGMII / XFI.10	FFFFSSSS	FFFFSSSS
6	USXGMII / XFI.3	USXGMII / XFI.4	SGMII.5	SGMII.6	SGMII.7	SGMII.8	SGMII.9	SGMII.10	SSFFFFFF	N/A
7	USXGMII / XFI.3	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	SGMII.7	SGMII.8	SGMII.9	SGMII.10	SSSSFFFF	N/A
8	USXGMII / XFI.3	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	USXGMII / XFI.7	USXGMII / XFI.8	USXGMII / XFI.9	USXGMII / XFI.10	SSSSSSSS	N/A
9	PCIe.1 x1	SGMII.4	SGMII.5	SGMII.6	PCIe.2 x1	SGMII.8	SGMII.9	SGMII.10	SSSSSSSS	FSSSFSSS
10	PCIe.1 x1 (gen 1,2)	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	PCIe.2 x1 (gen 1,2)	USXGMII / XFI.8	USXGMII / XFI.9	USXGMII / XFI.10	FSSSFSSS	N/A
11	PCIe.1 x2		SGMII.5	SGMII.6	PCIe.2 x2		SGMII.9	SGMII.10	SSSSSSSS	FFSSFFSS
12	PCIe.1 x4				PCIe.2 x2		SGMII.9	SGMII.10	SSSSSSSS	FFFFFFSS
13	100GE.1				100GE.2				FFFFFFFF	N/A
14	100GE.1				PCIe.2 x4				FFFFSSSS	FFFFSSSS
15	50GE.1		50GE.2		PCIe.2 x4				FFFFSSSS	FFFFSSSS
16	50GE.1		25GE.5	25GE.6	PCIe.2 x4				FFFFSSSS	FFFFSSSS
17	25GE.3	25GE.4	25GE.5	25GE.6	PCIe.2 x4				FFFFSSSS	FFFFSSSS
18	USXGMII / XFI.3	USXGMII / XFI.4	25GE.5	25GE.6	USXGMII / XFI.7	USXGMII / XFI.8	USXGMII / XFI.9	USXGMII / XFI.10	SSFFSSSS	N/A
19	USXGMII / XFI.3	USXGMII / XFI.4	25GE.5	25GE.6	40GE.2				SSFFSSSS	N/A
20	40GE.1				40GE.2				SSSSSSSS	N/A
21	25GE.3	25GE.4	25GE.5	25GE.6	PCIe.2 x2		25GE.9	25GE.10	FFFFSSFF	FFFFSSFF
22	USXGMII / XFI.3	USXGMII / XFI.4	USXGMII / XFI.5	USXGMII / XFI.6	PCIe.2 x2		USXGMII / XFI.9	USXGMII / XFI.10	SSSSFFSS	SSSSFFSS

Serdes 2:

	Front Side Right SERDES2 (x8)							
	0	1	2	3	4	5	6	7
	A	B	C	D	E	F	G	H
1	PCIe.3 x2 (gen 1,2)		SATA.1	SATA.2	PCIe.4 x4 (gen 1,2)			
2	PCIe.3 x8							
3	PCIe.3 x4				PCIe.4 x4			
4	PCIe.3 x4 (gen 1,2)				PCIe.4 x2 (gen 1,2)		SATA.1	SATA.2
5	PCIe.3 x4				SATA.3	SATA.4	SATA.1	SATA.2
6	PCIe.3 x4 (gen 1,2)				SGMII.15	SGMII.16	USXGMII / XFI.13	USXGMII / XFI.14
7	PCIe.3 x1 (gen 1,2)	SGMII.12	SGMII.17	SGMII.18	PCIe.4 x1 (gen 1,2)	SGMII.16	USXGMII / XFI.13	USXGMII / XFI.14
8	X	X	SATA.1	SATA.2	SATA.3	SATA.4	USXGMII / XFI.13	USXGMII / XFI.14
9	SGMII.11	SGMII.12	SGMII.17	SGMII.18	SGMII.15	SGMII.16	SGMII.13	SGMII.14
10	SGMII.11	SGMII.12	SGMII.17	SGMII.18	PCIe.4 x4			
11	PCIe.3 x1	SGMII.12	SGMII.17	SGMII.18	PCIe.4 x1	SGMII.16	SGMII.13	SGMII.14
12	SGMII.11	SGMII.12	SGMII.17	SGMII.18	PCIe.4 x2 (gen 1,2)		SATA.1	SATA.2
13	PCIe.3 x4				PCIe.4 x2		SGMII.13	SGMII.14
14	PCIe.3 x2		SGMII.17	SGMII.18	PCIe.4 x2		SGMII.13	SGMII.14

RCW[SRDS_PRTCL_S2] (decimal)	A Lane 0	B Lane 1	C Lane 2	D Lane 3	E Lane 4	F Lane 5	G Lane 6	H Lane 7	PLL mapping	PLL mapping after gen3/4 speed switch
0	off	off	off	off	off	off	off	off	SSSSSSSS	N/A
1	PCIe.3 x2 (gen 1,2)		SATA.1	SATA.2	PCIe.4 x4 (gen 1,2)				SSFFSSSS	N/A
2	PCIe.3 x8								SSSSSSSS	SSSSSSSS
3	PCIe.3 x4				PCIe.4 x4				SSSSSSSS	FFFFFFFF
4	PCIe.3 x4 (gen 1,2)				PCIe.4 x2 (gen 1,2)		SATA.1	SATA.2	SSSSSSFF	N/A
5	PCIe.3 x4				SATA.3	SATA.4	SATA.1	SATA.2	FFFFSSSS	FFFFSSSS
6	PCIe.3 x4 (gen 1,2)				SGMII.15	SGMII.16	USXGMII / XFI.13	USXGMII / XFI.14	FFFFFFSS	N/A
7	PCIe.3 x1 (gen 1,2)	SGMII.12	SGMII.17	SGMII.18	PCIe.4 x1 (gen 1,2)	SGMII.16	USXGMII / XFI.13	USXGMII / XFI.14	FFFFFFSS	N/A
8	X	X	SATA.1	SATA.2	SATA.3	SATA.4	USXGMII / XFI.13	USXGMII / XFI.14	SSFFFFSS	N/A
9	SGMII.11	SGMII.12	SGMII.17	SGMII.18	SGMII.15	SGMII.16	SGMII.13	SGMII.14	SSSSSSSS	N/A
10	SGMII.11	SGMII.12	SGMII.17	SGMII.18	PCIe.4 x4				SSSSSSSS	SSSSFFFF
11	PCIe.3 x1	SGMII.12	SGMII.17	SGMII.18	PCIe.4 x1	SGMII.16	SGMII.13	SGMII.14	SSSSSSSS	FSSSFSSS
12	SGMII.11	SGMII.12	SGMII.17	SGMII.18	PCIe.4 x2 (gen 1,2)		SATA.1	SATA.2	SSSSSSFF	N/A
13	PCIe.3 x4				PCIe.4 x2		SGMII.13	SGMII.14	SSSSSSSS	FFFFFFSS
14	PCIe.3 x2		SGMII.17	SGMII.18	PCIe.4 x2		SGMII.13	SGMII.14	SSSSSSSS	FFSSFFSS

Serdes 3:

RCW[SRDS_PRTCL_S3] (decimal)	A Lane 0	B Lane 1	C Lane 2	D Lane 3	E Lane 4	F Lane 5	G Lane 6	H Lane 7	PLL mapping	PLL mapping after gen3/4 speed switch
0	off	off	off	off	off	off	off	off		N/A
2	PCIe.5 x8								SSSSSSSS	SSSSSSSS
3	PCIe.5 x4				PCIe.6 x4				SSSSSSSS	FFFFFFFF

4.20.5 MAC Capabilities

The Frame Manager of the LX2160A supports eighteen MACs which support different protocols as summarized in the following table from NXP Semiconductor:

MAC	RGMII (1 Gbps)	SGMII (1 Gbps)	XFI (10 Gbps)	10G-SXGMII	25 Gpbs	100/50/40 Gbps	MACSEC Supported
1	-	-	-	-	-	✓	-
2	-	-	-	-	-	✓	-
3	-	✓	✓	✓	✓	-	✓
4	-	✓	✓	✓	✓	-	✓
5	-	✓	✓	✓	✓	-	✓
6	-	✓	✓	✓	✓	-	✓
9	-	✓	✓	✓	-	-	-
10	-	✓	✓	✓	-	-	-
11	-	✓	-	-	-	-	-
12	-	✓	-	-	-	-	-
13	-	✓	✓	✓	-	-	-
14	-	✓	✓	✓	-	-	-
15	-	✓	-	-	-	-	-
16	-	✓	-	-	-	-	-
17	✓ (EC1)	✓	-	-	-	-	-
18	✓ (EC2)	✓	-	-	-	-	-

Table 4-21 MAC capabilities

4.20.6 RGMII

The MPX-LX2160A module provides two RGMII ports.

The following table shows the internal connections of RGMII1:

SoC			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
G1	EC1_RX_CLK	←	ST1-A45		1.8V	
K1	EC1_RX_DV	←	ST1-A42		1.8V	
J2	EC1_RXD0	←	ST1-B41		1.8V	
J1	EC1_RXD1	←	ST1-A43		1.8V	
H1	EC1_RXD2	←	ST1-A44		1.8V	
G2	EC1_RXD3	←	ST1-B43		1.8V	
F3	EC1_GTX_CLK	→	ST1-C45		1.8V	SR: 22R
J3	EC1_TXD0	→	ST1-C42		1.8V	SR: 10R
H3	EC1_TXD1	→	ST1-C43		1.8V	SR: 10R
G4	EC1_TXD2	→	ST1-D45		1.8V	SR: 10R
G3	EC1_TXD3	→	ST1-C44		1.8V	SR: 10R
J4	EC1_TX_EN	→	ST1-D43		1.8V	SR: 10R
R1	EMI1_MDIO	↔	ST1-B45		1.8V	PU: 4,7k
R2	EMI1_MDC	→	ST1-B46		1.8V	PU: 4,7k SR: 10R
P3	EC_GTX_CLK125	←	ST1-G35		1.8V	

Table 4-22 RGMII1: pin assignments

The following table shows the internal connections of RGMII2:

SoC			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
K3	EC2_RX_CLK	←	ST1-A40		1.8V	
P1	EC2_RX_DV	←	ST1-A37		1.8V	
N2	EC2_RXD0	←	ST1-B37		1.8V	

SoC			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
N1	EC2_RXD1	←	ST1-A38		1.8V	
M1	EC2_RXD2	←	ST1-A39		1.8V	
L2	EC2_RXD3	←	ST1-B38		1.8V	
K3	EC2_GTX_CLK	→	ST1-C40		1.8V	SR: 10R
N3	EC2_TXD0	→	ST1-C36		1.8V	SR: 10R
M3	EC2_TXD1	→	ST1-C37		1.8V	SR: 10R
L4	EC2_TXD2	→	ST1-D39		1.8V	SR: 10R
L3	EC2_TXD3	→	ST1-C38		1.8V	SR: 10R
N4	EC2_TXEN	→	ST1-D38		1.8V	SR: 10R
R3	EMI2_MDIO	↔	ST1-F41		1.8V	PU: 2,2k
P4	EMI2_MDC	→	ST1-E45		1.8V	PU: 2,2k SR: 10R

Table 4-23 RGMII2: pin assignments

RGMII signals may be alternatively uses as GPIOs or IEEE1588 signals. Refer to NXP's processor reference manual for further information.

4.20.7 UART

The MPX-LX2160A module provides a maximum of 2 UARTs which can be configured in two ways:

- Two UARTs w/ hardware handshake signals *-or-*
- Four UARTs w/o hardware handshake signals (RX/TX only)

Configuration is done by software via RCW.

The following table shows the internal connections for two UARTs:

SoC			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
B5	UART1_SIN	←	ST1:A50	UART1_SIN	1,8V	
B6	UART1_SOUT	→	ST1:B50	UART1_SOUT	1,8V	
A6	UART1_CTS#	←	ST1:H50	UART3_SIN UART1_CTS#	1,8V	

SoC			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
A5	UART1_RTS#	→	ST1:G50	UART3_SOUT UART1_RTS#	1,8V	
D5	UART2_SIN	←	ST1:D50	UART2_SIN	1,8V	
D6	UART2_SOUT	→	ST1:E50	UART2_SOUT	1,8V	
C6	UART2_CTS#	←	ST1:F50	UART2_CTS#	1,8V	
C5	UART2_RTS#	→	ST1:C50	UART2_RTS#	1,8V	

Table 4-24 UART w/ hardware handshake: pin assignments

UART1 is the serial console of the MPX-LX2160A module but it can be configured for GPIO as well. This setup may require hardware modifications which are not covered by standard module versions. For more information on configuration and ordering please contact MicroSys.

The following tables list the pin sharing options for UART1 and UART2:

SoC pin sharing			Module Connector	
Ball	**Primary function**	**Secondary function**	**Pin**	**Description**
B5	UART1_SIN	GPIO1_10	ST1:A50	configurable as GPIO
B6	UART1_SOUT	GPIO1_11	ST1:B50	configurable as GPIO
A6	UART1_CTS#	GPIO1_08	ST1:H50	configurable as GPIO
A5	UART1_RTS#	GPIO1_09	ST1:G50	configurable as GPIO

Table 4-25 UART1 interface: pin sharing options

SoC pin sharing			Module Connector	
Ball	**Primary function**	**Secondary function**	**Pin**	**Description**
D5	UART2_SIN	GPIO1_06	ST1:D50	configurable as GPIO
D6	UART2_SOUT	GPIO1_07	ST1:E50	configurable as GPIO
C6	UART2_CTS#	GPIO1_04	ST1:F50	configurable as GPIO
C5	UART2_RTS#	GPIO1_05	ST1:C50	configurable as GPIO

Table 4-26 UART2 interface: pin sharing options

4.20.8 I2C

The MPX-LX2160A module offers a maximum of 6 independent I²C busses which run at up to 400kHz. While I2C1 and I2C6 have dedicated pins on the module connector, I2C2 and I2C5 share their pins with SDHC1. Whereas I2C3 and I2C4 share their pins with CAN signals.

I2C3, I2C4 and I2C5 require external pull-ups. For more information on configuration please contact MicroSys.

SoC			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
F5	IIC1_SCL	→	ST1:H45	IIC1_SDA	3,3V	PU: 10k
G5	IIC1_SDA	↔	ST1:H46	IIC1_SCL	3,3V	PU: 10k
E4	IIC2_SDA	↔	ST1:A49	IIC2_SDA	1,8V	PU: 10k
E3	IIC2_SCL	→	ST1:D49	IIC2_SCL	1,8V	PU: 10k
J5	IIC3_SDA	↔	ST1:F1	IIC3_SDA	1,8V	
H5	IIC3_SCL	→	ST1:F2	IIC3_SCL	1,8V	
L5	IIC4_SDA	↔	ST1:F5	IIC4_SDA	1,8V	
K5	IIC4_SCL	→	ST1:F4	IIC4_SCL	1,8V	
D3	IIC5_SDA	↔	ST1:E47	SPI3_SIN	1,8V	
C4	IIC5_SCL	→	ST1:F47	SPI3_SOUT	1,8V	
C27	IIC6_SDA	↔	ST1:H43	IIC6_SDA	1,8V	
D27	IIC6_SCL	→	ST1:H42	IIC6_SCL	1,8V	

Table 4-27 I2C: pin assignments

4.20.9 CAN

CAN signals are alternate functions from IIC3 and IIC4. Depending on RCW, signals may be used as an IICx or a CANx interface.

SoC			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
J5	IIC3_SDA	↔	ST1:F1	CAN1-RX	1,8V	
H5	IIC3_SCL	→	ST1:F2	CAN1-TX	1,8V	
L5	IIC4_SDA	↔	ST1:F5	CAN2-RX	1,8V	
K5	IIC4_SCL	→	ST1:F4	CAN2-TX	1,8V	

Table 4-28 CAN: pin assignments

4.20.10 SDHC-1 (SD)

Signal mapping for the SDHC-1 (SD) interface:

SoC			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
E3	SDHC1_CD#	←	ST1-D49	49	EVDD 1,8V	II2_SCL
D1	SDHC1_CLK	→	ST1-C47	47	EVDD 1,8V	
E1	SDHC1_CMD	→	ST1-B48	48	EVDD 1,8V	
F1	SDHC1_DAT0	↔	ST1-D48	48	EVDD 1,8V	
E2	SDHC1_DAT1	↔	ST1-E48	48	EVDD 1,8V	
C1	SDHC1_DAT2	↔	ST1-F48	48	EVDD 1,8V	
C2	SDHC1_DAT3	↔	ST1-G48	48	EVDD 1,8V	
E4	SDHC1_WP	→	ST1-A49	49	EVDD 1,8V	II2_SDA

Table 4-29 SDHC-1: pin assignments

4.20.11 eSDHC

The MPX-LX2160A has two SDHC interfaces. The SDHC1 module interface supports SD/SDIO cards (1/4-bit) and SDHC2 supports eMMC devices (1/4/8-bit) up to HS400 mode of operation.

The SHDC1 interface (8-bit) and the SPI3 interface share pins, thus 8-bit support and SPI are mutually exclusive.

The following table shows the internal connections:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
P3	SDHC2_CLK	→	ST1-E17	SDHC2_EXT_	OVDD (1,8V)	SR: 0R
P2	SDHC2_CMD	↔	ST1-E16	SDHC2_EXT_CMD	OVDD (1,8V)	PU: 4k7 SR: 0R
P1	SDHC2_DS	↔	ST1-E15	SDHC2_EXT_	OVDD (1,8V)	PD: 47k SR:0R
R2	SDHC2_DAT0	↔	ST1-D18	SDHC2_EXT_	OVDD (1,8V)	
R1	SDHC2_DAT1	↔	ST1-E19	SDHC2_EXT_	OVDD (1,8V)	
T1	SDHC2_DAT2	↔	ST1-D17	SDHC2_EXT_	OVDD (1,8V)	
U1	SDHC2_DAT3	↔	ST1-E20	SDHC2_EXT_	OVDD (1,8V)	
R3	SDHC2_DAT4	↔	ST1-F15	SDHC2_EXT_	OVDD (1,8V)	
T3	SDHC2_DAT5	↔	ST1-G15	SDHC2_EXT_	OVDD (1,8V)	
V1	SDHC2_DAT6	↔	ST1-F16	SDHC2_EXT_	OVDD (1,8V)	
	SDHC2_DAT7	↔	ST1-G16	SDHC2_EXT_	OVDD (1,8V)	

Table 4-30 SDHC2 interface: pin assignments

4.20.12 USB

The MPX-LX2160A has two USB3.0 ports which can be configured as host or device.

All ports support super-speed (5 Gbit/s) high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) operations.

When OTG is enabled, super-speed operation is not supported.

The following table shows the internal connections:

SoC			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
G8	USB1_VBUS	←		USB1-VBUS	USB_HVDD	SR: 30k1
E9	USB1_ID	←		USB1_UID		
F8	USB1_D_P	↔		USB1_UDP_P		
F9	USB1_D_M	↔		USB1_UDM_N		
C8	USB1_RX_P	←		USB1_RX_P		
D8	USB1_RX_M	←		USB1_RX_N		
A9	USB1_TX_P	→		USB1_TX_P		AC-coupling: 100nF
B9	USB1_TX_M	→		USB1_TX_N		AC-coupling: 100nF

Table 4-31 USB port 1: pin assignments

SoC			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
G10	USB2_VBUS	←		USB2_VBUS	USB_HVDD	SR: 30k1
E11	USB2_ID	←		USB2_UID	USB_HVDD	
F10	USB2_D_P	↔		USB2_UDP_P		
F11	USB2_D_M	↔		USB2_UDM_N		
C10	USB2_RX_P	←		USB2_RX_P		
D10	USB2_RX_M	←		USB2_RX_N		
A11	USB2_TX_P	→		USB2_TX_P		AC-coupling: 100nF
B11	USB2_TX_M	→		USB2_TX_N		AC-coupling: 100nF

Table 4-32 USB port 2: pin assignments

Moreover, the module provides control signals. Each port can be individually enabled and has its own overcurrent signal.

SoC			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
A7	USB1_DRVVBUS	→	ST1:A35	USB1_DRVBUS	OVDD	
B7	USB1_PWRFAULT	←	ST1:A34	USB1_PWR_FLT	OVDD	
E7	USB2_DRVVBUS	→	ST1:A32	USB2_DRVBUS	OVDD	
G7	USB2_PWRFAULT	←	ST1:A31	USB2_PWR_FLT	OVDD	

Table 4-33 USB power control signals: pin assignments

USBx_PWRFAULT signals are high-active signals.
A logic high level signals the port is in an overcurrent situation.

The USB power control signals are optional signals and can be configured as GPIOs. The following table lists the possible functions which are mutually exclusive and may entail hardware modifications.

USB is the primary function used on the pins. Any other setup may require hardware modifications which are not covered by standard module versions. For more information on configuration and ordering please contact MicroSys.

SoC pin sharing				Module Connector	
Ball	**Primary function**	**Secondary function**	**Tertiary function**	**Pin**	**Description**
A7	USB1_DRVVBUS	GPIO4_25		ST1-A35	configurable as GPIO
B7	USB1_PWRFAULT	GPIO4_26		ST1-A34	configurable as GPIO
E7	USB2_DRVVBUS	GPIO4_27		ST1-A32	configurable as GPIO
G7	USB2_PWRFAULT	GPIO4_28		ST1-A31	configurable as GPIO

Table 4-34 USB power control signals: pin sharing options

4.20.13 XSPI

The following table shows the internal connections:

SoC			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
C23	VB_XSPI_EMU#	→	ST1-D16		1,8V	
F25	XSPI_A_DATA0	↔	ST1-C13		1,8V	
E24	XSPI_A_DATA1	↔	ST1-C12		1,8V	
E26	XSPI_A_DATA2	↔	ST1-C11		1,8V	
E27	XSPI_A_DATA3	↔	ST1-C10		1,8V	
F27	XSPI_A_DATA4	↔	ST1-C9		1,8V	
D26	XSPI_A_DATA5	↔	ST1-D15		1,8V	
E25	XSPI_A_DATA6	↔	ST1-D14		1,8V	
D24	XSPI_A_DATA7	↔	ST1-D13		1,8V	
E23	XSPI_A_DQS	→	ST1-C16		1,8V	
D22	XSPI_A_SCK	→	ST1-C15		1,8V	

Table 4-35 XSPI interface: pin assignments

This interface offers the ability to connect to an external eMMC on the carrier. If externally used, the on-board eMMC cannot be used at same time.

4.20.14 SPI

The following table shows the internal connections:

SoC			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
A3	SPI3_PCS0	→	ST1-G49		OVDD (1.8V)	SR: 0R
A4	SPI3_PCS1	→	ST1-A48		OVDD (1.8V)	PU: 4k7 SR: 0R
B3	SPI3_PCS2	→	ST1-C49		OVDD (1.8V)	PD: 47k SR:0R
C3	SPI3_PCS3	→	ST1-A47		OVDD (1.8V)	
B2	SPI3_SCK	→	ST1-E49		OVDD (1.8V)	
D3	SPI3_SIN	←	ST1-E47		OVDD (1.8V)	
C4	SPI3_SOUT	→	ST1-F47		OVDD (1.8V)	

Table 4-36 SPI interface: pin assignments

4.20.15 FTM

The following table shows the internal connections:

SoC			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
M7	ASLEEP	↔	ST2-A7		1.8V	PU: 4k7
L6	FTM1_CH1	↔	ST2-A13		1.8V	PU: 4k7
L11	FTM1_CH2	↔	ST2-A12		1.8V	PU: 4k7
L10	FTM1_CH3	↔	ST2-A9		1.8V	PU: 4k7
K9	FTM2_CH1	↔	ST2-A6		1.8V	PU: 4k7
G6	FTM2_CH2	↔	ST2-A11		1.8V	PU: 4k7
M10	FTM2_CH3	↔	ST2-A8		1.8V	PU: 4k7

Table 4-37 FTM interface: pin assignments

4.20.16 JTAG/COP

The MPX-LX2160A module has a JTAG interface that is directly connected to the module connector.

The following table shows the internal connections of the JTAG interface:

SoC			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
G26	TCK	←	ST1-A22	JTDI	1.8V	PU: 4k7
H27	TDI	←	ST1-A17	JTDO	1.8V	
G27	TDO	→	ST1-A19	JTCK	1.8V	
G25	TMS	←	ST1-A20	JTMS	1.8V	
H26	TRST_B	←	ST1-A16	JTRST#	1.8V	

Table 4-38 JTAG interface: pin assignments

4.20.17 Interrupts

The following table shows the interrupt connections:

SoC			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
H9	IRQ00	↔	ST1-A14		1,8V	PU: 4k7
H10	IRQ01	↔	ST1-E12		1,8V	PU: 4k7
H11	IRQ02	↔	ST1-F13		1,8V	PU: 4k7
J7	IRQ03	↔	ST1-B14		1,8V	PU: 4k7
J11	IRQ04	↔	ST1-H13		1,8V	PU: 4k7
J9	IRQ05	↔	ST1-C9		1,8V	PU: 4k7
H6	IRQ06	↔	ST1-B13		1,8V	PU: 4k7
K6	IRQ07	↔	ST1-G13		1,8V	PU: 4k7
H7	IRQ08	↔	ST1-D13		1,8V	PU: 4k7
K7	IRQ09	↔	ST1-E13		1,8V	PU: 4k7

Table 4-39 Interrupt interface: pin assignments

4.20.18 Control / Reset

The following table shows the control connections:

Module Connector			
Pin	**Signal**	**I/O Range**	**Signal conditioning**
ST1: A10	RESIN#	1.8V	CPLD (PU)
ST1: A10	RESET_OUT#	1.8V	CPLD
ST1: D41	RST_PHY#	1.8V	CPLD
ST2-H21	RST-OUT1-B		CPLD
ST2-G21	RST-OUT2-DELAY-B		CPLD

Table 4-40 Reset pins: pin assignments

4.20.19 Alternate function

Please refer to LX2160A reference manual to find your preferred configuration and corresponding settings for alternate pin functions of the LX2160A SoC.

4.20.20 GPIOs

The MPX-LX2160A provides many interfaces that can be configured as GPIOs. For more information on the GPIO capability of each interface please refer to the SoCs reference manual.

Due to dependencies between the interfaces there can be limitations.

For more information and configuration please contact MicroSys.

RGMII, IRQ or FlexTimer module pins can be configured as GPIOs as well.

4.21 Management Engine (ME)

The management engine interfaces are available on request for customer specific modifications.

4.21.1 ME Console

The microcontroller's console is available and may assist initial bring up activities. For better access, it is recommended to add a connector to your carrier to interface to the serial console. **The interface uses RS232 voltage levels**. For more information, please contact MicroSys.

uC pin			Module Connector	ST7 on Module
Pin	**Signal at uC**	**Signal @ connector**	**Pin**	**Pin**
37	UART-TX-SRCV	UART_SOUT_ME	ST1:H7	4
44	UART-RX-SRCV	UART_SIN_ME	ST1:H8	5

Table 4-41 ME-UART interface

4.21.2 ME Programming

Available on request, custom modifications can be implemented. For better access, it is recommended to add a connector to the carrier to interface to the Segger JLink.

uC pin			Module Connector	ST7 on Module
Pin	**Signal at uC**	**Signal @ connector**	**Pin**	**Pin**
33	SWDIO	SWDIO	ST1:B6	2
32	SWCLK	SWCLK	ST1:B7	3

Table 4-42 ME-Debug interface

For programming the ME, the e²studio for the Renesas S128 Chip is needed, plus a Segger JLink for loading and debugging.

4.21.3 ME I2C

Available on request, custom modifications can be implemented.

4.21.4 ME SPI

Available on request, custom modifications can be implemented.

4.21.5 ME USB

Available on request, custom modifications can be implemented.

4.21.6 ME Power Control

Available on request, custom modifications can be implemented.

4.22 CPLD Interfaces

Available on request, custom modifications can be implemented.

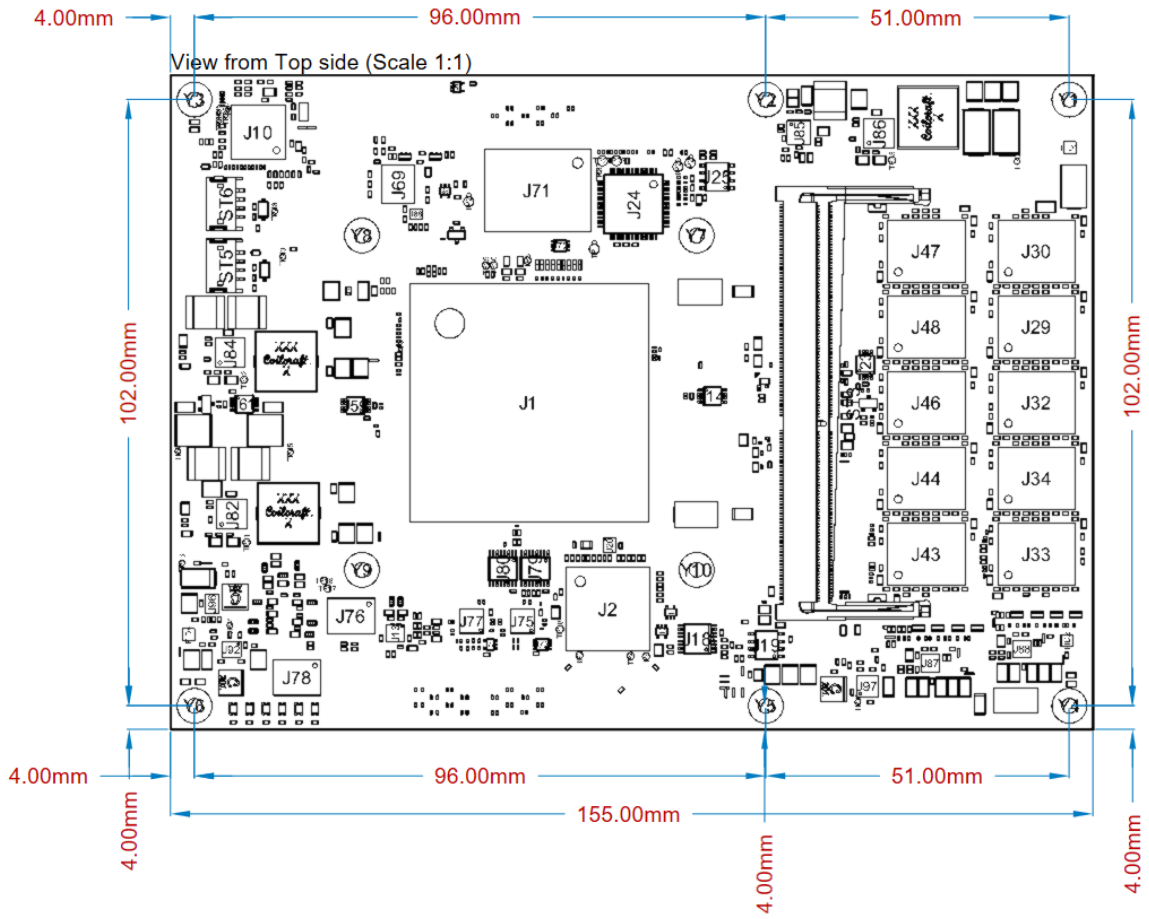
4.23 Fan

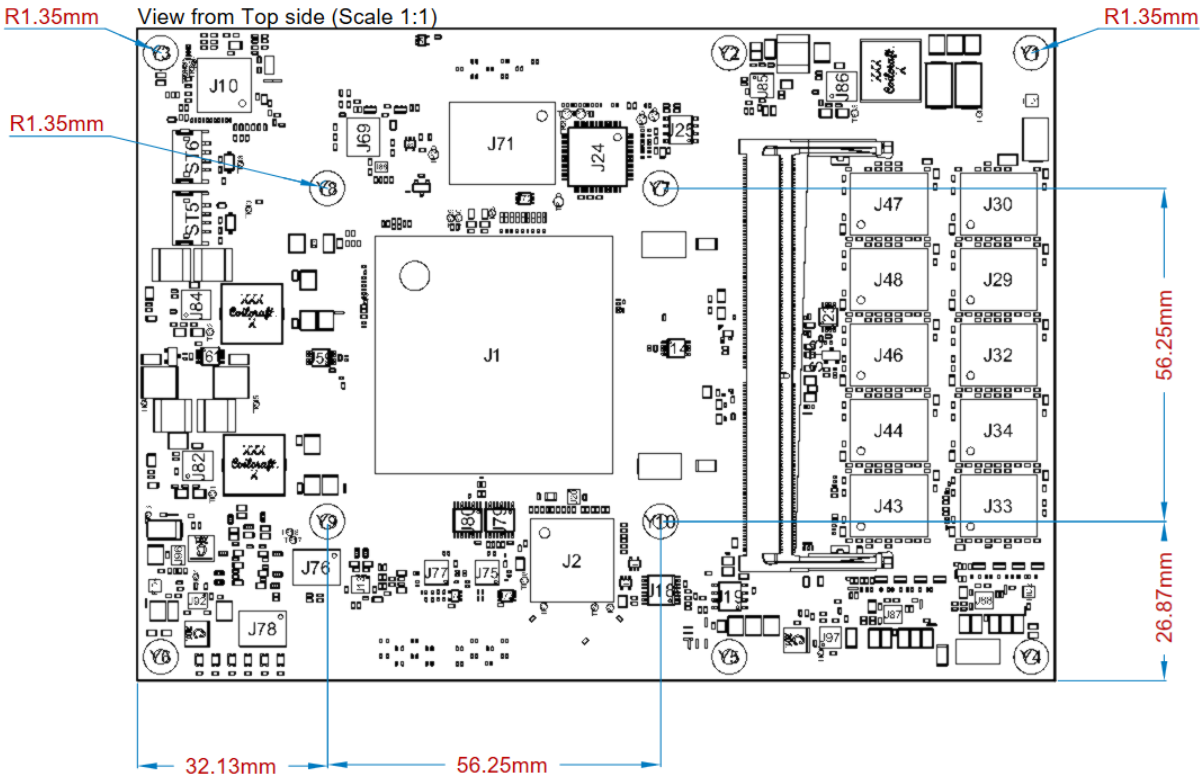
The fans are controlled by the management controller depending on the board temperature. There are 2 independent channels on the module, each controlled by a MAX31790 fan controller. Fans may be connected to ST5 and ST6 (one each).

5 Mechanical Description

5.1 Board Outline

The following drawing shows the mechanical outline of the MPX-LX2160A module.





NOTE

Drawings are not to scale.

NOTE

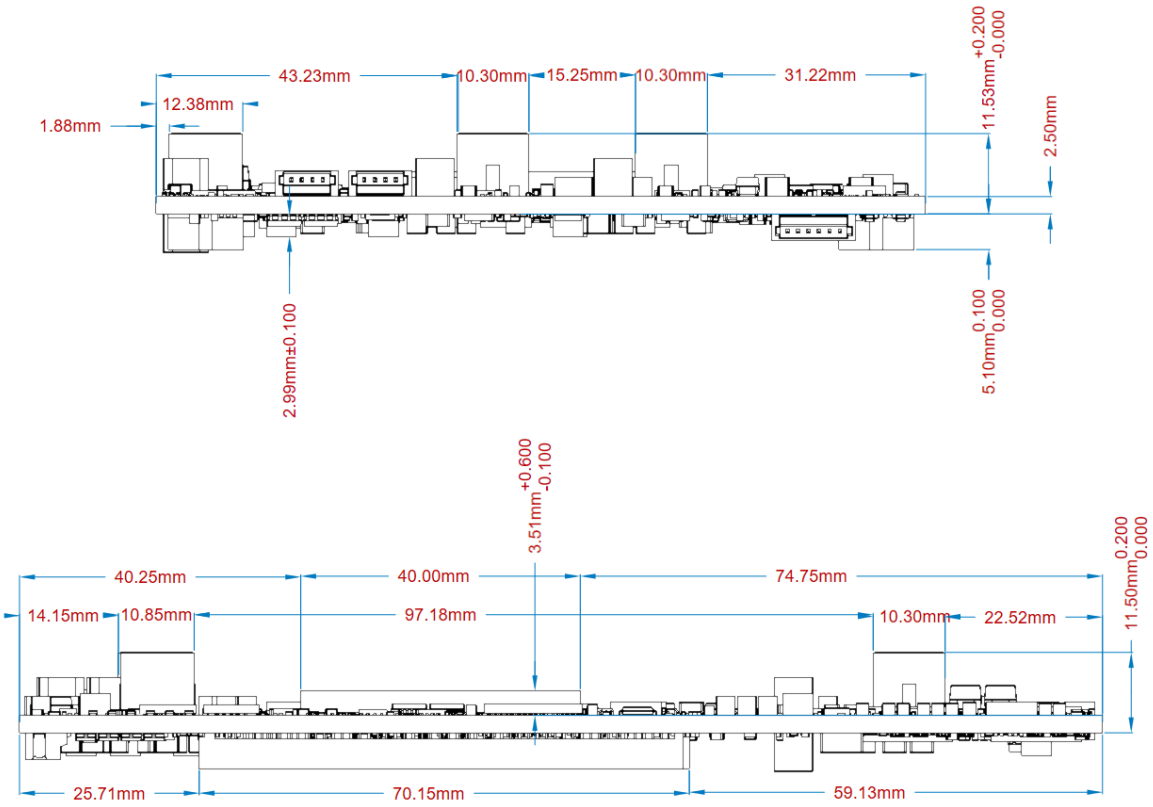
For 3D data files please contact MicroSys.

NOTE

If not stated otherwise, tolerances and acceptance criteria as per IPC-A-600 (current revision at manufacturing date) apply.

5.2 Height

Depending on the connector used, the constructional height for parts on the carrier board placed beneath the module may vary. A 3D Model of the SoM is available on request for mechanical integration.



NOTE

If not stated otherwise, tolerances and acceptance criteria as per IPC-A-600 (current revision at manufacturing date) apply.

5.3 PCB Thickness

Nominal PCB thickness of the MPX-LX2160A module is 2.5mm.

NOTE

If not stated otherwise, tolerances and acceptance criteria as per IPC-A-600 (current revision at manufacturing date) apply.

5.4 Carrier Connector Placement and Mounting~~/Unmounting~~

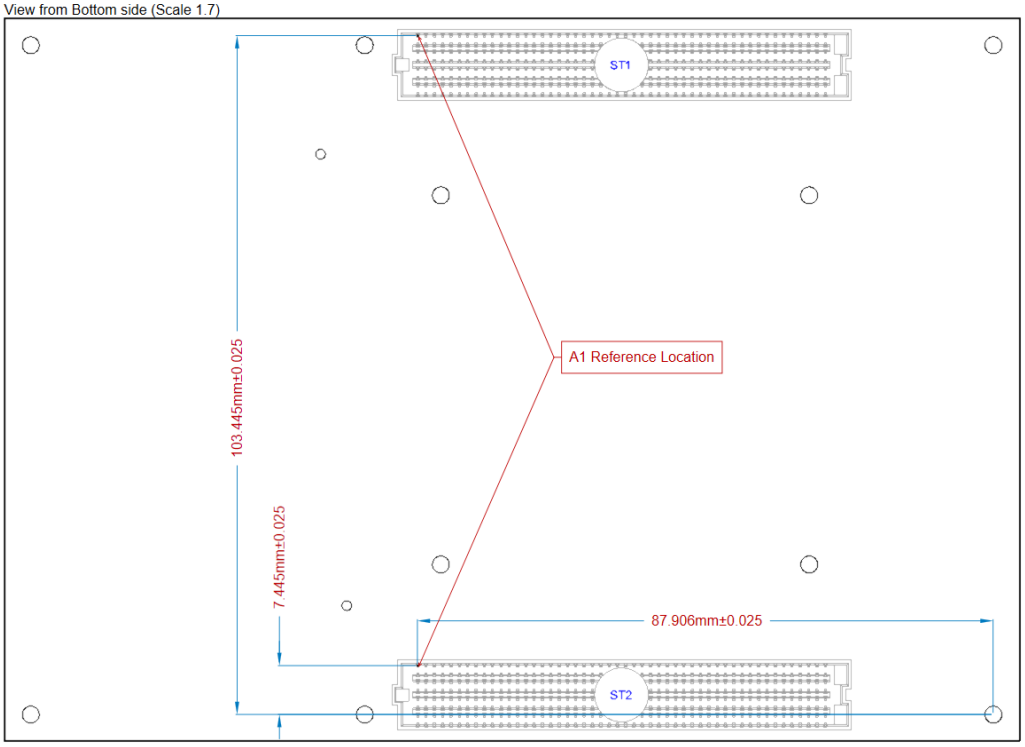
~~tbd~~

Please refer to the official connector product specification from Samtec for final mated tolerances and allowable mated angles for both connectors. Based on the manufacturers reference point of A1 Row A, the total, cumulated placement tolerance on the MPX-LX2160 is +-0.05mm in both x and y direction (see following figure).

Please ensure that the maximum allowed mated displacement tolerances are met according to the connector's product specification, by taking the module placement tolerances into account when designing your carrier solution. Further information can be obtained under NDA from Samtec for general advice on multi-connector assemblies and tolerances.

For additional information or design-in advice, please contact MicroSys Electronics GmbH.

View from Bottom side (Scale 1.7)



6 Software

6.1 U-Boot

The MPX-LX2160A uses ATF/U-Boot as the standard bootloader. A U-Boot image is always flashed in the board's XSPI Flash and/or eMMC memories on delivery.

6.2 Operating System

MicroSys Electronics GmbH offers Linux support for the module.

Other Operating Systems are available on request only.

6.3 Flash Layout

Binary Type	Start Address
bl2_flexspi_nor.pbl	0x0
1D & 2D Training Daten	0xe0000
fip.bin	0x100000
fip_ddr_all.bin	0x800000
mc.itb	0xa00000
dpl-eth.19.dtb	0xd00000
dpc-usxgmii.crx08.dtb	0xe00000

Table 6-1: Flash layout

7 Safety Requirements and Protective Regulations

7.1 EMC

The System on Module MPX-LX2160A is designed according to general requirements of electromagnetic compatibility. Nevertheless, there are several factors which in the target system may require measures against interference.

Active components, especially SoCs of the latest generation not only operate with high frequencies but also drive very fast signal rise times.

At least the following measures shall be applied:

- Provide sufficient block capacitors in your supply voltage rails
- Keep all clock lines short in order to prevent interference with other signals
- Shield clock lines with ground planes or keep as much distance as possible to other signals
- Provide filtering for all external signals
- Provide an EMI proof housing for your electronics

7.2 ESD

For technical reasons there is no ESD protection on the MPX-LX2160A. Please provide sufficient protection on the baseboard and/or at system level.

7.3 Reliability

The SoM is available for operation in extended temperature range.

Please note that steady high temperature operation reduces lifetime of all electronic components. Make sure that no component on the module ever exceeds its maximum specified temperature during operation or storage. A reasonable cooling concept can dramatically increase the lifetime of your electronics.

The MPX-LX2160A is designed to withstand a high level of shock and vibration since the weight of the SoM is relatively low and there are no overhanging components on the SoM. If desired, MicroSys Electronics GmbH can support you with your shock and vibration concept. Please ask your sales representative or send an email inquiry to support@microsys.de.

Relevant components on the module are chosen with values for a high level of derating.

7.4 Climatic Conditions

The relative humidity during operation or storage of the module may not exceed 10% to 90%, non-condensing.

7.5 RoHS

All components on the MPX-LX2160A are RoHS compliant, also an RoHS compliant soldering process is used for manufacturing.

8 General notes

Customers responsibility for chip errata:

It is the user's responsibility to make sure all application relevant errata published by the manufacturer of each component are taken note of.

The manufacturer’s advice should be followed.

If desired, MicroSys Electronics GmbH can support you with your lifecycle management regarding chip errata. Please ask your sales representative or send an email inquiry to support@microsys.de.

9 History

Date	Version	Change Description
2021-02-12	1.0	Initial Version
2021-02-18	1.1	ST1 H45 = IIC1_3V3_SDA, ST1-H46 = IIC1_3V3_SCL
2021-03-18	1.2	Correct PCB tolerance definitions
2021-06-09	1.3	Update PCB Drawings, Correct Document Markups
2021-10-07	1.4	Add warning for module handling

Table 9-1 Document history

10 Appendix

10.1 Acronyms

These acronyms are being used within the document; note that this list does not claim to be complete or exhaustive:

CPU ..... *Central Processing Unit*
ESD ..... *Electrostatic Discharge*
eSDHC ..... *Enhanced Secured Digital Host Controller*
GPL ..... *General Public License*
I²C ..... *Inter-Integrated Circuit*
LED ..... *Light Emitting Diode*
PU ..... *Pull-Up Resistor*
RCW ..... *Reset Configuration Word*
RTC ..... *Real-Time clock*
SDHC ..... *Secure Digital High Capacity*
SOM ..... *System On Module*
SPI ..... *Serial Peripheral Interface*
SR ..... *Series Resistor*
UART ..... *Universal Asynchronous Receiver/Transmitter*

10.2 Table of Figures

10.3 Table of Tables