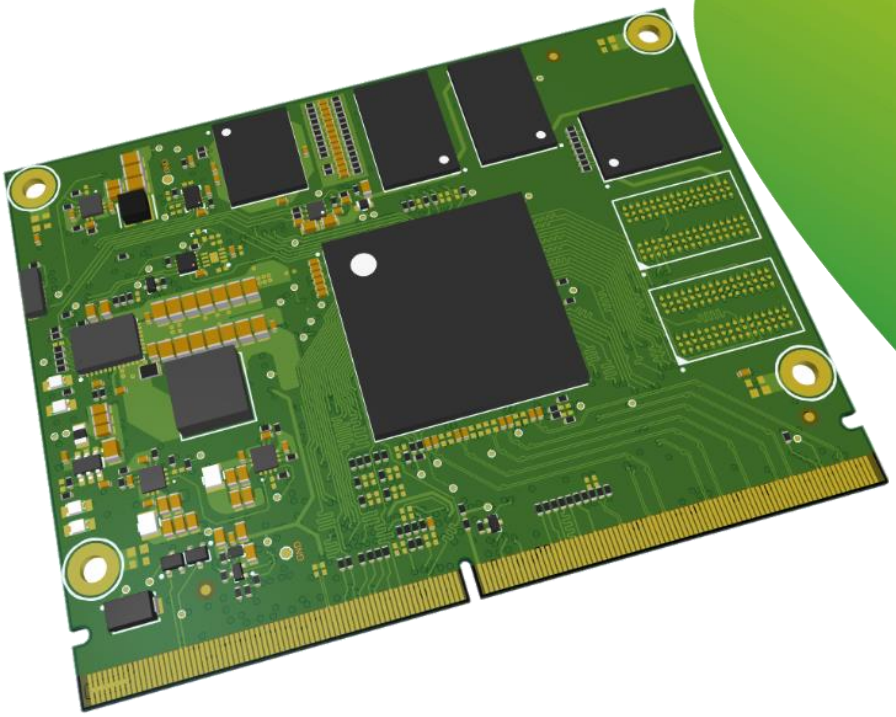

miriac MPX-LS1043A2

User Manual (HW Revision 5)

V 5.3

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1 General Notes

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MicroSys Electronics GmbH
Muehlweg 1
D-82054 Sauerlach
Germany

Phone: +49 8104 801-0

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1.5 Symbols, Conventions and Abbreviations

1.5.1 Symbols

Throughout this document, the following symbols will be used:

	Information marked with this symbol MUST be obeyed to avoid the risk of severe injury, health danger, or major destruction of the unit and its environment
	Information marked with this symbol MUST be obeyed to avoid the risk of possible injury, permanent damage or malfunction of the unit.
	Information marked with this symbol gives important hints upon details of this manual, or in order to get the best use out of the product and its features.

Table 1-1 Symbols

1.5.2 Conventions

Symbol	explanation
#	denotes a low active signal
←	denotes the signal flow in the shown direction
→	denotes the signal flow in the shown direction
↔	denotes the signal flow in both directions
→	denotes the signal flow in the shown direction with additional logic / additional ICs in the signal path
I/O	denotes a bidirectional pin
Input	denotes an input pin
matched	denotes the according signal to be routed impedance controlled and length matched
Output	denotes an output pin
Pin 1	refers to the numeric pin of a component package
Pin a1	refers to the array position of a pin within a component package
XXX-	denotes the negative signal of a differential pair
XXX+	denotes the positive signal of a differential pair
XXX	denotes an optional not mounted or fitted part

Table 1-2 Conventions

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1.6 Safety and Handling Precautions

	**DO NOT exceed the rated maximum values for the power supply! This may result in severe permanent damage to the unit, as well as possible serious injury.** **ALWAYS keep the unit dry, clean and free of foreign objects. Otherwise, irreparable damage may occur.**
	**Parts of the unit may become hot during operation. Take care not to touch any parts of the circuitry during operation to avoid burns, and operate the unit in a well-ventilated location. Provide an appropriate cooling solution as required.**
	**ALWAYS take care of ESD-safe handling!** **Many pins on the module connector are directly connected to the CPU or other ESD sensitive devices.** **Make or break ANY connections ONLY while the unit is switched OFF.** **Otherwise, permanent damage to the unit may occur, which is not covered by warranty.**
	**There is no separate SHIELD connection.** **The module's mounting holes are not connected to GND** **Take this into account when handling and mounting the unit.**

Table 1-3 Safety and Handling Precautions

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2 Short Description

The miriac MPX-LS1043A2 is a member of the MPX module family based on the MicroSys MPX2 specification and NXP's QorIQ® Layerscape LS1043A Multicore Communications Processor.

MicroSys Electronics GmbH offers a Starterkit which provides the key features of the module. The customer can:

- …evaluate the basic concept of the MPX2 standard
- …test the operation of the MPX-LS1043A2 module
- …evaluate the main interfaces of the LS1043A CPU
- …test the provided software
- …start developing

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3 System Description

3.1 Block Diagram

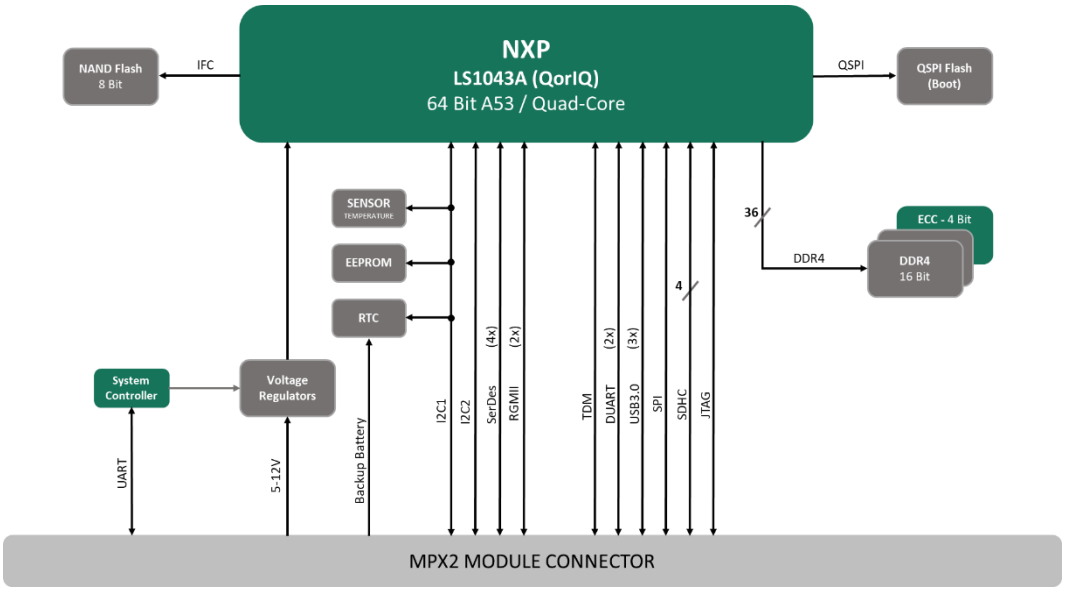

Figure 3-1 Block Diagram

3.2 System Components

- QorIQ Layerscape processor LS1043A or LS1023A
- Microcontroller as monitoring and supervising unit with power management and configuration tasks
- DDR4 SDRAM
- Clock Generators for CPU and interface clocks
- QSPI flash as boot or storage device
- NAND flash as boot or storage device
- I²C EEPROM
- I²C temperature sensor
- I²C RTC
- Voltage regulators for onboard generated voltages

3.3 Power Consumption

The MPX-LS1043A2 can be supplied by a single input power rail ranging from 5V to 12V. The efficiency of the voltage regulators differs in that range. Thus for best overall efficiency choose 5V input voltage if possible. The typical power consumption values for the module are determined on a CRX05 carrierboard running U-boot (idle) at room temperature (4 cores @ 1400MHz / 400MHz CCB clock) with 2GByte of DDR4 memory + ECC (1600 MHz) and passive cooling:

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- 5V input: ~4,5 Watt
- 12V input: ~5,4 Watt

The consumed power is distributed among the following components based on estimated values:

- CPU: ~3-5 Watt
- DDR4 + ECC: ~0,7-0,9 Watt
- QSPI Flash: ~0,05 Watt
- NAND Flash: ~0,05 Watt
- Onboard clock generator: ~0,25 Watt
- Temperature Sensor, RTC, EEPROM: ~0,025 Watt
- Regulator efficiency: ~80-90%

The typical power consumption values for the module over junction temperature are determined on a CRX05 carrier running Linux. Input voltage 12V with 4 times RJ45 1G Ethernet connected as well as console over USB.

Linux Stress: stressapptest (https://github.com/stressapptest/stressapptest) (start parameters: -W -s 60, all cores)

Linux Idle: command prompt

T_j [°C] from internal probe	Power dissipation idle [W]	Power dissipation stress [W]
10	4,8	6,8
30	5,0	7,0
50	5,4	7,3
80	6,2	8,1
105	8,2	10,0

Table 3-1 Typical power consumption running module with Linux

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3.4 Cooling

In chapter 3.3 the power consumption of the MPX-LS1043A2 module was specified. With this information a cooling method needs to be designed in coordination with the final use case. If desired, MicroSys Electronics GmbH can support you with your cooling concept. Please ask your sales representative or send an email inquiry to support@microsys.de.

Commercial temperature grade (0/+70° C) variants:

Component	Temperature (max.)	Description
CPU	105° C	Junction Temperature
DDR	85° C	Case Temperature
Core Regulator	150° C	Junction Temperature

Table 3-2 Commercial grade variants: maximum temperature

Industrial temperature grade (-40/+85° C) variants:

Component	Temperature (max.)	Description
CPU	105° C	Junction Temperature
DDR	95° C	Case Temperature
Core Regulator	150° C	Junction Temperature

Table 3-3 Industrial grade variants: maximum temperature

3.5 Ordering Information

Ordering information can be found on the website http://microsys.de/de/produkte/system-on-modules/qoriqr-armr-architecture/miriactm-mpx-ls1043a/ or contact your local sales representative.

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4 Technical Description

4.1 Pinouts

The following table gives an overview of the 314 pins of the module's edge finger. For a detailed connector description see chapter 5.1. The pins will be described in chapter 4.11 and the following sections.

Hardware Revision 3 added four additional pins named "TK1", "TK2", "BK1" and "BK2".

In Hardware Revision 1 and 2 those pins were "KEY" pins which did not carry any signals.

Please note that the pinout has not been shifted!

The signal direction is from the module's view. For example JTDO (pin B104) is an output from the module and an input to peripheral devices on the carrierboard.

4.1.1 Module Connector – Bottom Pins [ST1]

The following pinout is specific for the MPX-LS1043A2 module and to large parts common for most of the MPX modules.

Nevertheless, different modules do not claim to be pin compatible. Individual modules may have deviating assignments for some functions, whereas power and ground are always assigned to the same pins.

Pin	Signal	I/O	Group	Power Rail
B1	n.c.	O	Quicc Engine	3,3V Level
B2	GND		Power	Ground
B3	TDMB-RXD	I/O	Quicc Engine	3,3V Level
B4	TDMB-TXD	I/O	Quicc Engine	3,3V Level
B5	TDMB-TSYNC	I/O	Quicc Engine	3,3V Level
B6	TDMB-RSYNC	I/O	Quicc Engine	3,3V Level
B7	TDMB-RQ	I/O	Quicc Engine	3,3V Level
B8	GND		Power	Ground
B9	TDMA-RXD	I/O	Quicc Engine	3,3V Level
BK1	n.c.			
BK2	10G-MODE#	I	Management	3,3V Level

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Pin	Signal	I/O	Group	Power Rail
B10	TDMA-TXD	I/O	Quicc Engine	3,3V Level
B11	TDMA-TSYNC	I/O	Quicc Engine	3,3V Level
B12	TDMA-RSYNC	I/O	Quicc Engine	3,3V Level
B13	TDMA-RQ	I/O	Quicc Engine	3,3V Level
B14	GND		Power	Ground
B15	n.c.	O	Quicc Engine	3,3V Level
B16	n.c.	O	Quicc Engine	3,3V Level
B17	GND		Power	Ground
B18	QE-CLK1	O	Quicc Engine	3,3V Level
B19	QE-CLK2	O	Quicc Engine	3,3V Level
B20	GND		Power	Ground
B21	QE-CLK3	O	Quicc Engine	3,3V Level
B22	QE-CLK4	O	Quicc Engine	3,3V Level
B23	GND		Power	Ground
B24	n.c.	I/O	TDM / DMA	3,3V Level
B25	n.c.	I/O	TDM / DMA	3,3V Level
B26	n.c.	I/O	TDM / DMA	3,3V Level
B27	n.c.	I/O	TDM / DMA	3,3V Level
B28	GND		Power	Ground
B29	n.c.	I/O	TDM / DMA	3,3V Level
B30	n.c.	I/O	TDM / DMA	3,3V Level
B31	GND		Power	Ground
B32	UART2-RXD	I	UART2	3,3V Level
B33	UART2-TXD	O	UART2	3,3V Level
B34	UART2-CTS#	I	UART2	3,3V Level
B35	UART2-RTS#	O	UART2	3,3V Level
B36	GND		Power	Ground
B37	UART1-RXD	I	UART	3,3V Level
B38	UART1-TXD	O	UART	3,3V Level
B39	UART1-CTS#	I	UART	3,3V Level
B40	UART1-RTS#	O	UART	3,3V Level

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Pin	Signal	I/O	Group	Power Rail
B41	GND		Power	Ground
B42	n.c.	O	IEEE1588	1,8V Level
B43	n.c.	I	IEEE1588	1,8V Level
B44	n.c.	O	IEEE1588	1,8V Level
B45	n.c.	O	IEEE1588	1,8V Level
B46	n.c.	I	IEEE1588	1,8V Level
B47	n.c.	I	IEEE1588	1,8V Level
B48	n.c.	O	IEEE1588	1,8V Level
B49	n.c.	O	IEEE1588	1,8V Level
B50	GND		Power	Ground
B51	n.c.	O	Display	3,3V Level
B52	n.c.	O	Display	3,3V Level
B53	n.c.	O	Display	3,3V Level
B54	n.c.	O	Display	3,3V Level
B55	GND		Power	Ground
B56	n.c.	O	Display	3,3V Level
B57	n.c.	O	Display	3,3V Level
B58	n.c.	O	Display	3,3V Level
B59	n.c.	O	Display	3,3V Level
B60	n.c.	O	Display	3,3V Level
B61	n.c.	O	Display	3,3V Level
B62	n.c.	O	Display	3,3V Level
B63	n.c.	O	Display	3,3V Level
B64	n.c.	O	Display	3,3V Level
B65	n.c.	O	Display	3,3V Level
B66	n.c.	O	Display	3,3V Level
B67	n.c.	O	Display	3,3V Level
B68	GND		Power	Ground
B69	SPI-CLK	O	SPI	3,3V Level
B70	SPI-CS0#	O	SPI	3,3V Level
B71	SPI-MOSI	O	SPI	3,3V Level

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Pin	Signal	I/O	Group	Power Rail
B72	SPI-MISO	I	SPI	3,3V Level
B73	GND		Power	Ground
B74	I2C2-SDA	I/O	I2C	3,3V Level
B75	I2C2-SCL	O	I2C	3,3V Level
B76	GND		Power	Ground
B77	I2C1-SDA	I/O	I2C	3,3V Level
B78	I2C1-SCL	O	I2C	3,3V Level
B79	GND		Power	Ground
B80	VBAT	Power	Power	3,0V
B81	VREF-SDC	Power	Power	Reference voltage for SD-Card Interface
B82	GND		Power	Ground
B83	MDC2	O	EC Management2	1,2V Level
B84	MDIO2	I/O	EC Management2	1,2V Level
B85	GND		Power	Ground
B86	MDC1	O	EC Management1	VREF-MII
B87	MDIO1	I/O	EC Management1	VREF-MII
B88	GND		Power	Ground
B89	SDC-WP	O	SDHC	3,3V Level
B90	SDC-CD#	I	SDHC	3,3V Level
B91	SDC-D7 / SPI-CS3#	I/O	eMMC / SPI	eMMC: 1,8V SPI: 3,3V
B92	SDC-D6 / SPI-CS2#	I/O	eMMC / SPI	eMMC: 1,8V SPI: 3,3V
B93	SDC-D5 / SPI-CS1#	I/O	eMMC / SPI	eMMC: 1,8V SPI: 3,3V
B94	SDC-D4	I/O	eMMC	1,8V Level
B95	SDC-D3	I/O	eMMC / SDHC	eMMC: 1,8V SDC: 3,3V
B96	SDC-D2	I/O	eMMC / SDHC	eMMC: 1,8V SDC: 3,3V
B97	SDC-D1	I/O	eMMC / SDHC	eMMC: 1,8V SDC: 3,3V
B98	SDC-D0	I/O	eMMC / SDHC	eMMC: 1,8V SDC: 3,3V
B99	SDC-CMD	I/O	eMMC / SDHC	eMMC: 1,8V SDC: 3,3V
B100	SDC-CLK	O	eMMC / SDHC	eMMC: 1,8V SDC: 3,3V
B101	GND		Power	Ground
B102	JTMS	I	JTAG	1,8V Level

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Pin	Signal	I/O	Group	Power Rail
B103	JTDI	I	JTAG	1,8V Level
B104	JTDO	O	JTAG	1,8V Level
B105	JTCK	I	JTAG	1,8V Level
B106	COP-TRST#	O	JTAG / COP	1,8V Level
B107	GND		Power	
B108	n.c.	I	COP	1,8V Level
B109	COP-CKSTPO#	O	COP	1,8V Level
B110	COP-PRST#	O	COP	1,8V Level
B111	MCU-HRST#	O	COP	1,8V Level
B112	GND		Power	Ground
B113	DBG-RXD	I	Debug	1,8V Level
B114	DBG-TXD	O	Debug	1,8V Level
B115	GND		Power	Ground
B116	GPIO1	I/O	GPIO	1,8V Level
B117	GPIO2	I/O	GPIO	1,8V Level
B118	WDOG-TRIG#	I/O	GPIO	1,8V Level
B119	GPIO4	I/O	GPIO	1,8V Level
B120	GPIO5	I/O	GPIO	1,8V Level
B121	GPIO6	I/O	GPIO	1,8V Level
B122	GPIO7	I/O	GPIO	1,8V Level
B123	GPIO8	I/O	GPIO	1,8V Level
B124	GND		Power	Ground
B125	USB2-ID	Analog	USB2.0	1,8V Level
B126	USB2-OC	I	USB2.0	3,3V Level
B127	USB2-EN	O	USB2.0	3,3V Level
B128	USB2-VBUS	I	USB2.0	5V sense
B129	GND		Power	Ground
B130	USB1-ID	Analog	USB2.0	1,8V Level
B131	USB1-OC	I	USB2.0	3,3V Level
B132	USB1-EN	O	USB2.0	3,3V Level
B133	USB1-VBUS	I	USB2.0	5V sense

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Pin	Signal	I/O	Group	Power Rail
B134	GND		Power	Ground
B135	USB3-ID	Analog	USB2.0	1,8V Level
B136	USB3-OC	I	USB2.0	3,3V Level
B137	USB3-EN	O	USB2.0	3,3V Level
B138	USB3-VBUS	I	USB2.0	5V sense
B139	GND		Power	Ground
B140	GND		Power	Ground
B141	GND		Power	Ground
B142	GND		Power	Ground
B143	GND		Power	Ground
B144	GND		Power	Ground
B145	GND		Power	Ground
B146	GND		Power	Ground
B147	GND		Power	Ground
B148	VCC		Power	5V (-5%) up to 12V (+5%)
B149	VCC		Power	5V (-5%) up to 12V (+5%)
B150	VCC		Power	5V (-5%) up to 12V (+5%)
B151	VCC		Power	5V (-5%) up to 12V (+5%)
B152	VCC		Power	5V (-5%) up to 12V (+5%)
B153	VCC		Power	5V (-5%) up to 12V (+5%)
B154	VCC		Power	5V (-5%) up to 12V (+5%)
B155	VCC		Power	5V (-5%) up to 12V (+5%)
B156	VCC		Power	5V (-5%) up to 12V (+5%)

Table 4-1 Module connector: Bottom pins

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4.1.2 Module Connector – Top Pins [ST1]

The following pinout is specific for the MPX-LS1043A2 module and to large parts common for most of the MPX modules.

Nevertheless, different modules do not claim to be pin compatible. Individual modules may have deviating assignments for some functions, whereas power and ground are always assigned to the same pins.

Pin	Signal	I/O	Group	Power Rail
T1	GND		Power	Ground
T2	RX7+	I	Serdes	
T3	RX7-	I	Serdes	
T4	GND		Power	Ground
T5	TX7+	O	Serdes	
T6	TX7-	O	Serdes	
T7	GND		Power	Ground
T8	n.c.	I	Serdes	
T9	n.c.	I	Serdes	
TK1	TBSCAN_EN#	I	JTAG	1,8V Level
TK2	VCC_FUSE		Power	1,8V
T10	GND		Power	Ground
T11	n.c.	O	Serdes	
T12	n.c.	O	Serdes	
T13	GND		Power	Ground
T14	RX5+	I	Serdes	
T15	RX5-	I	Serdes	
T16	GND		Power	Ground
T17	TX5+	O	Serdes	
T18	TX5-	O	Serdes	
T19	GND		Power	Ground
T20	n.c.	I	Serdes	
T21	n.c.	I	Serdes	
T22	GND		Power	Ground
T23	n.c.	O	Serdes	
T24	n.c.	O	Serdes	
T25	GND		Power	Ground
T26	RX3+	I	Serdes	
T27	RX3-	I	Serdes	

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Pin	Signal	I/O	Group	Power Rail
T28	GND		Power	Ground
T29	TX3+	O	Serdes	
T30	TX3-	O	Serdes	
T31	GND		Power	Ground
T32	n.c.	I	Serdes	
T33	n.c.	I	Serdes	
T34	GND		Power	Ground
T35	n.c.	O	Serdes	
T36	n.c.	O	Serdes	
T37	GND		Power	Ground
T38	RX1+	I	Serdes	
T39	RX1-	I	Serdes	
T40	GND		Power	Ground
T41	TX1+	O	Serdes	
T42	TX1-	O	Serdes	
T43	GND		Power	Ground
T44	n.c.	I	Serdes	
T45	n.c.	I	Serdes	
T46	GND		Power	Ground
T47	n.c.	O	Serdes	
T48	n.c.	O	Serdes	
T49	GND		Power	Ground
T50	CLK1+	O	Serdes	
T51	CLK1-	O	Serdes	
T52	GND		Power	Ground
T53	n.c.	O	Serdes	
T54	n.c.	O	Serdes	
T55	GND		Power	Ground
T56	MII2-TXCTL	O	RGMII2	VREF-MII
T57	n.c.	I/O	-	VREF-MII
T58	GND		Power	Ground
T59	MII2-TXD0	O	RGMII2	VREF-MII
T60	MII2-TXD1	O	RGMII2	VREF-MII
T61	GND		Power	Ground
T62	MII2-TXD2	O	RGMII2	VREF-MII
T63	MII2-TXD3	O	RGMII2	VREF-MII

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Pin	Signal	I/O	Group	Power Rail
T64	GND		Power	Ground
T65	MII2-TCLK	O	RGMII2	VREF-MII
T66	MII2-RXCTL	I	RGMII2	VREF-MII
T67	GND		Power	Ground
T68	MII2-RXD0	I	RGMII2	VREF-MII
T69	MII2-RXD1	I	RGMII2	VREF-MII
T70	GND		Power	Ground
T71	MII2-RXD2	I	RGMII2	VREF-MII
T72	MII2-RXD3	I	RGMII2	VREF-MII
T73	GND		Power	Ground
T74	n.c.	I	-	VREF-MII
T75	MII2-RCLK	I	RGMII2	VREF-MII
T76	GND		Power	Ground
T77	MII2-CLK125M	I	RGMII2	VREF-MII
T78	n.c.	O/I	RGMII2	VREF-MII
T79	GND		Power	Ground
T80	VREF-MII		Power	Reference Voltage for MII-Interface
T81	GND		Power	Ground
T82	n.c.	I	RGMII1	VREF-MII
T83	MII-CLK125M	I	RGMII1	VREF-MII
T84	GND		Power	Ground
T85	n.c	I	-	VREF-MII
T86	MII-RCLK	I	RGMII1	VREF-MII
T87	GND		Power	Ground
T88	MII-RXD0	I	RGMII1	VREF-MII
T89	MII-RXD1	I	RGMII1	VREF-MII
T90	GND		Power	Ground
T91	MII-RXD2	I	RGMII1	VREF-MII
T92	MII-RXD3	I	RGMII1	VREF-MII
T93	GND		Power	Ground
T94	MII-TCLK	O	RGMII1	VREF-MII
T95	MII-RXCTL	I	RGMII1	VREF-MII
T96	GND		Power	Ground
T97	MII-TXD0	O	RGMII1	VREF-MII
T98	MII-TXD1	O	RGMII1	VREF-MII
T99	GND		Power	Ground

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Pin	Signal	I/O	Group	Power Rail
T100	MII-TXD2	O	RGMII1	VREF-MII
T101	MII-TXD3	O	RGMII1	VREF-MII
T102	GND		Power	Ground
T103	MII-TXCTL	O	RGMII1	VREF-MII
T104	n.c.	O	-	VREF-MII
T105	GND		Power	Ground
T106	USB3_SSRX+	I	USB3.0	
T107	USB3_SSRX-	I	USB3.0	
T108	GND		Power	Ground
T109	USB3_SSTX+	O	USB3.0	
T110	USB3_SSTX-	O	USB3.0	
T111	GND		Power	Ground
T112	USB2_SSRX+	I	USB3.0	
T113	USB2_SSRX-	I	USB3.0	
T114	GND		Power	Ground
T115	USB2_SSTX+	O	USB3.0	
T116	USB2_SSTX-	O	USB3.0	
T117	GND		Power	Ground
T118	USB1_SSRX+	I	USB3.0	
T119	USB1_SSRX-	I	USB3.0	
T120	GND		Power	Ground
T121	USB1_SSTX+	O	USB3.0	
T122	USB1_SSTX-	O	USB3.0	
T123	GND		Power	Ground
T124	USB3+	I/O	USB2.0 Port3	
T125	USB3-	I/O	USB2.0 Port3	
T126	GND		Power	Ground
T127	USB2_D+	I/O	USB2.0 Port2	
T128	USB2_D-	I/O	USB2.0 Port2	
T129	GND		Power	Ground
T130	USB1_D+	I/O	USB2.0 Port1	
T131	USB1_D-	I/O	USB2.0 Port1	
T132	GND		Power	Ground
T133	BOOT-SEL2	I	Management	1,8V Level
T134	BOOT-SEL1	I	Management	1,8V Level
T135	RST-OUT#	O	Management	Open collector output

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Pin	Signal	I/O	Group	Power Rail
T136	RST-IN#	I	Management	
T137	GND		Power	Ground
T138	GND		Power	Ground
T139	GND		Power	Ground
T140	GND		Power	Ground
T141	GND		Power	Ground
T142	GND		Power	Ground
T143	GND		Power	Ground
T144	GND		Power	Ground
T145	GND		Power	Ground
T146	VCC		Power	5V (-5%) up to 12V (+5%)
T147	VCC		Power	5V (-5%) up to 12V (+5%)
T148	VCC		Power	5V (-5%) up to 12V (+5%)
T149	VCC		Power	5V (-5%) up to 12V (+5%)
T150	VCC		Power	5V (-5%) up to 12V (+5%)
T151	VCC		Power	5V (-5%) up to 12V (+5%)
T152	VCC		Power	5V (-5%) up to 12V (+5%)
T153	VCC		Power	5V (-5%) up to 12V (+5%)
T154	VCC		Power	5V (-5%) up to 12V (+5%)

Table 4-2 Module connector: top pins

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4.1.3 Programming Connector [ST2]

Manufacturer:	JST
Type:	SM06B-XSRS-ETB
Mates with:	06XSR-36S

CPU		ST3			
Ball	**Signal**	**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
		1	1,8V Supply	1,8V	
G13	PROG_SFP	2	VCC_FUSE	1,8V	PD: 330R
		3	t.b.d		For production use only – do not connect
		4	t.b.d		For production use only – do not connect
		5	t.b.d		For production use only – do not connect
		6	GND		

Table 4-3 Programming Connector: Pinout and pin assignments

VCC_FUSE is connected to the CPU pin “G13” and used for supplying the fuse programming voltage. Estimated power consumption is < 180mW.

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4.2 Reset Structure

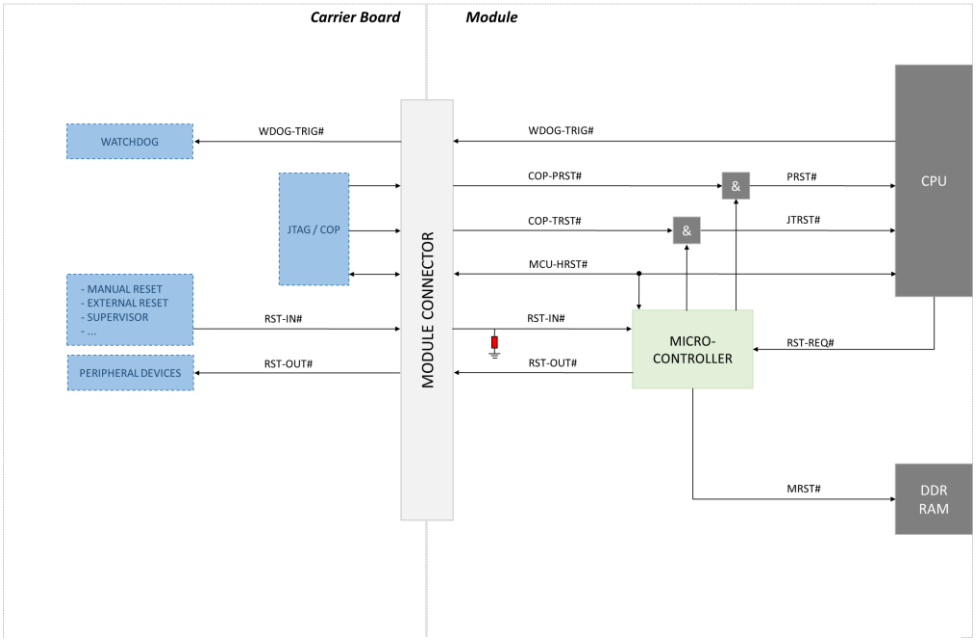

Figure 4-1 Reset Structure

The reset structure of the MPX-LS1043A2 module is shown in Figure 4-1 Reset Structure. For the basic operation only RST-IN# and RST-OUT# are necessary.

The RST-IN# is an input to the module. It signals that the voltage supplies on the carrierboard are within their limits and no manual reset is triggered. When active (signal is low) the microcontroller unit on the module initiates the reset sequence in order to keep the CPU in a defined reset state. No further interaction from the carrierboard is necessary. In case the module reset is active, the module triggers the RST-OUT# signal which is intended to control the reset of peripheral devices on the carrierboard i.e. Ethernet PHYs, PCIe slots and devices.

MCU-HRST#, COP-PRST# and COP-TRST# are for JTAG and debugging purposes only.

NOTE

The default state for RST-IN# is active. Consequently the module is always in a reset state when the RST-IN# signal is not actively driven high by the carrierboard.

RST-OUT# follows HRST# (which is controlled by the CPU), minimum pulse width is 25ms.

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The following table shows the internal connections:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
-	-	←	T136	RST-IN#		Connected to base of PDTC123JT
-	-	→	T135	RST-OUT#		Connected to collector of PDTC123JT
W3	GPIO1_31	←	B118	WDOG-TRIG#	1,8V	PU: 4,7k
F8	HRESET#	↔	B111	MCU-HRST#	1,8V	PU: 1k
F9	PORESET#	←	B110	COP-PRST#	1,8V	PU: 10k
E19	TRST#	→	B106	COP-TRST#	1,8V	PU: 10k

Table 4-4 Reset signals: overview

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4.3 Power Structure

The MPX-LS1043A2 module is supplied by a single supply. For RTC backup buffering an additional supply from the carrierboard is necessary.

The module itself does not provide any supply voltage to the carrier but it has some reference voltages that show the voltage level of the respective interface on the module. In order to preserve flexibility the MPX2 standard does not specify a certain level on those pins. If necessary the carrierboard has to track the reference voltages and generate a copy which can carry higher loads.

The following diagram shows the structure of the power supplies:

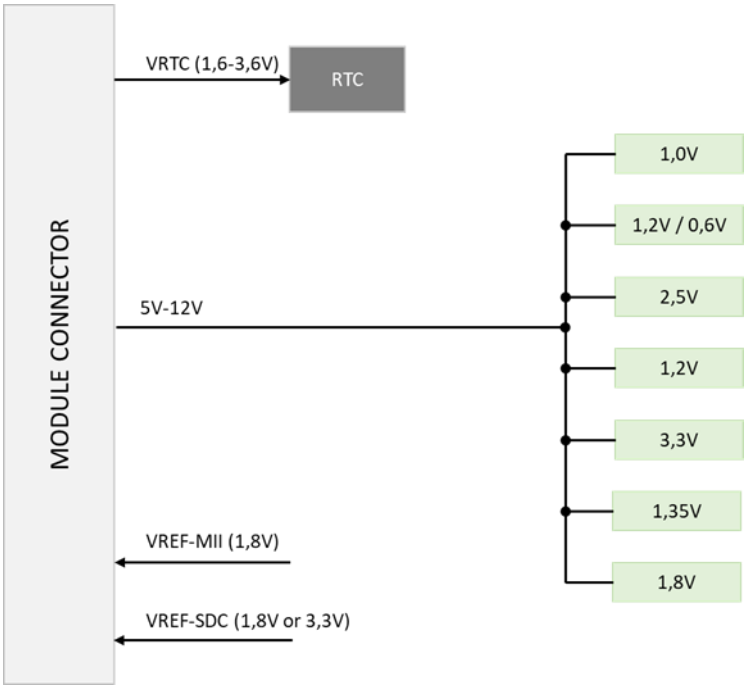

Figure 4-2 Power supplies: structure

The following table shows the internal connections:

Module Connector			
Pin	**Signal**	**I/O Range**	**Signal conditioning**
B80	VRTC	Typ. 1,6V-3,6V	See Figure 4-4
B81	VREF-SDC	1,8V or 3,3V	Maximum current to be drawn: 250mA
T80	VREF-MII	1,8V	Maximum current to be drawn: 250mA
T146-T154 / B148-B156	VIN	5V (-5%) up to 12V (+5%)	TVS diode protection

Table 4-5 Module connector: power pin assignments

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The voltages which are necessary for the CPU and peripheral devices are generated from the input voltage on the module. The voltages are:

Voltage rail	Tolerance	Description
1,0V	1,0V ± 30mV	CPU core voltage
1,2V	1,2V ± 60mV	DDR4 memory voltage
0,6V	0,6V ± 25mV	DDR4 termination voltage
0,6V	0,6V ± 15mV	DDR4 reference voltage
2,5V	2,5V ± 125mV	DDR4 wordline supply voltage
1,2V	1,2V ± 20mV	Ethernet MDC2 interface voltage
1,35V	1,35V ± 67mV	SerDes transmitter voltage
1,8V	1,8V ± 90mV	PLL, GPIO, Ethernet voltage (VREF-MII) & peripheral devices
3,3V	3,3V ± 165mV	USB, GPIO voltage (VREF-SDC) & peripheral devices

Table 4-6 Voltage rails of the module

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4.4 Clock Structure

The MPX-LS1043A2 creates several clocks for different interfaces. For basic operation no external clocks are necessary. There are two exceptions:

- The SerDes clock has to be provided by the carrierboard if the module will be configured as PCIe endpoint

  (supplied via SRD-CLK1 on connector pins T50 & T51)
- RGMII requires an external 125 MHz clock

  (supplied via ECx_GTX_CLK125 on either T83 or T77)

The following table shows the clocks that are available on the MPX-LS1043A2:

CPU			Module Connector				
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**	**Frequency**
P3	SDHC_CLK	→	B100	SDC-CLK	VREF-SDC (1,8V / 3,3V)	PU: 47k SR: 10R	t.b.d.
U2	SPI_CLK	→	B69	SPI-CLK	Level shifted to 3,3V	PU: 10k SR: 10R	t.b.d.
N1	IIC1_SCL	→	B78	I2C1-SCL	3,3V	PU: 2,2k	400 kHz
K3	IIC2_SCL	→	B75	I2C2-SCL	3,3V	PU: 2,2k	400 kHz
E18	TCK	←	B105	JTCK	1,8V	PU: 10k	t.b.d.
W4	EC1_TX_CLK	→	T94	MII1-TXCK	VREF-MII (1,8V)	SR: 10R	125 MHz
W1	EC1_RX_CLK	←	T86	MII1-RXCK	VREF-MII (1,8V)		125 MHz
AC3	EC1_GTX_CLK 125	←	T83	MII1-CRS	VREF-MII (1,8V)		125 MHz
AC4	EC2_GTX_CLK	→	T65	MII2-TXCK	VREF-MII (1,8V)	SR: 10R	125 MHz
AC1	EC2_RX_CLK	←	T75	MII2-RXCK	VREF-MII (1,8V)		125 MHz
AG4	EC2_GTX_CLK 125	←	T77	MII2-GTXCK	VREF-MII (1,8V)		125 MHz

Table 4-7 Clock: pin assignments

IDT6V49205B			Module Connector			
Pin	**Signal**		**Pin**	**Signal**	**Signal conditioning**	**Frequency**
36	PCIeT_LR4	→	T50	SRD-CLK1+	Parallel termination: SR: 33R PD: 49R9	100 MHz / 125 MHz
35	PCIeC_LR4	→	T51	SRD-CLK1-	Parallel termination: SR: 33R PD: 49R9	100 MHz / 125 MHz

Table 4-8 SerDes clock: pin assignments

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4.5 Boot Sources

The MPX-LS1043A2 module offers the option of booting from different boot devices.

The boot source can be selected by means of two pins:

Module Connector			
Pin	**Signal**	**I/O Range**	**Signal conditioning**
T134	BOOT-SEL1	1,8V	PU: 10k
T133	BOOT-SEL2	1,8V	PU: 10k

Table 4-9 Boot select pins: pin assignments

Four different boot devices are possible:

BOOT-SEL1	BOOT-SEL2	Boot Source	Description	Boot Location
HIGH	*HIGH*	QSPI Flash		module
HIGH	*LOW*	reserved	**NOT** any longer supported	module
LOW	*HIGH*	SD/MMC	MMC Bus width: 8 bit SPI-CS0# [PIN-B70] is NOT accessable	carrier board
LOW	*LOW*	SD/MMC	MMC Bus width: 4 bit SPI-CS0# [PIN-B70] is accessable	carrier board

Table 4-10 Boot devices: overview

Booting from NAND is not any longer supported by HW. It was never recommended to do so and latest HW has restrictions, which do not allow to boot from NAND at all. The recommended way of booting is to boot into U-Boot from QSPI flash and load the OS from NAND or to use SD/MMC boot for U-Boot and OS.

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4.6 LEDs

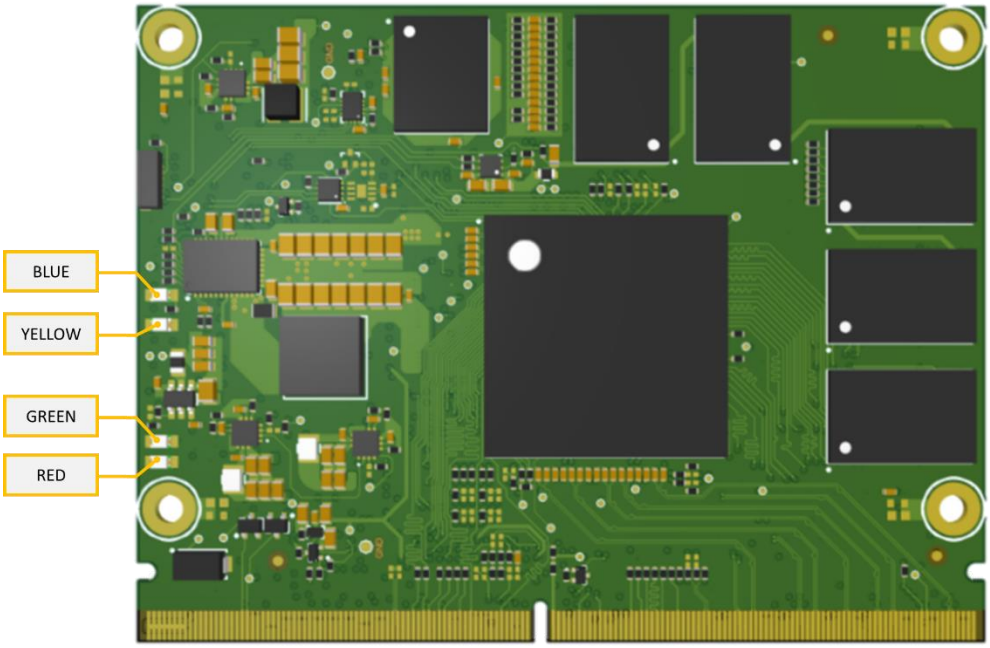

Figure 4-3 LEDs

Colour	Function	
Blue	LED ON:	Onboard clocks configured for 10G (Serdes1- Refclk2 = 156.25MHz)
	LED OFF:	Standard mode (Serdes1- Refclk2 = 100MHz)
Green	LED ON:	Power-up sequence of the module is finished, power is good
	LED BLINKING:	Overvoltage has been detected, the board needs a power cycle
	LED OFF:	Power is not good
Red	LED ON:	Module reset is active
	LED OFF:	Reset is inactive
Yellow	LED ON:	Power Fail
	LED OFF:	No errors detected

Table 4-11 LED: pin description

More information can be found in chapter 4.9.

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4.7 RTC (Real-Time Clock)

The RTC is implemented with an Epson RX-8803LC chip:

- I²C clock frequency up to 400 kHz
- Operating temperature -40°C to 85°C
- Deviation ~13s per month, ~156s per year
- Address see Table 4-22 I2C1: bus map

The RTC needs to be buffered on the carrierboard. The following table shows the internal connection:

Module Connector			
Pin	**Signal**	**I/O Range**	**Signal conditioning**
B80	VRTC	Typ. 1,6V-3.6V	See Figure 4-4

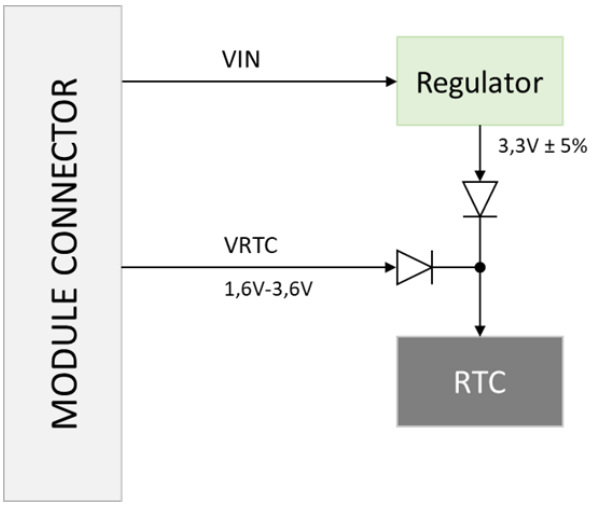

Figure 4-4 RTC: buffering

The RTC provides an interrupt which is connected to the CPU:

CPU			TMP451			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
F11	IRQ00	←	11	INT#	1,8V	PU: 4,7k

Table 4-12 RTC: IRQs

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4.8 Temperature sensor

The LS1043A has an integrated temperature diode which is connected to an TMP451 temperature sensor from Texas Instruments.

- I²C clock frequency up to 400 kHz
- Operating temperature -40°C to 125°C
- Address see Table 4-22 I2C1: bus map
- Local temperature monitoring (TMP451 internal temperature)
- Remote temperature monitoring (LS1043A temperature diode)
- Two CPU interrupts for adjusting two temperature thresholds

	Ambient: 0°C / +70°C	Ambient: -40°C / +125°C
Local Temperature (of the sensor itself)	Max. ± 1°C	Max. ± 2°C
Remote Temperature (of the CPU internal diode)	Max. ± 1°C	Max. ± 4°C

Figure 4-5 Temperature sensor: accuracy

The temperature sensor provides two interrupts which are connected to the CPU:

CPU			TMP451			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
F15	IRQ01	←	6	ALRT#/THRM2	1,8V	PU: 4,7k
H7	IRQ02	←	4	THRM#	1,8V	PU: 4,7k

Table 4-13 Temperature sensor: IRQs

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4.9 Power-up/down behaviour

The module can be normally operated within 5V to 12V.

The input voltage is monitored by the microcontroller which controls the module's power-up and power-down.

Starting from power-off state requires at least 4.75V for the module to start the power-up sequence. During normal state any voltage drop of the input voltage below 4.5V causes the module to power off. In case the voltage recovers and rises above 4.75V again, the module re-starts.

The behaviour is different in case any onboard created voltage is out of specification or the input voltage rises above 13.5V. If that happens, the module is switched off and the orange LED is blinking. A power cycle is required to clear internally generated error flags and to re-start the module.

State	Input voltage	Onboard voltages	RED LED	GREEN LED	ORANGE LED
OFF ↑	< 4.0V ↑	OFF	OFF	OFF	OFF
OFF ↓	< 3.65V ↓				
Undervoltage ↑	4.0V – 4.75V ↑	OFF	ON	OFF	BLINKING
Undervoltage ↓	3.65V – 4.5V ↓				
Running	4.75V – 13.5V	ON / OK	OFF	ON	OFF
Overvoltage[1]	> 13.55V	OFF	OFF	OFF	BLINKING
Power fail	4.75V – 13.5V	FAIL	ON	OFF	OFF
Reset	4.75V – 13.5V	ON / OK	ON	ON	OFF

[1] Requires Powercycle

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4.10 GPIO Expander (2 GByte NAND version only)

For the 2 GByte NAND version an additional GPIO expander FXL6408 is necessary:

- I²C clock frequency up to 400 kHz
- Slave address according to Table 4-22
- One interrupt out signaling pin state changes

For 512Mbyte and 1GByte NAND flash versions the I/O Expander is not populated.

It provides 3 GPIOs and replaces three native CPU GPIOs on the module connector.

It has 8 GPIOs which are used as follows:

GPIO Expander			Module Connector			
Pin	Signal			Pin	Signal	Signal conditioning
12	GPIO0	↔	ST1	B121	GPIO6	
11	GPIO1	↔	ST1	B122	GPIO7	
8	GPIO2	↔	ST1	B123	GPIO8	
7	GPIO3		---	---		
6	GPIO4		---	---		
5	GPIO5		---	---		
4	GPIO6		---	---		
3	GPIO7		---	---		

Table 4-14 GPIO Expander: pin description

CPU			GPIO Expander		
Ball	Signal		Pin	Signal	Signal conditioning
F11	IRQ0	←	1	IOEX_IRQ#	PU: 4k7

Table 4-15 GPIO Expander: IRQ

The IOEX_IRQ# is shared with RTC_IRQ#.

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4.11 Interface Description

4.11.1 GPIOs

The MPX-LS1043A2 provides GPIOs on dedicated pins. Additionally, many interfaces can be configured as GPIOs, too. For more information on the GPIO capability of each interface please refer to the corresponding chapter.

Due to dependencies between the interfaces there can be limitations.

For more information and configuration please contact MicroSys.

The following table shows the dedicated GPIOs and their internal connections:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
D17	GPIO2_14	↔	B116	GPIO1	1,8V	
E17	GPIO2_15	↔	B117	GPIO2	1,8V	
W3	GPIO1_31	↔	B118	GPIO3 / WDOG-TRIG#	1,8V	PU: 4,7k
E9	GPIO1_13	↔	B119	GPIO4	1,8V	PU: 4,7k
F17	GPIO1_14	↔	B120	GPIO5	1,8V	
C20	GPIO2_12	↔	B121	GPIO6[2]	1,8V	
D20	GPIO2_11	↔	B122	GPIO7[2]	1,8V	
A19	GPIO2_10	↔	B123	GPIO8[2]	1,8V	

Table 4-16 GPIOs: pin assignments

MPX2 modules usually provide a QUICC Engine interface that is also available on the LS1043A. However, those pins can be configured as GPIO, IRQ or FlexTimer module pins as well. The primary function on those pins is GPIO. For more information on the QUICC engine and the TDM interface in particular see chapter 4.11.12

The following table presents an overview of pin sharing options:

CPU pin sharing						Module Connector		
Ball	**Primary function**	**Secondary function**	**Tertiary function**	**Quaternary function**		**Pin**	**I/O Range**	**Signal conditioning**
J3	GPIO1_23	IRQ03	FTM3_CH7	TDMB_TSYNC	↔	B5	3,3V	SR: 33R
J4	GPIO1_24	IRQ04	FTM3_CH0	TDMA_RXD	↔	B9	3,3V	SR: 33R

[2] For 2 GByte NAND option GPIOs 6,7,8 are provided by an I2C GPIO Expander

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CPU pin sharing						Module Connector		
J5	GPIO1_25	IRQ05	FTM3_CH1	TDMA_RSYNC	↔	B12	3,3V	SR: 33R
K5	GPIO1_26	IRQ06	FTM3_CH2	TDMA_TXD	↔	B10	3,3V	SR: 33R
L5	GPIO1_27	IRQ07	FTM3_CH3	TDMA_TSYNC	↔	B11	3,3V	SR: 33R
M5	GPIO1_28	IRQ08	FTM3_CH4	TDMB_RXD	↔	B3	3,3V	SR: 33R
N5	GPIO1_29	IRQ09	FTM3_CH5	TDMB_RSYNC	↔	B6	3,3V	SR: 33R
P4	GPIO1_30	IRQ10	FTM3_CH6	TDMB_TXD	↔	B4	3,3V	SR: 33R

Table 4-17 GPIO: pin sharing options

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4.11.2 JTAG/COP

The MPX-LS1043A2 module has a JTAG interface that is directly connected to the module connector.

The following table shows the internal connections of the JTAG interface:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
G17	TDI	←	B103	JTDI	1,8V	
E20	TDO	→	B104	JTDO	1,8V	
E18	TCK	←	B105	JTCK	1,8V	PU: 10k
G18	TMS	←	B102	JTMS	1,8V	
E19	TRST#	←	B106	COP-TRST#	1,8V	PU: 10k

Table 4-18 JTAG interface: pin assignments

Additional COP signals are also available:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
F9	PORESET#	←	B110	COP-TRST#	1,8V	PU: 10k
G15	CKSTP_OUT#	→	B109	CKSTPO#	1,8V	PU: 10k
F8	HRESET#	↔	B111	MCU-HRST#	1,8V	PU: 1k

Table 4-19 COP interface: pin assignments

Hardware Revision 3 introduced a new signal TBSCAN_EN#. It can be temporarily pulled low to enable Boundary Scan.

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
F19	TBSCAN_EN#	←	TK1	TBSCAN-EN#	1,8V	PU: 4k7

Table 4-20 Boundary Scan enable

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4.11.3 I2C

The MPX-LS1043A2 module offers a maximum of four independent I²C busses which run at up 400kHz. While I2C1 and I2C2 have dedicated pins on the module connector, I2C3 and I2C4 share their pins with USB2 & 3 power control signals. More information on the possible options can be found in Table 4-30 USB power control signals: pin sharing options.

I2C3 and I2C4 require hardware modifications which are not covered by standard module versions. For more information on configuration and ordering please contact MicroSys.

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
M1	IIC1_SDA	↔	B77	I2C1_SDA	3,3V	PU: 2,2k
N1	IIC1_SCL	→	B78	I2C1_SCL	3,3V	PU: 2,2k
L3	IIC2_SDA	↔	B74	I2C2_SDA	3,3V	PU: 2,2k
K3	IIC2_SCL	→	B75	I2C2_SCL	3,3V	PU: 2,2k
M4	IIC3_SDA	↔	B22	QE-CLK4	3,3V	PU: 2,2k
L4	IIC3_SCL	→	B21	QE-CLK3	3,3V	PU: 2,2k
N3	IIC4_SDA	↔	B7	TDMB-RQ	3,3V	PU: 2,2k
M3	IIC4_SCL	→	B13	TDMA-RQ	3,3V	PU: 2,2k

Table 4-21 I2C: pin assignments

I2C1 has the following layout:

Device		**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**	**7 bit**
Temperature Sensor	TMP451AIDQF (slave address)	1	0	0	1	1	0	0	1/0	0x4C
	TMP451AIDQF (General Call reset address)	0	0	0	0	0	0	0	-/0	0x00
RTC	RX-8803LC	0	1	1	0	0	1	0	1/0	0x32
GPIO Ex-pander (2 Gbyte NAND Flash option only)	FXL6408	1	0	0	0	0	1	1	1/0	0x43
EEPROM	M24128-BFMC6TG	1	0	1	0	0	0	0	1/0	0x50
Clock Generator	IDT6V49205BNLGI	1	1	0	1	0	0	1	1/0	0x69
System Controller	MK02FN128VLH10	0	0	1	0	0	0	0	1/0	0x10

Table 4-22 I2C1: bus map

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The GPIO Expander is only populated for the 2 GByte NAND Flash option.

There are no devices on the I2C2 bus on the module.

When SD card boot mode is selected I2C-2 is not available (Errata A-008127)

I2C-2 and SD card write protect & card detect share their physical pins on the CPU. During SD card boot those two pins are automatically configured for card detect & write protect

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4.11.4 QSPI

The MPX-LS1043A2 module is equipped with 16MB of QSPI Flash on the LS1043A's QSPI port. Up to 64 MB are available on request/order.

The following table shows the internal connections:

CPU			QSPI Flash MT25QU128ABA8E12		
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**
D8	QSPI_A_CS0	→	C2	CS	1,8V
C9	QSPI_A_SCK	→	B2	CLK	1,8V
			B3	GND	
D11	QSPI_A_DATA0	↔	D3	D0	1,8V
C12	QSPI_A_DATA1	↔	D2	D1	1,8V
D13	QSPI_A_DATA2	↔	C4	D2	1,8V
C13	QSPI_A_DATA3	↔	D4	D3	1,8V
			B4	+1.8V	

Table 4-23 QSPI Flash: pin assignments

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4.11.5 SPI

The MPX-LS1043A2 module provides a SPI interface with a maximum of four chip selects. The signals are level shifted and routed to the module connector.

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
U3	SPI_SIN	←	B72	SPI-MISO	3,3V	Level shifted to 3,3V PU: 100k
V3	SPI_SOUT	→	B71	SPI-MOSI	3,3V	Level shifted to 3,3V
U2	SPI_SCK	→	B69	SPI-CLK	3,3V	Level shifted to 3,3V SR: 10R
U1	SPI_PCS0	→	B70	SPI-CS0#	3,3V	Level shifted to 3,3V PU: 10k
R3	SPI_PCS1	→	B93	SPI-CS1#	3,3V	Level shifted to 3,3V PU: 10k
T3	SPI_PCS2	→	B92	SPI-CS2#	3,3V	Level shifted to 3,3V PU: 10k
V1	SPI_PCS3	→	B91	SPI-CS3#	3,3V	Level shifted to 3,3V PU: 10k

Table 4-24 SPI: pin assignments

The eMMC interface (8 bit) and the SPI interface share pins, thus 8-bit support and SPI are mutually exclusive.

The SPI interface is not the primary interface available on the CPU pins. Furthermore, some of the pins can be configured as GPIOs as well. For more information see Table 4-37 SDHC interface: pin sharing options.

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4.11.6 NAND

The MPX-LS1043A2 module is equipped with 2GB of NAND Flash on the IFC port of the LS1043A by default. Different sizes may be available on request/order. The following table shows the connections and signal levels for the NAND Flash:

CPU			NAND Flash S34MS04G100BHI000		
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**
			G5	LOCK	1,8V
C16	IFC_RB0#	←	C8	RY/BY	1,8V
C18	IFC_OE#	→	D4	RE#	1,8V
C17 ***or*** A19	IFC_CS0# ***or*** IFC_CS1#	→	C6	CE#	1,8V
			D3,G4 ,H8,J6	VCC	1,8V
			C5,F7, K3,K8	GND	
C19	IFC_CLE	→	D5	CLE	1,8V
A18	IFC_AVD	→	C4	ALE	1,8V
C15	IFC_WE0#	→	C7	WE#	1,8V
D19	IFC_WP0#	→	C3	WP#	1,8V
B12	IFC_AD7	↔	H4	D0	1,8V
A11	IFC_AD6	↔	J4	D1	1,8V
B11	IFC_AD5	↔	K4	D2	1,8V
A10	IFC_AD4	↔	K5	D3	1,8V
A9	IFC_AD3	↔	K6	D4	1,8V
B9	IFC_AD2	↔	J7	D5	1,8V
A8	IFC_AD1	↔	K7	D6	1,8V
B8	IFC_AD0	↔	J8	D7	1,8V
			G3	n.c.	
			G8	n.c.	

Table 4-25 NAND Flash: pin assignments

The maximum size can be achieved by populating two flash devices of 1 GByte each. Due to pin multiplexing three native GPIOs are not available (B121, B122, B123) any more. They are replaced by GPIOs from an additional GPIO Expander on address 0x43 (7 bit address). For details see chapter 4.11.3.

GPIO6, GPIO7 and GPIO8 on the module connector are available as I2C controlled GPIOs only for the 2 GByte NAND Flash option (two flash devices populated).

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4.11.7 USB

The MPX-LS1043A2 has a maximum of three USB3.0 ports which can be configured as host or device.

All ports support super-speed (5 Gbit/s), high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) operations.

When OTG is enabled, super-speed operation is not supported.

The following table shows the internal connections:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
E7	USB1_VBUS	←	B133	USB1-VBUS	5V	
F5	USB1_ID	←	B130	USB1-UID	1,8V	
F6	USB1_D_P	↔	T130	USB1-D+		
E6	USB1_D_M	↔	T131	USB1-D-		
E3	USB1_RX_P	←	T118	USB1-SSRX+		
E4	USB1_RX_M	←	T119	USB1-SSRX-		
F1	USB1_TX_P	→	T121	USB1-SSTX+		AC-coupling: 100nF
F2	USB1_TX_M	→	T122	USB1-SSTX-		AC-coupling: 100nF

Table 4-26 USB port 1: pin assignments

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
C7	USB2_VBUS	←	B128	USB2-VBUS	5V	
D5	USB2_ID	←	B125	USB2-UID	1,8V	
D6	USB2_D_P	↔	T127	USB2-D+		
C6	USB2_D_M	↔	T128	USB2-D-		
C3	USB2_RX_P	←	T112	USB2-SSRX+		
C4	USB2_RX_M	←	T113	USB2-SSRX-		
D1	USB2_TX_P	→	T115	USB2-SSTX+		AC-coupling: 100nF
D2	USB2_TX_M	→	T116	USB2-SSTX-		AC-coupling: 100nF

Table 4-27 USB port 2: pin assignments

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CPU			Module Connector			
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
A7	USB3_VBUS	←	B138	USB3-VBUS	5V	
B5	USB_ID	←	B135	USB3-UID	1,8V	
B6	USB3_D_P	↔	T124	USB3-D+		
A6	USB3_D_M	↔	T125	USB3-D-		
A3	USB3_RX_P	←	T118	USB3-SSRX+		
A4	USB3_RX_M	←	T119	USB3-SSRX-		
B1	USB3_TX_P	→	T121	USB3-SSTX+		AC-coupling: 100nF
B2	USB3_TX_M	→	T122	USB3-SSTX-		AC-coupling: 100nF

Table 4-28 USB port 3: pin assignments

Moreover, the module provides control signals. Each port can be individually enabled and has an overcurrent signal on its own.

CPU			Module Connector			
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
H6	USB1_DRVVBUS	→	B132	USB1-EN	3,3V	
G6	USB1_PWRFAULT	←	B131	USB1-OC	3,3V	PD: 100k
L4	USB2_DRVVBUS	→	B127	USB2-EN	3,3V	
M4	USB2_PWRFAULT	←	B126	USB2-OC	3,3V	PD: 100k
M3	USB3_DRVVBUS	→	B137	USB3-EN	3,3V	
N3	USB3_PWRFAULT	←	B136	USB3-OC	3,3V	PD: 100k

Table 4-29 USB power control signals: pin assignments

USBx_PWRFAULT signals are high-active signals.
A logic high level signals the port is in an overcurrent situation.

The USB power control signals are optional signals and share the CPU balls with an additional I²C port. The following table lists the possible functions which are mutually exclusive and may entail hardware modifications.

USB is the primary function used on the pins. Any other setup may require hardware modifications which are not covered by standard module versions. For more information on configuration and ordering please contact MicroSys.

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CPU pin sharing				Module Connector	
Ball	**Primary function**	**Secondary function**	**Tertiary function**	**Pin**	**Description**
H6	USB1_DRVVBUS	GPIO4_29		B132	configurable as GPIO
G6	USB1_PWRFAULT	GPIO4_30		B131	configurable as GPIO
L4	USB2_DRVVBUS	GPIO4_10		B127	configurable as GPIO
			IIC3_SCL	B21	See 4.11.2
M4	USB2_PWRFAULT	GPIO4_11		B126	configurable as GPIO
			IIC3_SDA	B22	See 4.11.2
M3	USB3_DRVVBUS	GPIO4_12		B137	configurable as GPIO
			IIC4_SCL	B13	See 4.11.2
N3	USB3_PWRFAULT	GPIO4_13		B136	configurable as GPIO
			IIC4_SDA	B7	See 4.11.2

Table 4-30 USB power control signals: pin sharing options

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4.11.8 UART

The MPX-LS1043A2 module provides a maximum of four UARTs which can be configured in two ways:

- Two UARTs w/ hardware handshake signals *-or-*
- Four UARTs w/o hardware handshake signals (RX/TX only)

Configuration is done by software via RCW.

The following table shows the internal connections for **two** UARTs:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
H2	UART1_SIN	←	B37	UART1-RXD	3,3V	
H1	UART1_SOUT	→	B38	UART1-TXD	3,3V	
J1	UART1_CTS#	←	B39	UART1-CTS#	3,3V	PU: 4,7k
J2	UART1_RTS#	→	B40	UART1-RTS#	3,3V	PU: 4,7k
K1	UART2_SIN	←	B32	UART2-RXD	3,3V	
L2	UART2_SOUT	→	B33	UART2-TXD	3,3V	
M2	UART2_CTS#	←	B34	UART2-CTS#	3,3V	PU: 4,7k
L1	UART2_RTS#	→	B35	UART2-RTS#	3,3V	PU: 4,7k

Table 4-31 UART w/ hardware handshake: pin assignments

The following table shows the internal connections for **four** UARTs:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
H2	UART1_SIN	←	B37	UART1-RXD	3,3V	
H1	UART1_SOUT	→	B38	UART1-TXD	3,3V	
J1	UART3_SIN	←	B39	UART3-RXD	3,3V	PU: 4,7k
J2	UART3_SOUT	→	B40	UART3-TXD	3,3V	PU: 4,7k
K1	UART2_SIN	←	B32	UART2-RXD	3,3V	
L2	UART2_SOUT	→	B33	UART2-TXD	3,3V	
M2	UART4_SIN	←	B34	UART4-RXD	3,3V	PU: 4,7k
L1	UART4_SOUT	→	B35	UART4-RXD	3,3V	PU: 4,7k

Table 4-32 UART w/o hardware handshake: pin assignments

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UART1 is the serial console of the MPX-LS1043A2 module but can be configured as GPIOs as well.

The following tables list the pin sharing options for UART1 and UART2:

CPU pin sharing			Module Connector	
Ball	**Primary function**	**Secondary function**	**Pin**	**Description**
H2	UART1_SIN	GPIO1_17	B37	configurable as GPIO
H1	UART1_SOUT	GPIO1_15	B38	configurable as GPIO
J1	UART1_CTS#	GPIO1_21	B39	configurable as GPIO
J2	UART1_RTS#	GPIO1_19	B40	configurable as GPIO

Table 4-33 UART1 interface: pin sharing options

CPU pin sharing			Module Connector	
Ball	**Primary function**	**Secondary function**	**Pin**	**Description**
K1	UART2_SIN	GPIO1_18	B32	configurable as GPIO
L2	UART2_SOUT	GPIO1_16	B33	configurable as GPIO
M2	UART2_CTS#	GPIO1_22	B34	configurable as GPIO
L1	UART2_RTS#	GPIO1_20	B35	configurable as GPIO

Table 4-34 UART2 interface: pin sharing options

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4.11.9 eSDHC

The MPX-LS1043A2 module supports SD/SDIO cards (1/4 bit) and eMMC devices (1/4/8 bit). DDR modes are not supported.

NOTE

The eMMC interface (8 bit) and the SPI interface share pins, thus 8-bit support and SPI are mutually exclusive.

There are two possible configuration options:

4.11.9.1 4-bit SDHC & SPI

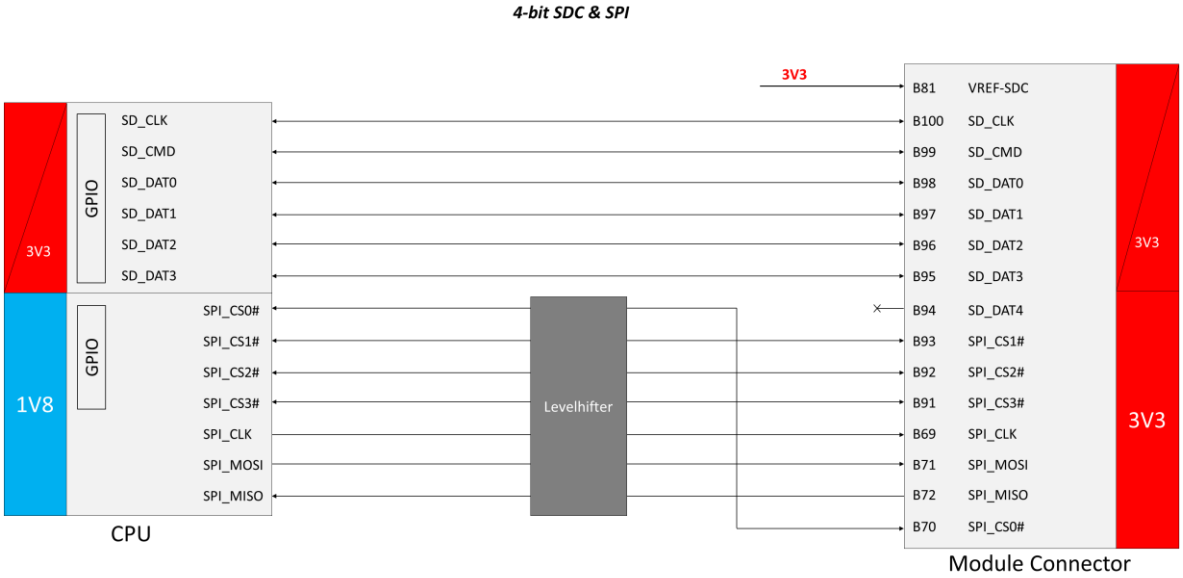

Figure 4-6 4-bit SHDC & SPI configuration

This is the default configuration which provides a SD card and a SPI interface with four chip selects at 3.3V levels. The SPI interface is level shifted. All chip selects have onboard pullups which have been introduced with Hardware Revision 3.

The SD card interface signals can be configured as GPIOs by software via RCW.

The four chip selects cannot be configured as GPIOs during QSPI boot due to a chip errata (A-010539).

In this configuration VREF-SDC is 3.3V.

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The following table shows the internal connections:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
P2	SDHC_CMD	↔	B99	SDC-CMD	VREF-SDC (3,3V)	
P3	SDHC_CLK	→	B100	SDC-CLK	VREF-SDC (3,3V)	SR: 10R
P1	SDHC_DAT0	↔	B98	SDC-D0	VREF-SDC (3,3V)	
R2	SDHC_DAT1	↔	B97	SDC-D1	VREF-SDC (3,3V)	
R1	SDHC_DAT2	↔	B96	SDC-D2	VREF-SDC (3,3V)	
T1	SDHC_DAT3	↔	B95	SDC-D3	VREF-SDC (3,3V)	

Table 4-35 SDHC interface: pin assignments

The MPX-LS1043A2 module additionally provides signals for card detect and write protect. Those signals share the CPU balls with the I²C interface.

I2C2 is the primary function used on the pins. Any other setup may require hardware modifications which are not covered by standard module versions. For more information on configuration and ordering please contact MicroSys.

When SD card boot mode is selected I2C-2 is not available.

I2C-2 and SD card write protect & card detect share their physical pins on the CPU. During SD card boot those two pins are automatically configured for card detect & write protect.

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
K3	SDHC_CD#	←	B90	SDC-CD#	3,3V	PU: 2,2k
L3	SDHC_WP	←	B89	SDC-WP	3,3V	
		→	B81	VREF-SDC	3,3V	Up to 250mA

Table 4-36 SDHC control interface: pin assignments

The “VREF-SDC” voltage may be loaded up to 250mA. In case more current needs to be drawn, the voltage has to be tracked on the carrierboard.

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The following table lists the possible functions:

CPU pin sharing				Module Connector	
Ball	**Primary function**	**Secondary function**	**Tertiary function**	**Pin**	**Description**
P2	SDHC_CMD	GPIO2_04		B99	3,3V GPIO / SDHC
P3	SDHC_CLK	GPIO2_09		B100	3,3V GPIO / SDHC
P1	SDHC_DAT0	GPIO2_05		B98	3,3V GPIO / SDHC
R2	SDHC_DAT1	GPIO2_06		B97	3,3V GPIO / SDHC
R1	SDHC_DAT2	GPIO2_07		B96	3,3V GPIO / SDHC
T1	SDHC_DAT3	GPIO2_08		B95	3,3V GPIO / SDHC
U1	SPI-CS0#	***Erratum A-10539***		B70	3,3V GPIO / SPI
			SDHC_DAT4	B94	1,8V SDHC
R3	SPI-CS1#	***Erratum A-10539***	SDHC_DAT5	B93	3,3V GPIO / SPI 1,8V SDHC
T3	SPI-CS2#	***Erratum A-10539***	SDHC_DAT6	B92	3,3V GPIO / SPI 1,8V SDHC
V1	SPI-CS3#	***Erratum A-10539***	SDHC_DAT7	B91	3,3V GPIO / SPI 1,8V SDHC
K3	IIC2_SCL	GPIO4_02		B75	3,3V GPIO / I2C 1,8V SDHC
			SDHC_CD#	B90	3,3V SDHC card detect
L3	IIC2_SDA	GPIO4_03		B74	3,3V GPIO / I2C 1,8V SDHC
			SDHC_WP	B89	3,3V SDHC write protect

Table 4-37 SDHC interface: pin sharing options

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4.11.9.2 8-bit eMMC

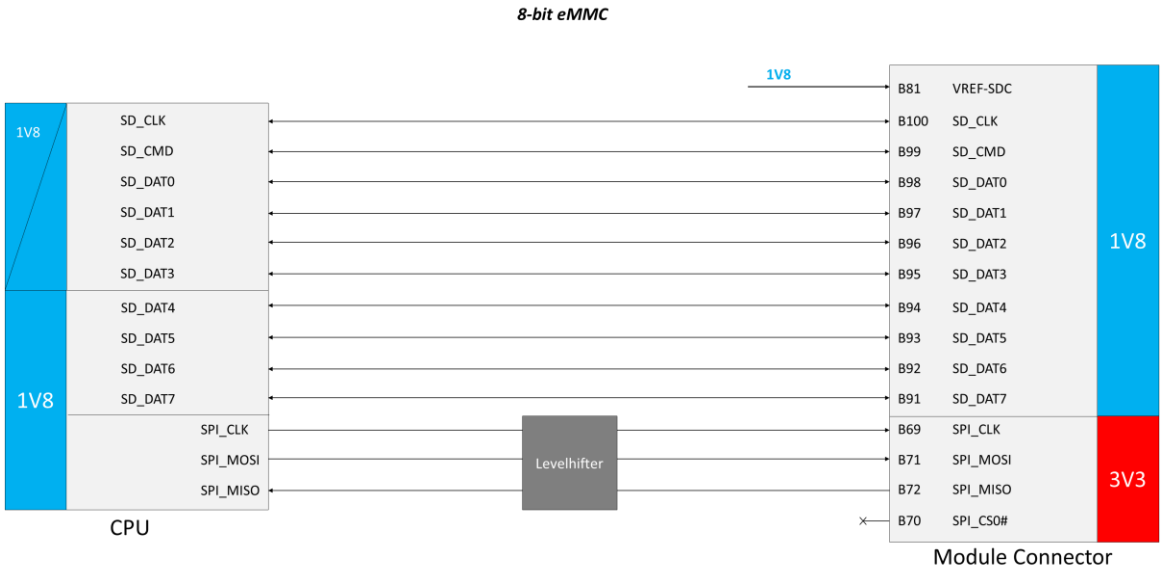

Figure 4-7 8-bit eMMC configuration

NOTE

An errata (A-010539) for the CPU restricts the 8-bit eMMC availability on the MPX module to eMMC boot mode only.

The CPU also provides an 8-bit eMMC configuration. This configuration re-uses the SPI chip select signals for the additional data bits. SPI-CLK, SPI-MOSI and SPI-MISO are not available as well.

In this configuration VREF-SDC is 1.8V.

The following table shows the internal connections:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
P2	SDHC_CMD	↔	B99	SDC-CMD	VREF-SDC (1,8V)	
P3	SDHC_CLK	→	B100	SDC-CLK	VREF-SDC (1,8V)	SR: 10R
P1	SDHC_DAT0	↔	B98	SDC-D0	VREF-SDC (1,8V)	
R2	SDHC_DAT1	↔	B97	SDC-D1	VREF-SDC (1,8V)	
R1	SDHC_DAT2	↔	B96	SDC-D2	VREF-SDC (1,8V)	
T1	SDHC_DAT3	↔	B95	SDC-D3	VREF-SDC (1,8V)	
U1	SDHC_DAT4	↔	B94	SDC-D4	VREF-SDC (1,8V)	
R3	SDHC_DAT5	↔	B93	SDC-D5	VREF-SDC (1,8V)	

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CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
T3	SDHC_DAT6	↔	B92	SDC-D6	VREF-SDC (1,8V)	
V1	SDHC_DAT7	↔	B91	SDC-D7	VREF-SDC (1,8V)	

Table 4-38 eMMC interface: pin assignments

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4.11.10 SerDes

The MPX-LS1043A2 module offers four SerDes lanes. These lanes can be configured according to the LS1043A reference manual provided by manufacturer NXP. More information on the MAC capabilities can be found in chapter 4.11.11.

SerDes mapping is configurable via RCW.
For more information on possible configurations please contact MicroSys.

The following table shows a mapping example in a configuration setup that is used on the SBC-LS1043A2 starterkit:

- SerDes 1: 0x3358

	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7
PCIe	N/A		N/A		N/A	✓	N/A	
SGMII	N/A	✓	N/A	✓	N/A		N/A	
QSGMII	N/A		N/A		N/A		N/A	
SATA	N/A		N/A		N/A		N/A	✓
XFI	N/A		N/A		N/A		N/A	

Table 4-39 SerDes interface: mapping example

The four SerDes lanes can support different protocols. Some of the protocols are available on specific lanes only. The following table shows the distribution across those lanes. Not all combinations are valid:

Lane on module connector:	Lane 0	Lane 1	Lane 2	Lane 3	Lane 4	Lane 5	Lane 6	Lane 7
		MAC9		MAC2		MAC5		MAC6
PCIe x1	N/A	✓	N/A	✓	N/A	✓	N/A	✓
PCIe x2	N/A	✓ (MAC2,9)	N/A	✓ (MAC2,9)	N/A	✓ (MAC5,6)	N/A	✓ (MAC5,6)
PCIe x4	N/A	✓	N/A	✓	N/A	✓	N/A	✓
SGMII (1 Gbps)	N/A	✓	N/A	✓	N/A	✓	N/A	✓
SGMII (2,5 Gbps)	N/A	✓	N/A	✓	N/A		N/A	
QSGMII	N/A	✓	N/A	✓	N/A		N/A	
SATA	N/A		N/A		N/A		N/A	✓
XFI	N/A	✓	N/A		N/A		N/A	

Table 4-40 MAC distribution

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The MPX-LS1043A2 module also provides one clock pair which is displayed in Table 4-8. The frequency on those pins depends on the configuration of the SerDes lanes as different interfaces require clocks at either 100MHz or 125MHz.

The following table shows the internal connections:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
AD6	SD1-TX0	→	T41	SRD-TX1+		AC-coupling: 100nF
AE6	SD1-TX0#	→	T42	SRD-TX1-		AC-coupling: 100nF
AG6	SD1-RX0	←	T38	SRD-RX1+		
AH6	SD1-RX0#	←	T39	SRD-RX1-		
AD10	SD1-TX1	→	T29	SRD-TX3+		AC-coupling: 100nF
AE10	SD1-TX1#	→	T30	SRD-TX3-		AC-coupling: 100nF
AG10	SD1-RX1	←	T26	SRD-RX3+		
AH10	SD1-RX1#	←	T27	SRD-RX3-		
AD16	SD1-TX2	→	T17	SRD-TX5+		AC-coupling: 100nF
AE16	SD1-TX2#	→	T18	SRD-TX5-		AC-coupling: 100nF
AG16	SD1-RX2	←	T14	SRD-RX5+		
AH16	SD1-RX2#	←	T15	SRD-RX5-		
AD19	SD1-TX3	→	T5	SRD-TX7+		AC-coupling: 100nF
AE19	SD1-TX3#	→	T6	SRD-TX7-		AC-coupling: 100nF
AH19	SD1-RX3#	←	T3	SRD-RX7-		
AG19	SD1-RX3	←	T2	SRD-RX7+		

Table 4-41 SerDes interface: pin assignments

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4.11.11 RGMII

The MPX-LS1043A2 module provides two RGMII ports.

The Frame Manager of the LS1043A supports seven MACs which support different protocols as summarized in the following table made available by NXP:

MAC	RGMII (1 Gbps)	SGMII (1 Gbps)	SGMII (2,5 Gbps)	XFI (10 Gbps)
1	-	✓	-	-
2	-	✓	✓	-
3	✓	-	-	-
4	✓	-	-	-
5	-	✓	-	-
6	-	✓	-	-
9	-	✓	✓	✓

Table 4-42 MAC capabilites: RGMII, SGMII, XFI

RGMII 1 and 2 interfaces require at least one external 125MHz clock (1,8V) on either “EC1_GTX_CLK125” (pin AC3) or “EC2_GTX_CLK125” (pin AG4).
The clock source is mandatory for RGMII and can be selected by software via RCW.

The following table shows the internal connections of RGMII1:

CPU			Module Connector			
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
W1	EC1_RX_CLK	←	T86	MII1-RXCK	VREF-MII (1,8V)	
AB1	EC1_RX_CTL	←	T95	MII1-RXCTL	VREF-MII (1,8V)	
AA2	EC1_RXD0	←	T88	MII1-RXD0	VREF-MII (1,8V)	
AA1	EC1_RXD1	←	T89	MII1-RXD1	VREF-MII (1,8V)	
Y1	EC1_RXD2	←	T91	MII1-RXD2	VREF-MII (1,8V)	
W2	EC1_RXD3	←	T92	MII1-RXD3	VREF-MII (1,8V)	
W4	EC1_GTX_CLK	→	T94	MII1-TXCK	VREF-MII (1,8V)	SR: 10R
AB3	EC1_TXD0	→	T97	MII1-TXD0	VREF-MII (1,8V)	SR: 10R
AA3	EC1_TXD1	→	T98	MII1-TXD1	VREF-MII (1,8V)	SR: 10R

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CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
Y4	EC1_TXD2	→	T100	MII1-TXD2	VREF-MII (1,8V)	SR: 10R
Y3	EC1_TXD3	→	T101	MII1-TXD3	VREF-MII (1,8V)	SR: 10R
AB4	EC1_TX_CTL	→	T103	MII1-TXCTL	VREF-MII (1,8V)	SR: 10R
AF2	EMI1_MDIO	↔	B87	MII1-MDIO	VREF-MII (1,8V)	PU: 4,7k
AG2	EMI1_MDC	→	B86	MII1-MDC	VREF-MII (1,8V)	PU: 4,7k SR: 10R
AC3	EC1_GTX_CLK125	←	T83	MII1-CLK125	VREF-MII (1,8V)	

Table 4-43 RGMII1: pin assignments

The following table shows the internal connections of RGMII2:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
AC1	EC2_RX_CLK	←	T75	MII2-RXCK	VREF-MII (1,8V)	
AF1	EC2_RX_CTL	←	T66	MII2-RXCTL	VREF-MII (1,8V)	
AE2	EC2_RXD0	←	T68	MII2-RXD0	VREF-MII (1,8V)	
AE1	EC2_RXD1	←	T69	MII2-RXD1	VREF-MII (1,8V)	
AD1	EC2_RXD2	←	T71	MII2-RXD2	VREF-MII (1,8V)	
AC2	EC2_RXD3	←	T72	MII2-RXD3	VREF-MII (1,8V)	
AC4	EC2_GTX_CLK	→	T65	MII2-TXCK	VREF-MII (1,8V)	SR: 10R
AF3	EC2_TXD0	→	T59	MII2-TXD0	VREF-MII (1,8V)	SR: 10R
AE4	EC2_TXD1	→	T60	MII2-TXD1	VREF-MII (1,8V)	SR: 10R
AE3	EC2_TXD2	→	T62	MII2-TXD2	VREF-MII (1,8V)	SR: 10R
AD3	EC2_TXD3	→	T63	MII2-TXD3	VREF-MII (1,8V)	SR: 10R
AG3	EC2_TX_CTL	→	T56	MII2-TXCTL	VREF-MII (1,8V)	SR: 10R
AH3	EMI2_MDIO	↔	B84	MII2-MDIO	***1,2V***	PU: 2,2k
AH4	EMI2_MDC	→	B83	MII2-MDC	***1,2V***	PU: 2,2k SR: 10R

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CPU			Module Connector			
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
AG4	EC2_GTX_CLK125	←	T77	MII2-CLK125	VREF-MII (1,8V)	

Table 4-44 RGMII2: pin assignments

The RGMII interfaces can also be configured and used as GPIOs:

CPU pin sharing			Module Connector	
Ball	Primary function	Secondary function	Pin	Description
W1	EC1_RX_CLK	GPIO3_13	T86	configurable as GPIO
AB1	EC1_RX_DV	GPIO3_14	T95	configurable as GPIO
AA2	EC1_RXD0	GPIO3_12	T88	configurable as GPIO
AA1	EC1_RXD1	GPIO3_11	T89	configurable as GPIO
Y1	EC1_RXD2	GPIO3_10	T91	configurable as GPIO
W2	EC1_RXD3	GPIO3_09	T92	configurable as GPIO
W4	EC1_GTX_CLK	GPIO3_07	T94	configurable as GPIO
AB3	EC1_TXD0	GPIO3_05	T97	configurable as GPIO
AA3	EC1_TXD1	GPIO3_04	T98	configurable as GPIO
Y4	EC1_TXD2	GPIO3_03	T100	configurable as GPIO
Y3	EC1_TXD3	GPIO3_02	T101	configurable as GPIO
AB4	EC1_TXEN	GPIO3_06	T103	configurable as GPIO
AF2	EMI1_MDIO	GPIO3_01	B87	configurable as GPIO
AG2	EMI1_MDC	GPIO3_00	B86	configurable as GPIO
AC3	EC1_GTX_CLK125	GPIO3_08	T83	configurable as GPIO

Table 4-45 RGMII1: pin sharing options

CPU pin sharing			Module Connector	
Ball	Primary function	Secondary function	Pin	Description
AC1	EC2_RX_CLK	GPIO3_26	T75	configurable as GPIO
AF1	EC2_RX_DV	GPIO3_27	T66	configurable as GPIO
AE2	EC2_RXD0	GPIO3_25	T68	configurable as GPIO
AE1	EC2_RXD1	GPIO3_24	T69	configurable as GPIO
AD1	EC2_RXD2	GPIO3_23	T71	configurable as GPIO
AC2	EC2_RXD3	GPIO3_22	T72	configurable as GPIO

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CPU pin sharing			Module Connector	
AC4	EC2_GTX_CLK	GPIO3_20	T65	configurable as GPIO
AF3	EC2_TXD0	GPIO3_18	T59	configurable as GPIO
AE4	EC2_TXD1	GPIO3_17	T60	configurable as GPIO
AE3	EC2_TXD2	GPIO3_16	T62	configurable as GPIO
AD3	EC2_TXD3	GPIO3_15	T63	configurable as GPIO
AG3	EC2_TXEN	GPIO3_19	T56	configurable as GPIO
AH3	EMI2_MDIO	GPIO4_01	B84	configurable as GPIO
AH4	EMI2_MDC	GPIO4_00	B83	configurable as GPIO
AG4	EC2_GTX_CLK125	GPIO3_21	T77	configurable as GPIO

Table 4-46 RGMII2: pin sharing options

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4.11.12 QUICC Engine

The QUICC Engine block consists of several communication peripheral controllers. It supports various protocols.

The QUICC Engine block of the LS1043A CPU has the following features:

- 32-bit RISC controller
- Serial DMA channel for receive and transmit on all serial channels
- Two TDM interfaces with T1/E1/J1 serial interfaces
- Two UCC controller (HDLC/Transparent)
- Four Baud Rate Generators

The following signals are available on the module connector:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
M5	TDMB_RXD	←	B3	TDMB-RXD	3,3V	SR: 33R
P4	TDMB_TXD	→	B4	TDMB-TXD	3,3V	SR: 33R
J3	TDMB_TSYNC	←	B5	TDMB-TSYNC	3,3V	SR: 33R
N5	TDMB_RSYNC	←	B6	TDMB-RSYNC	3,3V	SR: 33R
N3	TDMB_RQ	→	B7	TDMB-RQ	3,3V	SR: 33R
J4	TDMA_RXD	←	B9	TDMA-RXD	3,3V	SR: 33R
K5	TDMA_TXD	→	B10	TDMA-TXD	3,3V	SR: 33R
L5	TDMA_TSYNC	←	B11	TDMA-TSYNC	3,3V	SR: 33R
J5	TDMA_RSYNC	←	B12	TDMA-RSYNC	3,3V	SR: 33R
M3	TDMA_RQ	→	B13	TDMA-RQ	3,3V	SR: 33R
K3	CLK9	←	B18	QE-CLK1	3,3V	SR: 33R
L3	CLK10	←	B19	QE-CLK2	3,3V	SR: 33R
L4	CLK11	←	B21	QE-CLK3	3,3V	SR: 33R
M4	CLK12	←	B22	QE-CLK4	3,3V	SR: 33R

Table 4-47 Quicc Engine: pin assignments

The Quicc Engine is not the primary interface available on the CPU pins. Furthermore, some of the pins can be configured as GPIOs as well. For pin sharing options see Table 4-17 GPIO: pin sharing options and Table 4-21 I2C: pin assignments

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4.11.13 10G Mode

Some SerDes ports can be configured for XFI with 10.3125Gbps, which is called 10G mode.

10G mode requires 156.25MHz instead of 100MHz on the CPU's PLL input.

Both frequencies are available on the module and can be chosen via pin strapping of pin "BK2" on the module connector. This pin has been introduced with hardware revision 3 to make customer designs easier and more flexible.

For backwards compatibility there's still a resistor jumper on the module. Nevertheless, this requires a special hardware configuration which may come at higher costs.

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5 Mechanical Description

5.1 Edge Finger

The MPX-LS1043A2 module is connected with the carrierboard via a 314 pin connector with 0,5mm pitch. It accepts edge cards with a thickness of 1,2mm.

The pin layout is asymmetric, so the pins are unequally distributed among top and bottom side edge fingers.

Hardware Revision 3 introduced 4 additional pins. This is possible by using a 314 pin connector instead of a 310pin connector as in Hardware Revision 2.

Those four additional signals are in the former key area where the 314pin connector has physical pins instead.

Those four additional pins named “TK1, TK2, BK1, BK2” are inserted between T9/T10 on top side and B9/B10 on bottom side.

The pin numbering has not been shifted!

Figure 5-1 Additional Key Pins

There are 314 pins defined. Be careful, there are more pins on the bottom side than on the top side due to the fact that the pin layout is asymmetric:

Bottom Side	158 pins	Pin labels: “B1”, … „B9“, „BK1“, „BK2“, „B10“ … ”B155”, “B156”
Top Side	156 pins	Pin labels: “T1”, … ”T9”, „TK1“, „TK2“, ”T10”, … “T153”, “T154“

Table 5-1 Connector pin naming scheme

Figure 5-2 Connector orientation

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The module connector is usually used for MXM3 graphic cards commonly found in notebooks. Other than that, MicroSys changed the pin layout so all the physically available 314 pins can be used.

Basically, there are more connectors on the market that can be used as long as there are no conflicts with the mechanical dimensions of the module. The connectors usually have deviating mechanical pads thus drop-in replacements may require a combined PCB footprint. Please check the manufacturers' datasheets for details.

The recommended connectors for the MPX-LS1043A2 are:

Manufacturer	Type	Board-to-board height	Plating	Comment
JAE	MM70-314B1-2-R300	3mm	0,3µm min. gold plating over Ni	314 pins
Foxconn	AS0B826-S55B-7H	2,7mm	10µm gold plating	
Foxconn	AS0B826-S78B-7H	5mm	10µm gold plating	
Aces	91782-3140M-001	5mm	3µm gold plating	
Amphenol	10151114-001TLF	5mm	30µin gold plating	
Yamaichi	CNU113-314-2201-VE	5mm	0,3µin gold plating	

Table 5-2 Connector Types: Ordering Information

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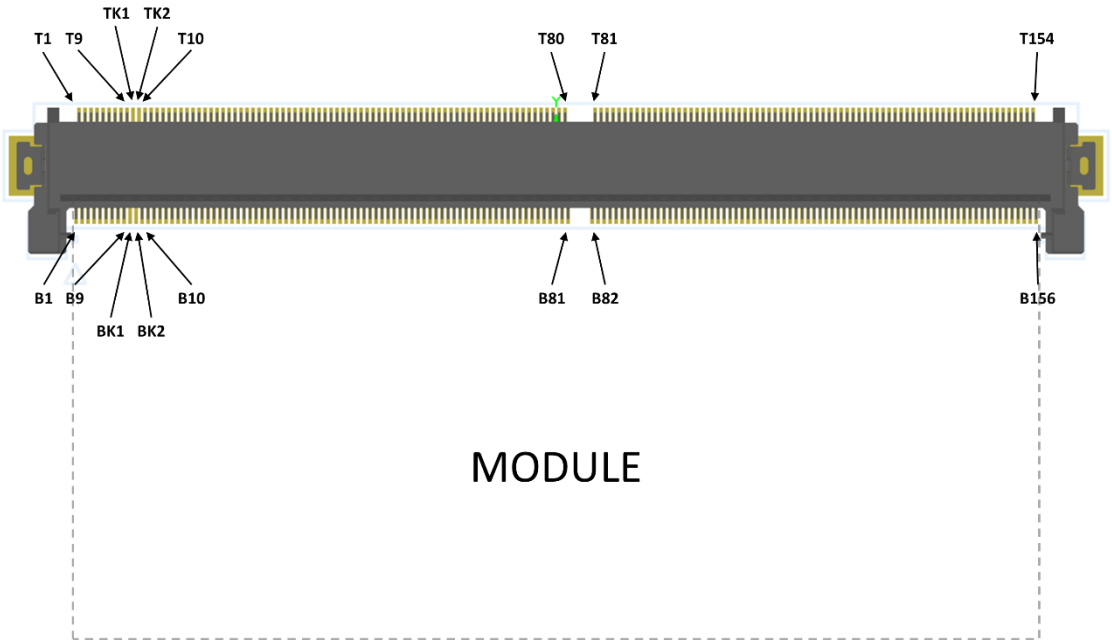

Figure 5-3 Connector pin definition

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5.2 Board Outline

NOTE

For 3D data files please contact MicroSys.

The following drawing shows the mechanical outline (82x62mm) of the MPX-LS1043A2 module plugged in a JAE - MM70-314B1-2-R300 connector. This drawing is not to scale:

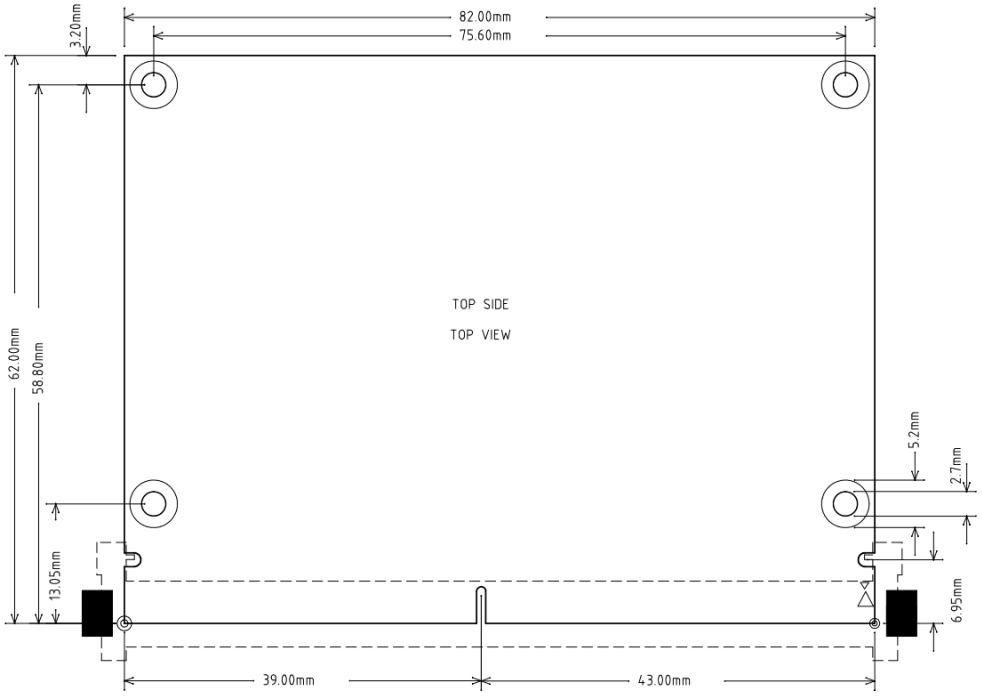

Figure 5-4 Module outline (82x62mm)

The mounting holes can be used with M2.5 screws. Dimensions are designed as follows:

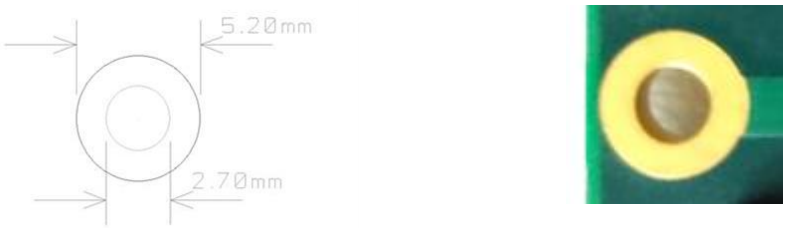

Figure 5-5 Mounting holes: dimensions

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5.3 Height

The MPX2 specification defines a maximum constructional height for bottom side parts of MPX2 CPU modules. The height is limited to 2,0 mm including tolerances.

Depending on the connector used, the constructional height for parts on the carrierboard placed beneath the module may vary. For example, the MM70 connector with 6,7mm product height allows a total board-to-board height of 3,0 mm. This results in a maximum part height on the carrierboard of 1,0 mm.

The MPX-LS1043A2 module conforms with the MPX2 specification.

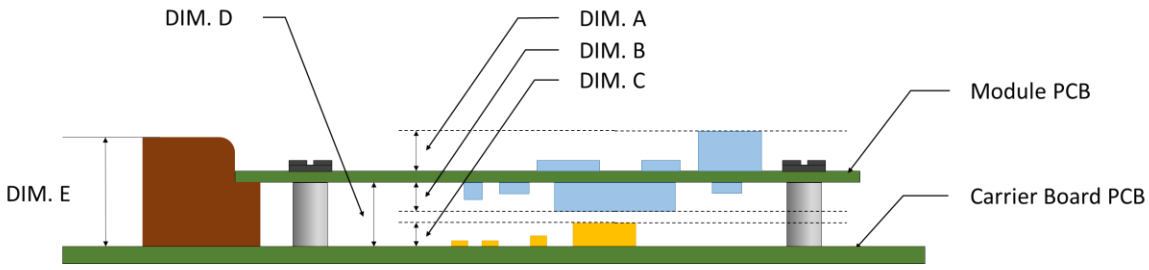

Figure 5-6 Construction height for parts

	Definition	Value	Comment
DIM. A	Module top side parts	3,10 mm	For LS1043A2 modules only
DIM. B	Module bottom side parts	1,60 mm	For LS1043A2 modules only
DIM. C	Carrier board parts under the module	DIM.D minus DIM. B	
DIM. D	Board-to-board height	Depending on connector type	
DIM. E	Connector product height	Depending on connector type	

Table 5-3 Construction height overview

5.4 Thickness

PCB thickness of the MPX-LS1043A2 module is 1,2mm ± 10%.

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5.5 Top Side Component Layout

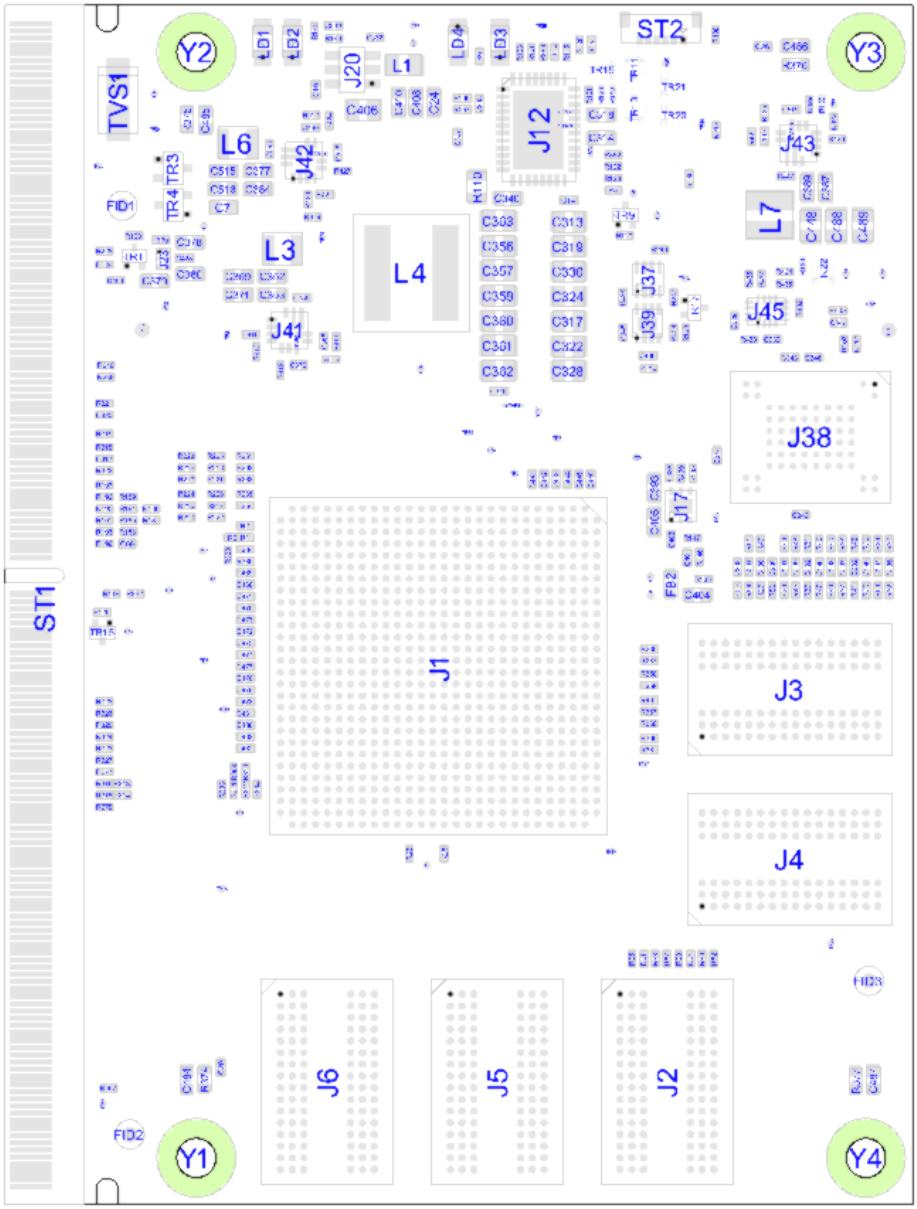

Figure 5-7 Top Components

The following table defines the main components on the top side:

Part Reference	Manufacturer	Type	Function
J1	NXP	LS1043A	CPU
J2/J3/J4	Micron	MT40A512M16	DDR4 memory
J37	Texas Instruments	TMP451	Temperature sensor
J38	SkyHigh	S34MS04G	NAND flash
ST2	JAE	SM06B-XSRS-ETB	Programming connector

Table 5-4 Top side components

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5.6 Bottom Side Component Layout

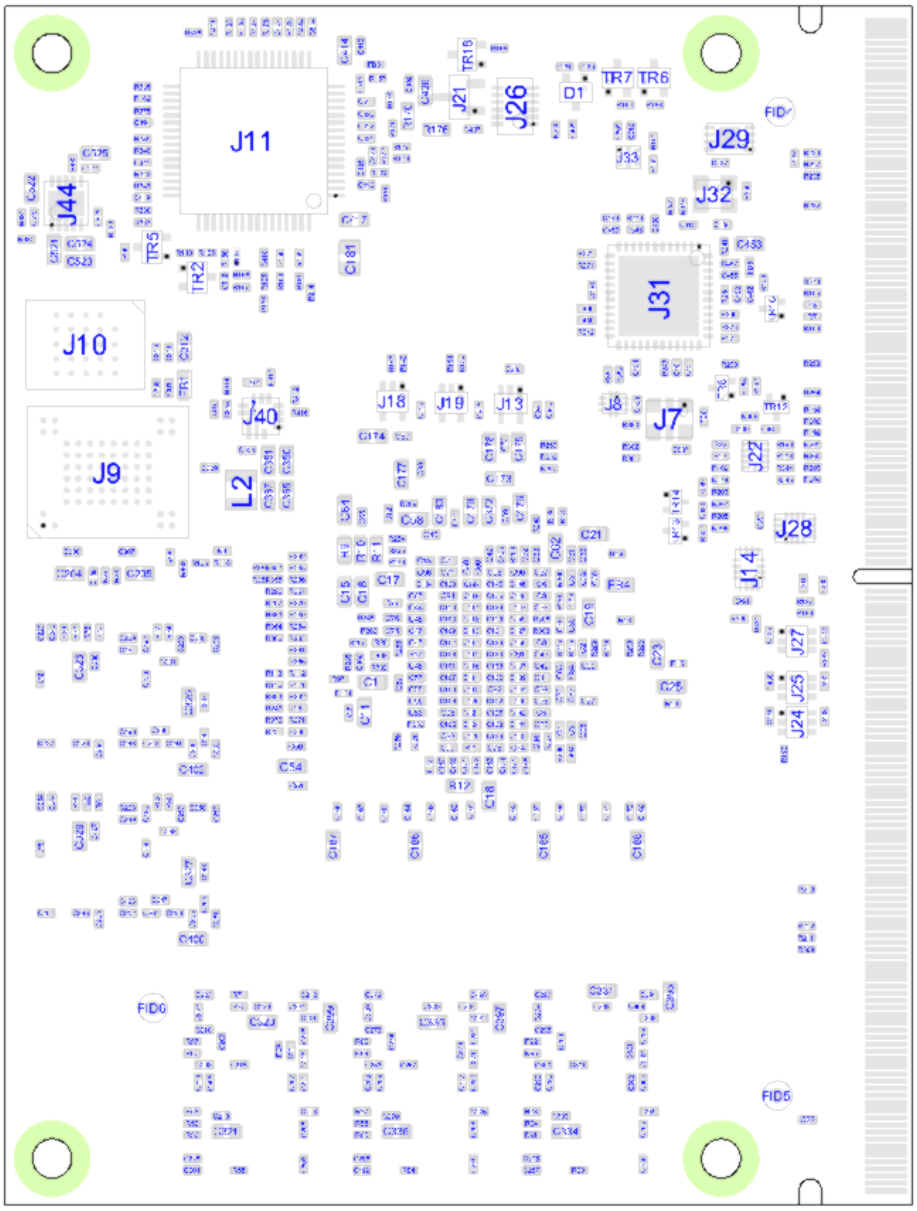

Figure 5-8 Bottom Components

The following table defines the main components on the bottom side:

Part Reference	Manufacturer	Type	Function
J9	SkyHigh	S34MS04G	NAND flash
J10	Micron	MT25QU	QSPI flash
J11	NXP	MK02	MCU
J26	Epson	RX-8803LC	Real-time clock
J29	ST	M24128	EEPROM
J31	IDT	IDT6V49205B	Clock generator

Table 5-5 Bottom side components

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6 Software

6.1 U-Boot

The MPX-LS1043A2 uses an U-Boot as standard boot loader, which is always integrated in the board's QSPI Flash memory on delivery.

Additionally, there’s an U-Boot version available to be placed on microSD card if that interface is implemented on the carrierboard.

More information on selecting the boot source can be found in chapter 4.5.

The U-Boot carries out the following tasks:

- Pin configuration
- CPU configuration
- Clock configuration
- DDR4 configuration and timing

6.2 Operating System

MicroSys Electronics GmbH offers Linux and Microware OS-9 RTOS support for the module.

Other Operating Systems are available on request only.

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7 Safety Requirements And Protective Regulations

7.1 EMC

The System on Module MPX-LS1043A2 is designed according to the requirements of electromagnetic compatibility. Nevertheless, there are several factors which in the target system may require measures against interference.

Active components, especially CPU's of the latest generation do not only operate with high frequencies but also drive very fast signal rise times.

At least the following measures shall be applied:

- Provide sufficient block capacitors in your supply voltages
- Keep short all clock lines in order to prevent interference with other signals
- Shield clock lines with ground planes or keep as much distance as possible to other signals
- provide filtering for all external signals
- provide an EMI proof housing for your electronics

7.2 ESD

For technical reasons there is no ESD protection on the MPX-LS1043A2. Please provide sufficient protection on the baseboard and/or system level.

7.3 Reliability

The SOM MPX-LS1043A2 is available for operation in extended temperature range.

Please note that steady high temperature operation reduces life time of all electronic components. Make sure that no component on the module ever exceeds it's maximum specified temperature during operation or storage. A reasonable cooling concept can dramatically increase lifetime of your electronics.

The MPX-LS1043A2 is designed to withstand a high level of vibration and shock as there are low weight and no overhanging components on the module. If desired, MicroSys Electronics GmbH can support you with your shock and vibration concept. Please ask your sales representative or send an email inquiry to support@microsys.de.

Relevant components on the module are choosen with values for a high level of derating.

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7.4 Climatic conditions

The relative humidity during operation or storage of the module may not exceed 10% to 90%, non condensing.

7.5 Storage Temperatur

The storage temperature of the module described here is -55°C - +100°C

7.6 RoHS

All components of the MPX-LS1043A2 are RoHS compliant, also a RoHS compliant soldering process is used for manufacturing.

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8 General notes

Customers responsibility for chip errata:

It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of.

The manufacturer’s advice should be followed.

If desired, MicroSys Electronics GmbH can support you with your lifecycle management regarding to chip errata. Please ask your sales representative or send an email inquiry to support@microsys.de.

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9 Appendix

9.1 Acronyms

These acronyms are being used within the document; note that this list does not claim to be complete or exhaustive:

COP ..... *Common on-chip processor*
ESD ..... *Electrostatic Discharge*
eSDHC ..... *Enhanced Secured Digital Host Controller*
GND ..... *Ground*
GPIO ..... *General Purpose Input Output*
GPL ..... *General Public License*
I²C ..... *Inter-Integrated Circuit, Inter-Integrated Circuit*
LED ..... *Light Emitting Diode*
MAC ..... *Media Access Control*
MCU ..... *Microcontroller Unit*
PU ..... *Pull-Up Resistor*
QSGMII ..... *Quad Serial Gigabit Media Independent Interface*
QSPI ..... *Quad Serial Peripheral Interface*
RCW ..... *Reset Configuration Word*
RGMII *Reduced Gigabit Media Independent Interface, Reduced Gigabit Media Independent Interface*
RTC ..... *Real-Time clock*
SATA ..... *Serial Advanced Technology Attachment*
SDHC ..... *Secure Digital High Capacity*
SerDes ..... *Serializer Deserializer*
SGMII ..... *Serial Gigabit Media Independent Interface*
SPI ..... *Serial Peripheral Interface*
UART ..... *Universal Asynchronous Receiver/Transmitter*
UCC ..... *Universal Communication Controller*
USB ..... *Universal Serial Bus*

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9.2 Table of Figures

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9.3 Table of Tables

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10 History

Date	Version	Change Description
2017-07-05	1.0	Initial Release Version
2017-08-21	1.1	- Changed Figure 4-1 - Table 4-6 Voltage rails of the module: added VREF-MII and VREF-SDC - Table 4-7: added VREF-MII and VREF-SDC; changed direction of TCK signal; added note relating to onboard clocks - Table 4-7 / Table 4-8: added frequencies - Table 4-9: swapped pins T133/T134 - Table 4-18: Direction corrected for TCK, TMS - Table 4-33 / Table 4-34: added VREF-SDC - Table 4-43 / Table 4-44: added VREF-MII - added cross reference to SerDes clock in chapter 4.11.10 - modified Table 5-2
2017-11-14	2.0	Hardware Revision 2 - Added new temperature sensor (and I2C addresses) - Corrected pin for “COP-TRST#” in Table 4-19 - Added new LED in chapter 4.6 - Re-newed ordering information link to website - Re-newed connector recommendations - Corrected spelling mistakes
2018-01-26	2.1	- Corrected I/O Level of Pins B125, B130, B135 in Table 4-1 - Added USB-ID I/O Level in Table 4-26, Table 4-27, Table 4-28 - UARTx-SIN & UARTx-SOUT re-named UART-RXD & UART-TXD on connector pins in Table 4-32
2018-03-01	2.2	- Added chapter 4.1.3 - Revised chapter 5.1 - Revised chapter 5.3
2020-05-14	2.3	-Table 4-22: corrected bit A3 for I2C address 0x4C - JAE connector obsolete: updated Table 5-2
2021-10-27	2.4	- Table 4-16: GPIO8 → connector pin B123 - Table 4-44: EC2_GTX_CLK125 (ball AG4) → connector pin T77 - Table 4-46: EC2_GTX_CLK125 (ball AG4) → connector pin T77
2021-04-14	2.5	- Added data for power consumption over Tj in Table 3-1
2022-01-05	3.0	Hardware Revision 3 not released – manual skipped

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Date	Version	Change Description
2022-08-02	4.0	- Hardware Revision 4 - Added pins TK1, TK2, BK1, BK2 in chapter 4.2 - Updated pin definitions B89 to B100 in Table 4-1 - Updated Figure 4-2, Table 4-5, Table 4-6 - Added RST-OUT# minimum pulse width in chapter 4.2 - Removed former Table 4-11 - Changed deviation and VRTC range in chapter 4.7 - Added chapter 4.9 - Added chapter 4.11.13 - Added Table 4-20 - Added hint in chapter 4.4 - Added pullups to SPI chip selects in Table 4-24 - Added note in chapter 4.11.3 for I2C-2 - Chapter 4.11.9 redesigned - Added restrictions due to erratum A-010539 in chapter - Added note in chapter 4.11.11 for 125MHz clock - Adjusted top height in Table 5-3 - Updated chapter 5.1 - Updated chapter 5.5 - Updated chapter 5.6 - Added voltage for fuse programming on pin TK2 - Added chapter 4.10 - Changed VRTC range in chapter 4.7 back to 3,3V - Added blinking LED description in chapter 4.6 - Added 100k pullup for SPI-MISO in Table 4-24
2023-05-11	5.0	Hardware Revision 5 - Updated assembly drawings in chapters 5.5 & 5.6 - Added overview in chapter 4.9
2024-06-10	5.1	Removed “SPI-CS0#” for Pin B94 in Table 4-1
2024-09-30	5.2	NAND boot defeatured in chapter 4.5 and 6.1
2024-10-14	5.3	- Adding a storage temperature chapter 7.5 - Fax number removed under chapter 1.3

Table 10-1 Document history

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