miriac MPX-LS1028A

User Manual (HW Revision 2)

V1.0

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1 General Notes

1.1 Warranty

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MicroSys Electronics GmbH
Muehlweg 1
D-82054 Sauerlach
Germany

Phone: +49 8104 801-0
Fax: +49 8104 801-110

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1.5 Symbols, Conventions and Abbreviations

1.5.1 Symbols

Throughout this document, the following symbols will be used:

	Information marked with this symbol MUST be obeyed to avoid the risk of severe injury, health danger, or major destruction of the unit and its environment
	Information marked with this symbol MUST be obeyed to avoid the risk of possible injury, permanent damage or malfunction of the unit.
	Information marked with this symbol gives important hints upon details of this manual, or in order to get the best use out of the product and its features.

Table 1-1 Symbols

1.5.2 Conventions

Symbol	Explanation
# / XXX_B	denotes a low active signal
←	denotes the signal flow in the shown direction
→	denotes the signal flow in the shown direction
↔	denotes the signal flow in both directions
→	denotes the signal flow in the shown direction with additional logic / additional ICs in the signal path
I/O	denotes a bidirectional pin
Input	denotes an input pin
Output	denotes an output pin
matched	denotes the according signal to be routed impedance controlled and length matched
Pin 1	refers to the numeric pin of a component package
Pin a1	refers to the array position of a pin within a component package
XXX- / XXX_N	denotes the negative signal of a differential pair
XXX+ / XXX_P	denotes the positive signal of a differential pair
XXX	denotes an optional not mounted or fitted part

Table 1-2 Conventions

1.6 Safety and Handling Precautions

	**DO NOT exceed the rated maximum values for the power supply! This may result in severe permanent damage to the unit, as well as possible serious injury.** **ALWAYS keep the unit dry, clean and free of foreign objects. Otherwise, irreparable damage may occur.**
	**Parts of the unit may become hot during operation. Take care not to touch any parts of the circuitry during operation to avoid burns and operate the unit in a well-ventilated location. Provide an appropriate cooling solution as required.**
	**ALWAYS take care of ESD-safe handling!** **Many pins on the module connector are directly connected to the CPU or other ESD sensitive devices.** **Make or break ANY connections ONLY while the unit is switched OFF.** **Otherwise, permanent damage to the unit may occur, which is not covered by warranty.**
	**There is no separate SHIELD connection.** **The module's mounting holes are not connected to GND** **Take this into account when handling and mounting the unit.**

Table 1-3 Safety and Handling Precautions

2 Short Description

The miriac MPX-LS1028A is a member of the MPX module family based on NXP's QorIQ® Layerscape LS1028A Multicore Communications Processor.

MicroSys Electronics GmbH offers a Starterkit which provides the key features of the module. The customer can:

- …evaluate the basic concept of the standard
- …test the operation of the MPX-LS1028A module
- …evaluate the main interfaces of the LS1028A CPU
- …test the provided software
- …start developing

3 System Description

3.1 Block Diagram

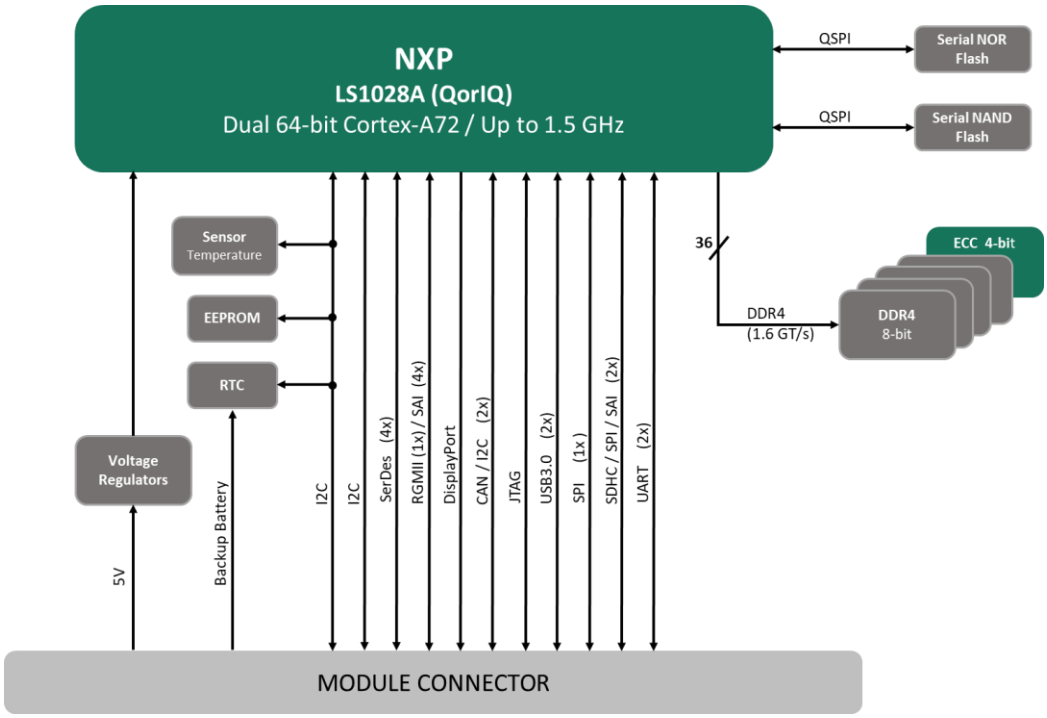

Figure 3-1 Block Diagram

3.2 System Components

- QorIQ Layerscape processor LS1028A (dual core) or LS1018A (single core)
- DDR4 SDRAM
- Clock Generators for CPU and interface clocks
- Serial NOR flash as boot or storage device
- Serial NAND flash as boot or storage device
- I²C EEPROM
- I²C temperature sensor
- I²C RTC
- Voltage regulators for the onboard voltages

3.3 Power Consumption

The MPX-LS1028A is supplied by a single input power rail of 5V nominal.

The typical power consumption values for the module are determined on a CRX07 carrier running U-Boot (idle) at room temperature with heatsink and 25mm fan:

- LS1028A (dual core)
- CPU core frequency 1500 MHz (2 cores enabled / 1 core used by U-Boot)
- 400 MHz bus clock
- 4 GBytes of DDR4 memory + ECC (1600 MHz)
- ~5.6 Watt

3.4 Cooling

In chapter 3.3 the power consumption of the MPX-LS1028A module was specified. With this information a cooling method needs to be designed suitable for the final use case. If desired, MicroSys Electronics GmbH can support you with your cooling concept. Please ask your sales representative or send an email inquiry to support@microsys.de.

Please make sure that the cooling solution is always sufficiently dimensioned to keep the operating temperature of all parts below the maximum specified temperature.

The most critical parts are listed in the following tables.

Commercial temperature grade (0/+70° C) variants:

Component	Temperature (max.)	Description
CPU	105° C	Junction Temperature
DDR	85° C	Case Temperature
Core Regulator	150° C	Junction Temperature
DDR Regulator	125° C	Junction Temperature

Table 3-1 Commercial grade variants: maximum temperature

Industrial temperature grade (-40/+85° C) variants:

Component	Temperature (max.)	Description
CPU	105° C	Junction Temperature
DDR	95° C	Case Temperature
Core Regulator	150° C	Junction Temperature
DDR Regulator	125° C	Junction Temperature

Table 3-2 Industrial grade variants: maximum temperature

3.5 Ordering Information

Ordering information can be found on the website

https://microsys.de/produkte/system-on-modules/qoriq/miriactm-mpx-ls1028a.html?L=1

or contact your local sales representative.

4 Technical Description

4.1 Pinouts

The signal direction is from the module's view. For example, DP_LANE3_P (pin B39) is an output from the module and an input to peripheral devices on the carrier board.

The following table gives an overview of the 230 pins of the module's edge finger. For a detailed connector description see chapter 5.1. The pins will be described in chapter 4.10 and the following sections.

The signal names in the following two tables do not show all available options for each pin. Pin multiplexing can only be implemented in combination with the vendor's datasheet.

4.1.1 Module Connector – Top Pins

Pin	Pin Name / Primary Function	Alternate Functions	GPIO?
T1	GND	---	---
T2	N.C.	---	---
T3	N.C.	---	---
T4	BOOT_INV	---	---
T5	HRST#	---	---
T6	TA_TMP_DETECT#	---	---
T7	RSTIN#	---	---
T8	GND	---	---
T9	SDHC2_CMD	✓	GPIO2_DAT19
T10	GND	---	
T11	SDHC2_CLK	✓	GPIO2_DAT09
T12	GND	---	
T13	GND	---	
T14	SDHC2_DAT3	✓	GPIO2_DAT14
T15	SDHC2_DAT2	✓	GPIO2_DAT13
T16	SDHC2_DAT1	✓	GPIO2_DAT12
T17	SDHC2_DAT0	✓	GPIO2_DAT11
T18	GND	---	
T19	SDHC2_DS	✓	GPIO2_DAT10
T20	GND	---	

Pin	Pin Name / Primary Function	Alternate Functions	GPIO?
T21	SDHC1_DAT3	✓	GPIO1_DAT20
T22	SDHC1_DAT2	✓	GPIO1_DAT19
T23	SDHC1_DAT1	✓	GPIO1_DAT18
T24	SDHC1_DAT0	✓	GPIO1_DAT17
T25	GND	---	
T26	SDHC1_CMD	✓	GPIO1_DAT21
T27	GND	---	
T28	SDHC1_CLK	✓	GPIO1_DAT16
T29	GND	---	---
T30	SD_CLK100_N	---	---
T31	SD_CLK100_P	---	---
T32	GND	---	---
T33	SD_CLKIN_N	---	---
T34	SD_CLKIN_P	---	---
T35	GND	---	---
T36	SD1_TX3_N	---	---
T37	SD1_TX3_P	---	---
T38	GND	---	---
T39	SD1_RX3_N	---	---
T40	SD1_RX3_P	---	---
T41	GND	---	---
T42	SD1_TX2_N	---	---
T43	SD1_TX2_P	---	---
T44	GND	---	---
T45	SD1_RX2_N	---	---
T46	SD1_RX2_P	---	---
T47	GND	---	---
T48	SD1_TX1_N	---	---
T49	SD1_TX1_P	---	---
T50	GND	---	---
T51	SD1_RX1_N	---	---
T52	SD1_RX1_P	---	---
T53	GND	---	---

Pin	Pin Name / Primary Function	Alternate Functions	GPIO?
T54	SD1_TX0_N	---	---
T55	SD1_TX0_P	---	---
T56	GND	---	---
T57	SD1_RX0_N	---	---
T58	SD1_RX0_P	---	---
T59	GND	---	---
T60	EMI1_MDIO	---	---
T61	GND	---	---
T62	EMI1_MDC	---	---
T63	GND	---	---
T64	EC1_TX_EN	✓	GPIO3_DAT08
T65	GND	---	
T66	EC1_TXD3	✓	GPIO3_DAT12
T67	EC1_TXD2	✓	GPIO3_DAT11
T68	EC1_TXD1	✓	GPIO3_DAT10
T69	EC1_TXD0	✓	GPIO3_DAT09
T70	GND	---	
T71	EC1_GTX_CLK	✓	GPIO3_DAT07
T72	GND	---	---
T73	USB1_ID	---	---
T74	USB1_VBUS	---	---
T75	GND	---	---
T76	USB1_SSTX_N	---	---
T77	USB1_SSTX_P	---	---
T78	GND	---	---
T79	USB1_SSRX_N	---	---
T80	USB1_SSRX_P	---	---
T81	GND	---	---
T82	USB1_D_N	---	---
T83	USB1_D_P	---	---
T84	GND	---	---
T85	SPI3_MOSI	✓	GPIO3_DAT16
T86	SPI3_MISO	✓	GPIO3_DAT13

Pin	Pin Name / Primary Function	Alternate Functions	GPIO?
T87	SPI3_SCK	✓	GPIO3_DAT14
T88	GND	---	
T89	SPI3_CS2#	✓	GPIO3_DAT18
T90	SPI3_CS1#	✓	GPIO3_DAT17
T91	SPI3_CS0#	✓	GPIO3_DAT15
T92	VCC_RTC	---	---
T93	GND	---	---
T94	EVDD_VCC	---	---
T95	GND	---	---
T96	1V8	---	---
T97	1V8	---	---
T98	GND	---	---
T99	3V3	---	---
T100	3V3	---	---
T101	5V0_VIN	---	---
T102	5V0_VIN	---	---
T103	5V0_VIN	---	---
T104	5V0_VIN	---	---
T105	5V0_VIN	---	---
T106	5V0_VIN	---	---
T107	5V0_VIN	---	---
T108	5V0_VIN	---	---
T109	GND	---	---
T110	GND	---	---
T111	GND	---	---
T112	GND	---	---
T113	GND	---	---
T114	GND	---	---
T115	GND	---	---

Table 4-1 Module connector: top pins

4.1.2 Module Connector – Bottom Pins

Pin	Pin Name / Primary Function	Secondary Function	GPIO?
B1	IRQ0#	---	See chapter 4.9
B2	IRQ1#	---	See chapter 4.9
B3	PCIE_RST#	---	GPIO2_DAT29
B4	WD_TRIG#	---	GPIO2_DAT31
B5	N.C.	---	---
B6	TA_PROG_SFP	---	---
B7	GND	---	
B8	CFG_RCW3/GPIO	✓	GPIO2_DAT07
B9	CFG_RCW2/GPIO	✓	GPIO2_DAT06
B10	GND	---	
B11	I2C8_SDA	✓	GPIO2_DAT17
B12	I2C8_SCL	✓	GPIO2_DAT18
B13	GND	---	
B14	I2C7_SDA	✓	GPIO2_DAT15
B15	I2C7_SCL	✓	GPIO2_DAT16
B16	GND	---	
B17	I2C6_SDA	✓	GPIO1_DAT22
B18	I2C6_SCL	✓	GPIO1_DAT23
B19	GND	---	
B20	I2C5_SDA	✓	GPIO1_DAT24
B21	I2C5_SCL	✓	GPIO1_DAT25
B22	GND	---	
B23	I2C4_SDA	✓	GPIO1_DAT26
B24	I2C4_SCL	✓	GPIO1_DAT27
B25	GND	---	
B26	I2C3_SDA	✓	GPIO1_DAT28
B27	I2C3_SCL	✓	GPIO1_DAT29
B28	GND	---	
B29	I2C2_SDA	✓	GPIO1_DAT30
B30	I2C2_SCL	✓	GPIO1_DAT31
B31	GND	---	---

Pin	Pin Name / Primary Function	Secondary Function	GPIO?
B32	I2C1_SDA	---	---
B33	I2C1_SCL	---	---
B34	GND	---	---
B35	DP_AUX_N	---	---
B36	DP_AUX_P	---	---
B37	GND	---	---
B38	DP_LANE3_N	---	---
B39	DP_LANE3_P	---	---
B40	GND	---	---
B41	DP_LANE2_N	---	---
B42	DP_LANE2_P	---	---
B43	GND	---	---
B44	DP_LANE1_N	---	---
B45	DP_LANE1_P	---	---
B46	GND	---	---
B47	DP_LANE0_N	---	---
B48	DP_LANE0_P	---	---
B49	GND	---	---
B50	DP_HPD	---	---
B51	GND	---	---
B52	EC1_RX_DV	✓	GPIO3_DAT00
B53	EC1_RX_CLK	✓	GPIO3_DAT01
B54	GND	---	
B55	EC1_RXD3	✓	GPIO3_DAT05
B56	EC1_RXD2	✓	GPIO3_DAT04
B57	EC1_RXD1	✓	GPIO3_DAT03
B58	EC1_RXD0	✓	GPIO3_DAT02
B59	GND	---	
B60	EC1_GTX_CLK125	✓	GPIO3_DAT06
B61	GND	---	---
B62	USB2_ID	---	---
B63	USB2_VBUS	---	---
B64	GND	---	---

Pin	Pin Name / Primary Function	Secondary Function	GPIO?
B65	USB2_SSTX_N	---	---
B66	USB2_SSTX_P	---	---
B67	GND	---	---
B68	USB2_SSRX_N	---	---
B69	USB2_SSRX_P	---	---
B70	GND	---	---
B71	USB2_D_N	---	---
B72	USB2_D_P	---	---
B73	GND	---	---
B74	N.C.	---	---
B75	N.C.	---	---
B76	GND	---	---
B77	BSCAN_EN#	---	---
B78	JTRST#	---	---
B79	JTMS	---	---
B80	JTDO	---	---
B81	JTDI	---	---
B82	GND	---	---
B83	JTCK	---	---
B84	GND	---	---
B85	GND	---	---
B86	UART2_RXD	✓	GPIO1_DAT06
B87	UART2_TXD/CFG_RCW0	✓	GPIO1_DAT07
B88	GND	---	
B89	UART1_RXD	✓	GPIO1_DAT10
B90	UART1_TXD/CFG_RCW1	✓	GPIO1_DAT11
B91	GND	---	---
B92	VCC_RTC	---	---
B93	GND	---	---
B94	EVDD_VCC	---	---
B95	GND	---	---
B96	1V8	---	---
B97	1V8	---	---

Pin	Pin Name / Primary Function	Secondary Function	GPIO?
B98	GND	---	---
B99	3V3	---	---
B100	3V3	---	---
B101	5V0_VIN	---	---
B102	5V0_VIN	---	---
B103	5V0_VIN	---	---
B104	5V0_VIN	---	---
B105	5V0_VIN	---	---
B106	5V0_VIN	---	---
B107	5V0_VIN	---	---
B108	5V0_VIN	---	---
B109	GND	---	---
B110	GND	---	---
B111	GND	---	---
B112	GND	---	---
B113	GND	---	---
B114	GND	---	---
B115	GND	---	---

Table 4-2 Module connector: bottom pins

4.2 Power Structure

The MPX-LS1028A module is supplied by a single 5V supply. For RTC backup buffering an additional supply from the carrier board is necessary.

The module itself does not provide any supply voltage to the carrier but it has some reference voltages that show the voltage level of the respective interface on the module. If necessary, the carrier board must track the reference voltages and generate a copy which can carry higher loads.

The following diagram shows the structure of the power supplies:

The following table shows the internal connections:

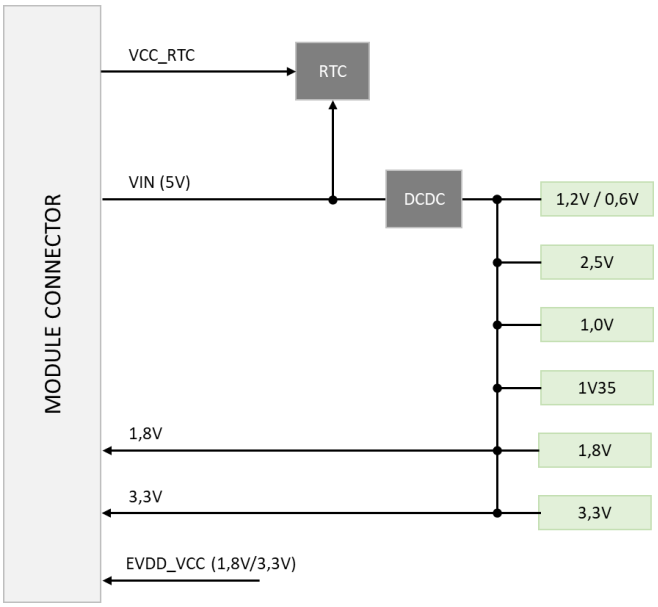

Figure 4-1 Power Structure

Module Connector			
Pin	**Signal**	**I/O Range**	**Signal conditioning**
T101-T108 / B101-B108	VIN	5V (± 5%)	
T92, B92	VCC_RTC	1,2V-5.5V	
T94, B94	EVDD_VCC	1.8V / 3.3V	Maximum current to be drawn: 250mA
T96, T97, B96, B97	1V8	1.8V	Maximum current to be drawn: 250mA
T99, T100, B99, B100	3V3	3.3V	Maximum current to be drawn: 250mA

Table 4-3 Module connector: power pin assignments

The voltages which are necessary for the CPU and peripheral devices are generated from the input voltage on the module. The voltages are:

Voltage rail	Tolerance	Description
1.0V	1.0V ± 30mV	CPU core voltage
1.2V	1.2V ± 60mV	DDR4 memory voltage
0.6V	0.6V ± 25mV	DDR4 termination voltage
0.6V	0.6V ± 15mV	DDR4 reference voltage
2.5V	2.5V ± 125mV	DDR4 wordline supply voltage
1.35V	1.35V ± 67mV	SerDes transmitter voltage
1.8V	1.8V ± 90mV	PLL, GPIO, Ethernet voltage & peripheral devices
3.3V	3.3V ± 165mV	USB voltage & peripheral devices

Table 4-4 Voltage rails of the module

4.3 Reset Structure

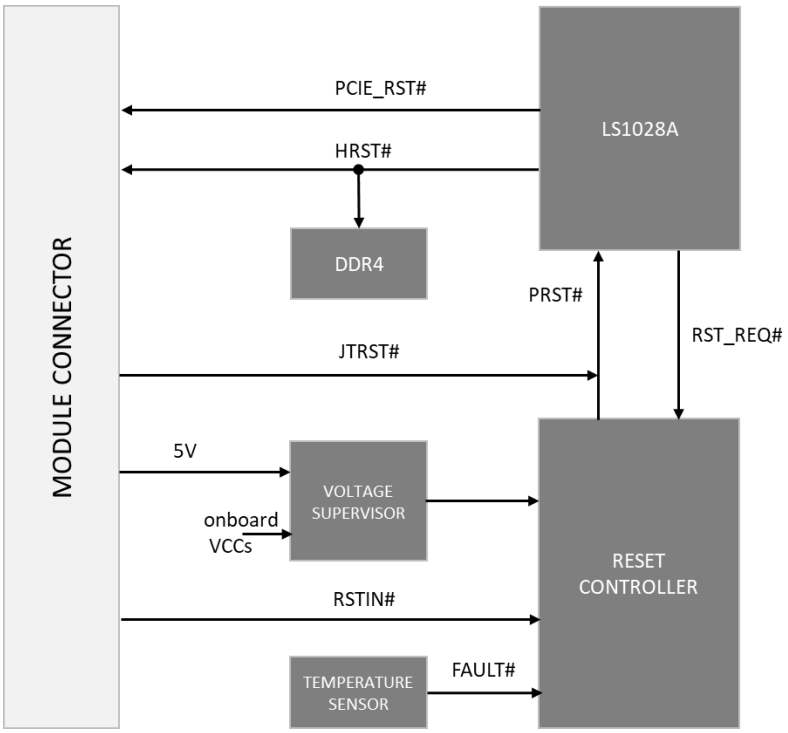

Figure 4-2 Reset Structure

The reset structure of the MPX-LS1028A module is shown in Figure 4-2. For the basic operation only RSTIN# and HRST# are necessary.

In case the input supply is within limits the module will initially start. Any power fail will immediately trigger a reset.

The RSTIN# is an input to the module. It signals that the voltage supplies on the carrier board are within their limits and no manual reset was triggered. When active (signal is low) the reset controller on the module initiates the (power-on) reset sequence to keep the CPU in a defined reset state. No further interaction from the carrier board is necessary. In case the module reset is active, the CPU triggers the HRST# signal which is intended to control the reset of peripheral devices on the carrier board i.e. Ethernet PHYs and other devices. PCIe slots and devices can optionally be reset by the PCIE_RST# signal, which is a GPOUT of the CPU.

Please note that the HRST# reset timing is controlled by the CPU, thus the pulse length and timing may vary.

JTRST# is for JTAG and debugging purposes and should be controlled by external debuggers, for example Lauterbach's TRACE32 or NXP’s CodeWarrior TAP.

The following table shows the internal connections:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
-	-	←	T7	RSTIN#	5,0V (VIN)	SR: 100R PU: 2k2
AB2	HRESET_B	→	T5	HRST#	1,8V	PU: 4k7
D14	GPIO2_DAT29	→	B3	PCIE_RST#	1,8V	-
Y6	PORESET_B	←	B78	JTRST#	1,8V	PU: 10k

Table 4-5 Reset signals: overview

4.4 Clock Structure

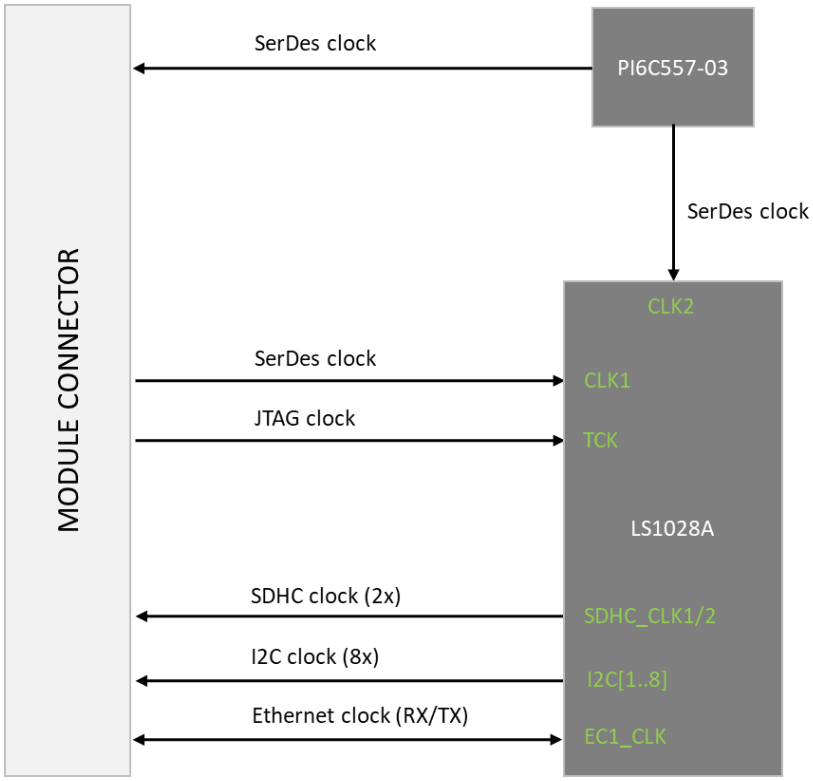

Figure 4-3 Clock Structure

The following table shows the available clocks on the MPX-LS1028A:

CPU			Module Connector				
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**	**Frequency**
M6	SDHC1_CLK	→	T28	SDHC1_CLK	EVDD	SR: 10R	t.b.d
F20	SDHC2_CLK	→	T11	SDHC2_CLK	1V8	SR: 10R	t.b.d
K6	SPI3_CLK	→	T87	SPI3_CLK	1V8	SR: 0R	t.b.d.
R5	IIC1_SCL	→	B33	I2C1_SCL	1V8	PU: 1k	400 kHz
U1	IIC2_SCL	→	B30	I2C2_SCL	1V8		400 kHz
V2	IIC3_SCL	→	B27	I2C3_SCL	1V8		400 kHz
U7	IIC4_SCL	→	B24	I2C4_SCL	1V8		400 kHz
P2	IIC5_SCL	→	B21	I2C5_SCL	1V8		400 kHz
F16	IIC6_SCL	→	B18	I2C6_SCL	1V8	PD: 100k	400 kHz

CPU			Module Connector				
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**	**Frequency**
D20	IIC7_SCL	→	B15	I2C7_SCL	1V8	PU: 49k9	400 kHz
H22	IIC8_SCL	→	B12	I2C8_SCL	1V8	PU: 49k9	400 kHz
W7	TCK	←	B83	JTCK	1V8	PU: 10k	t.b.d.
AH4	EC1_GTX_CLK	→	T71	EC1_GTX_CLK	1V8	SR: 10R	125 MHz
AD2	EC1_RX_CLK	←	B53	EC1_RX_CLK	1V8		125 MHz
AK2	EC1_GTX_CLK 125	←	B60	EC1_GTX_CLK125	1V8		125 MHz
AG9	SD1_REF_CLK 1_N	←	T33	SD_CLKIN_N	HCSL	PD: 49R9	100 MHz
AF10	SD1_REF_CLK 1_P	←	T34	SD_CLKIN_P	HCSL	PD: 49R9	100 MHz

Table 4-6 Clock: pin assignments

PI6C557-03			Module Connector				
Pin	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**	**Frequency**
10	CLK-	→	T30	SD_CLK100_N	HCSL	SR: 33R PD: 49R9	100 MHz
11	CLK+	→	T31	SD_CLK100_P	HCSL	SR: 33R PD: 49R9	100 MHz

Table 4-7 SerDes clock: pin assignments

4.5 Boot Sources

The MPX-LS1028A module offers the option of booting from different boot devices.

The following table shows the boot devices supported by hardware.

Some options may be restricted by software.

Please contact MicroSys for currently supported boot devices.

Not listed combinations are reserved.

cfg_rcw_src[3:0]	Boot Source	Description	Boot Location
1000	SDHC1	SD-Card	carrier board
1001	SDHC2	eMMC	carrier board
1010	I2C1	I2C address 0x50 (7 bit address), 2 bytes addressing only	carrier board
1101	XSPI1	Serial NAND Flash	module
1111		Serial NOR Flash	module

Table 4-8 Boot devices: overview

The boot source can be selected by means of four pins which are directly connected to the LS1028A CPU. These pins are sampled during the rising edge of the CPU reset and must be pulled to a defined level on the carrier board.

Do not leave them floating.

A logical 1 is represented by pulling the ***cfg_rcw_src*** pin to 1,8V, whereas a logical 0 can be achieved by pulling the pin to ground.

Recommended resistors:

- Pullup: 10k
- Pulldown: 4k7

	Pin	Signal	I/O Range	Signal conditioning
cfg_rcw_src3	B8	CFG_RCW3/GPIO	1,8V	---
cfg_rcw_src2	B9	CFG_RCW2/GPIO	1,8V	---
cfg_rcw_src1	B90	UART1_TXD	1,8V	---
cfg_rcw_src0	B87	UART2_TXD	1,8V	---

Table 4-9 Boot select pins: pin assignments

4.6 LEDs

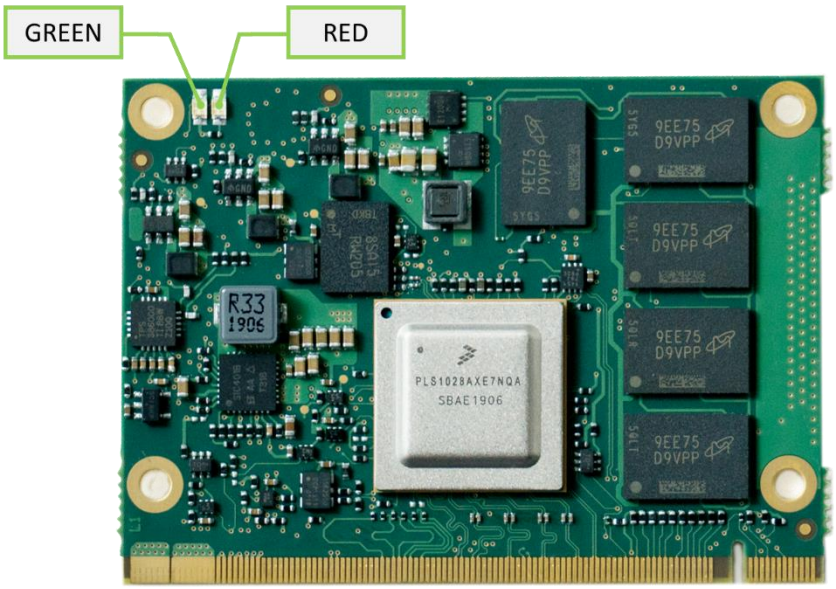

Figure 4-4 LEDs

Colour	Function	
Green	LED ON:	Power-up sequence of the module is finished, power is good
	LED OFF:	Power fail
Red	LED ON:	Module reset is active
	LED OFF:	Reset is inactive

Table 4-10 LED: pin description

4.7 RTC

The Real-Time Clock (RTC) is implemented with an NXP PCF85063ATT chip:

- I²C clock frequency up to 400 kHz
- Operating temperature -40°C to 85°C
- Slave address according to Table 4-18

The RTC is supplied by the input voltage. Any backup voltage needs to be provided on the carrier board if buffering is desired. The following table shows the internal connection:

Module Connector			
Pin	**Signal**	**I/O Range**	**Signal conditioning**
T92, B92	VCC_RTC	1.2V – 5.5V	See Figure 4-5

NOTE

In case a non-rechargeable battery is connected, make sure VCC_RTC is lower than VIN. Otherwise the battery will be unnecessarily drained.

The RTC will continue operating until 0,9V at the end of battery discharge, thus 1,2V is a theoretical limit taking temperature rise and diode drop into account.

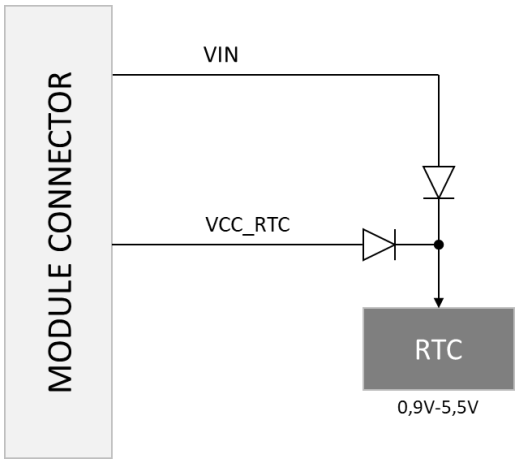

Figure 4-5 RTC: buffering

The RTC's interrupt output is connected to the GPIO Expander:

GPIO Expander			PCF85063ATT			
Pin	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
8	RTC_IRQ#	←	3	INT#	1.8V	PU: 1k

Table 4-11 RTC: IRQ

4.8 Temperature sensor

The LS1028A has an integrated temperature diode which is connected to a TMP451 temperature sensor from Texas Instruments.

- I²C clock frequency up to 400 kHz
- Operating temperature -40°C to 125°C
- Slave address according to Table 4-18
- Local temperature monitoring (TMP451 internal temperature)
- Remote temperature monitoring (LS1028A temperature diode)
- Two interrupts for adjusting two temperature thresholds

	Ambient: 0°C / +70°C	**Ambient: -40°C / +125°C**
Local Temperature (of the sensor itself)	Max. ± 1°C	Max. ± 2°C
Remote Temperature (of the CPU internal diode)	Max. ± 1°C	Max. ± 4°C

Figure 4-6 Temperature sensor: accuracy

The temperature sensor provides two interrupts which are connected to the GPIO Expander:

GPIO Expander			**TMP451**			
Pin	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
12	THERM_ALERT#	←	6	ALERT#/THERM2	1.8V	PU: 1k
11	THERM_FAULT#	←	4	THERM#	1.8V	PU: 1k

Table 4-12 Temperature sensor: IRQs

4.9 GPIO Expander

The scope of functions on the LS1028A is extended by a GPIO expander FXL6408:

- I²C clock frequency up to 400 kHz
- Slave address according to Table 4-18
- One interrupt out signaling pin state changes

It has 8 GPIOs which are used as follows:

GPIO Expander						
Pin	**Signal**			**Pin**	**Signal**	**Signal conditioning**
12	GPIO0	←	J30	6	THERM_ALERT#	PU: 1k
11	GPIO1	←	J30	4	THERM_FAULT#	PU: 1k
8	GPIO2	←	J7	3	RTC_IRQ#	PU: 1k
7	GPIO3	←	ST6	B2	IRQ1#	PU: 1k
6	GPIO4	←	ST6	B1	IRQ0#	PU: 1k
5	GPIO5	←	---	---	HW_REV2	See Table 4-14
4	GPIO6	←	---	---	HW_REV1	
3	GPIO7	←	---	---	HW_REV0	

Table 4-13 GPIO Expander: pin description

HW_REV2	HW_REV1	HW_REV0	Description
0	0	0	Hardware Revision 1
0	0	1	Hardware Revision 2
0	1	0	Hardware Revision 3
0	1	1	Hardware Revision 4
1	0	0	Hardware Revision 5
1	0	1	Hardware Revision 6
1	1	0	Hardware Revision 7
1	1	1	Hardware Revision 8

Table 4-14 GPIO Expander: Hardware Revision

CPU			GPIO Expander		
Ball	**Signal**		**Pin**	**Signal**	**Signal conditioning**
F14	GPIO2_DAT28	←	1	EXPD_IRQ#	PU: 10k

Table 4-15 GPIO Expander: IRQ

4.10 Interface Description

In the following chapters the interfaces, their pins and the common multiplexing options are explained.

The tables list the multiplexing options as “functions” arranged by columns. If functions are listed in the same column it does not necessarily mean that they can exist at the same time. Pin multiplexing is finally done by software and configured in the reset configuration word (“RCW”).

The terms “primary”, “secondary”, … do not imply any priority. The connector’s pin names are derived from the primary functions.

4.10.1 JTAG

The following table shows the internal connections of the JTAG interface:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
V4	TDI	←	B81	JTDI	1.8V	
W1	TDO	→	B80	JTDO	1.8V	
W7	TCK	←	B83	JTCK	1.8V	PU: 10k
V6	TMS	←	B79	JTMS	1.8V	
Y2	TRST#	←	B78	JTRST#	1.8V	PU: 10k
W5	TBSCAN_EN#	←	B77	BSCAN_EN#	1.8V	PU: 4k7

Table 4-16 JTAG interface: pin assignments

4.10.2 CAN

The two FlexCAN interfaces of the LS1028A are implemented for CAN2.0 version B and CAN FD protocols at data rates up to 8Mb/s. CAN transceivers are not installed on the module.

CAN is not a primary function and the pins are shared with I2C3 and I2C4. See Table 4-19 for details.

4.10.3 SAI

The LS1028A provides a maximum of six identical SAI modules.

None of the SAIs is a primary interface, which is why all of them share their pins with other interfaces:

- SAI 1: see Table 4-30
- SAI 2: see Table 4-30
- SAI 3: see Table 4-35
- SAI 4: see Table 4-35
- SAI 5: see Table 4-35
- SAI 6: see Table 4-35

4.10.4 I2C

The MPX-LS1028A module offers a maximum of eight independent I²C busses which run at up to 400kHz. All I²C pins have multiplexing options except for I2C1 which is a dedicated I2C bus that is also used on the module.

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
T4	IIC1_SDA	↔	B32	I2C1_SDA	1,8V	PU: 1k
R5	IIC1_SCL	→	B33	I2C1_SCL	1,8V	PU: 1k
T2	IIC2_SDA	↔	B29	I2C2_SDA	1,8V	
U1	IIC2_SCL	→	B30	I2C2_SCL	1,8V	
U3	IIC3_SDA	↔	B26	I2C3_SDA	1,8V	
V2	IIC3_SCL	→	B27	I2C3_SCL	1,8V	
T6	IIC4_SDA	↔	B23	I2C4_SDA	1,8V	
U7	IIC4_SCL	→	B24	I2C4_SCL	1,8V	
R1	IIC5_SDA	↔	B20	I2C5_SDA	1,8V	
P2	IIC5_SCL	→	B21	I2C5_SCL	1,8V	
H16	IIC6_SDA	↔	B17	I2C6_SDA	1,8V	
F16	IIC6_SCL	→	B18	I2C6_SCL	1,8V	
G19	IIC7_SDA	↔	B14	I2C7_SDA	1,8V	PU: 49k9
D20	IIC7_SCL	→	B15	I2C7_SCL	1,8V	PU: 49k9
H20	IIC8_SDA	↔	B11	I2C8_SDA	1,8V	PU: 49k9
H22	IIC8_SCL	→	B12	I2C8_SCL	1,8V	PU: 49k9

Table 4-17 I2C: pin assignments

I2C1 has the following layout:

Device		**A6**	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**	**7 bit**
GPIO Expander	FXL6408	1	0	0	0	0	1	1	1/0	0x43
Temperature Sensor	TMP451 (slave address)	1	0	0	1	1	0	0	1/0	0x4C
	TMP451 (General Call reset address)	0	0	0	0	0	0	0	-/0	0x00
RTC	PCF85063	1	0	1	0	0	0	1	1/0	0x51
EEPROM	BR24G128	1	0	1	0	1	0	0	1/0	0x54

Table 4-18 I2C1: bus map

The I2C interfaces have different multiplexing options. The most common functions are displayed in the following table. Please refer to the NXP datasheet for all possible combinations and potential group limitations:

Pin	Primary function	Secondary function	Tertiary function	Quaternary function	GPIO
B33	IIC1_SCL	---	---	---	---
B32	IIC1_SDA	---	---	---	---
B30	IIC2_SCL	---	SDHC1_CD_B	---	GPIO1_DAT31
B29	IIC2_SDA	---	SDHC1_WP	---	GPIO1_DAT30
B27	IIC3_SCL	LPUART1_SOUT	CAN1_TX	EVT5_B	GPIO1_DAT29
B26	IIC3_SDA	LPUART1_SIN	CAN1_RX	EVT6_B	GPIO1_DAT28
B24	IIC4_SCL	LPUART1_CTS_B	CAN2_TX	EVT7_B	GPIO1_DAT27
B23	IIC4_SDA	LPUART1_RTS_B	CAN2_RX	EVT8_B	GPIO1_DAT26
B21	IIC5_SCL	---	SDHC1_CLK_SYNC_OUT	EVT1_B	GPIO1_DAT25
B20	IIC5_SDA	---	SDHC1_CLK_SYNC_IN	EVT2_B	GPIO1_DAT24
B18	IIC6_SCL	USB2_PWRFAULT	SDHC2_CLK_SYNC_OUT	EVT3_B	GPIO1_DAT23
B17	IIC6_SDA	USB2_DRVVBUS	SDHC2_CLK_SYNC_IN	EVT0_B	GPIO1_DAT22
B15	IIC7_SCL	LPUART4_CTS_B	SDHC2_DAT5	XSPI1_B_DATA5	GPIO2_DAT16
B14	IIC7_SDA	LPUART4_RTS_B	SDHC2_DAT4	XSPI1_B_DATA4	GPIO2_DAT15
B12	IIC8_SCL	LPUART4_SOUT	SDHC2_DAT7	XSPI1_B_DATA7	GPIO2_DAT18
B11	IIC8_SDA	LPUART4_SIN	SDHC2_DAT6	XSPI1_B_DATA6	GPIO2_DAT17

Table 4-19 I2C pin multiplexing options

4.10.5 XSPI

The MPX-LS1028A uses the XSPI port A to connect both a serial NOR and a serial NAND flash. Port B is routed to the carrier board to connect further devices. “Combination mode” as mentioned in the NXP reference manual is not supported.

The following tables show the internal connections:

CPU			QSPI NOR Flash MT25QU128ABA8E12		
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**
H12	XSPI1_A_CS0#	→	C2	CS#	1.8V
D12	XSPI1_A_CS1#				
H10	XSPI1_A_SCK	→	B2	CLK	1.8V
			B3	GND	
G11	XSPI1_A_DATA0	↔	D3	D0	1.8V
F12	XSPI1_A_DATA1	↔	D2	D1	1.8V
H14	XSPI1_A_DATA2	↔	C4	D2	1.8V
E13	XSPI1_A_DATA3	↔	D4	D3	1.8V
			B4	+1.8V	

Table 4-20 XSPI NOR Flash: pin assignments

CPU			QSPI NAND Flash TC58CYG2S0HRAIG		
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**
H12	XSPI1_A_CS0#	→	1	CS#	1.8V
D12	XSPI1_A_CS1#				
H10	XSPI1_A_SCK	→	6	CLK	1.8V
			4	GND	
G11	XSPI1_A_DATA0	↔	5	SO0	1.8V
F12	XSPI1_A_DATA1	↔	2	SO1	1.8V
H14	XSPI1_A_DATA2	↔	3	SO2	1.8V
E13	XSPI1_A_DATA3	↔	7	SO3	1.8V
			8	+1.8V	

Table 4-21 XSPI NAND Flash: pin assignments

Port A, chip select 0 is always used for the boot device. Therefore, an additional signal “BOOT_INV” is introduced on the module connector:

			Module Connector			
BOOT_INV =			**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
0:	CS0# = NOR CS1# = NAND	←	T4	BOOT_INV	1.8V	PD: 100k
1:	CS0# = NAND CS1# = NOR					

Table 4-22 XSPI: BOOT_INV signal

4.10.6 SPI

The MPX-LS1028A CPU provides three SPI interfaces. One of them, SPI3, is routed as the primary function to the module connector. It has a maximum of three chip selects.

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
K4	SPI3_SIN	←	T86	SPI3_MISO	1.8V	
J5	SPI3_SOUT	→	T85	SPI3_MOSI	1.8V	
U2	SPI3_SCK	→	T87	SPI3_CLK	1.8V	
H6	SPI3_PCS0	→	T91	SPI3_CS0#	1.8V	PU: 100k
H8	SPI3_PCS1	→	T90	SPI3_CS1#	1.8V	PD: 100k
G7	SPI3_PCS2	→	T89	SPI3_CS2#	1.8V	

Table 4-23 SPI3: pin assignments

Only chip select 0 has a pullup resistor on the module.

The chip selects 1 and 2 are often used for USB control signals.

Pin	Primary function	Secondary function	GPIO
K4	SPI3_SIN	EC1_1722_DAT2	GPIO3_DAT13
J5	SPI3_SOUT	EC1_1588_ALARM_OUT2	GPIO3_DAT16
U2	SPI3_SCK	EC1_1722_DAT3	GPIO3_DAT14
H6	SPI3_PCS0	EC1_1588_TRIG_IN2	GPIO3_DAT15
H8	SPI3_PCS1	USB_PWRFAULT	GPIO3_DAT17
G7	SPI3_PCS2	USB_DRVVBUS	GPIO3_DAT18

Table 4-24 SPI3: pin multiplexing options

4.10.7 USB

The MPX-LS1028A has two USB3.0 ports which can be configured as host or device.

All ports support super-speed (5 Gbit/s), high-speed (480 Mbit/s), full-speed (12 Mbit/s), and low-speed (1.5 Mbit/s) operations.

When OTG is enabled, super-speed operation is not supported.

The following table shows the internal connections:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
H4	USB1_VBUS	←	T74	USB1_VBUS	0 – 5.25V	
D4	USB1_ID	←	T73	USB1_ID	0 - 1,8V	
E1	USB1_D_P	↔	T83	USB1_D_P		
D2	USB1_D_M	↔	T82	USB1_D_N		
L1	USB1_RX_P	←	T80	USB1_SSRX_P		
K2	USB1_RX_M	←	T79	USB1_SSRX_N		
H2	USB1_TX_P	→	T77	USB1_SSTX_P		AC-coupling: 100nF
G1	USB1_TX_M	→	T76	USB1_SSTX_N		AC-coupling: 100nF

Table 4-25 USB port 1: pin assignments

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
D6	USB2_VBUS	←	B63	USB2_VBUS	0 – 5.25V	
E5	USB2_ID	←	B62	USB2_ID	0 – 1.8V	
A7	USB2_D_P	↔	B72	USB2_D_P		
B8	USB2_D_M	↔	B71	USB2_D_N		
B2	USB2_RX_P	←	B69	USB2_SSRX_P		
A3	USB2_RX_M	←	B68	USB2_SSRX_N		
A5	USB2_TX_P	→	B66	USB2_SSTX_P		AC-coupling: 100nF
B6	USB2_TX_M	→	B65	USB2_SSTX_N		AC-coupling: 100nF

Table 4-26 USB port 2: pin assignments

Moreover, the module provides control signals. Each port can be individually enabled and has a separate overcurrent signal. The pins are shared with other functions.

More information can be obtained from Table 4-19 (USB2) and Table 4-24 (USB1).

USBx_PWRFAULT signals are high-active signals.
A logic high level signals the port is in an overcurrent situation.

4.10.8 UART

The MPX-LS1028A module provides a maximum of two UARTs without hardware handshake signals.

The following table shows the internal connections:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
AE7	UART1_SIN	←	B89	UART1_RXD	1.8V	PU: 10k
AB6	UART1_SOUT	→	B90	UART1_TXD	1.8V	
AD6	UART2_SIN	←	B86	UART2_RXD	1.8V	PU: 10k
AC5	UART2_SOUT	→	B87	UART2_TXD	1.8V	

Table 4-27 UART: pin assignments

The UART signals are partially shared with boot configuration pins of the CPU. Please refer to Table 4-9 Boot select pins: pin assignments for details.

The boot configuration pins must not be left floating on the carrier board!

Pin	Primary function	Secondary function	Configuration	GPIO
AE7	UART1_SIN	LPUART6_SIN		GPIO1_DAT10
AB6	UART1_SOUT	LPUART6_SOUT	**cfg_rcw_src1**	GPIO1_DAT11
AD6	UART2_SIN	LPUART6_CTS_B		GPIO1_DAT06
AC5	UART2_SOUT	LPUART6_RTS_B	**cfg_rcw_src0**	GPIO1_DAT07

Table 4-28 UART: pin multiplexing options

4.10.9 LPUART

The MPX-LS1028A module provides a maximum of four LPUARTs (low power UARTs) with hardware handshake signals.

LPUART2 and LPUART3 are not available.

None of the LPUARTs is a primary interface, which is why all of them share their pins with other interfaces:

- LPUART 1: see Table 4-19
- LPUART 4: see Table 4-19
- LPUART 5: see Table 4-32
- LPUART 6: see Table 4-28

4.10.10 eSDHC

The MPX-LS1028A module has two eSDHC interfaces with different capabilities.

8-bit data width is supported by eSDHC2 only.

	eSDHC1 (4 bit)	eSDHC2 (4 bit / 8 bit)
Supply Voltage	3,3V / 1,8V via SDHC_VSEL	1,8V
Card Detect Pin	✓	---
Write Protect Pin	✓	---
SD / SDIO	✓	---
eMMC	✓	✓

4.10.10.1 eSDHC1

The following table shows the internal connections:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
N7	SDHC1_CMD	↔	T26	SDHC1_CMD	EVDD_VCC (1,8V / 3,3V)	PU: 34k
M6	SDHC1_CLK	→	T28	SDHC1_CLK	EVDD_VCC (1,8V / 3,3V)	PU: 34k SR: 10R
N3	SDHC1_DAT0	↔	T24	SDHC1_DAT0	EVDD_VCC (1,8V / 3,3V)	PU: 34k
P4	SDHC1_DAT1	↔	T23	SDHC1_DAT1	EVDD_VCC (1,8V / 3,3V)	PU: 34k
N1	SDHC1_DAT2	↔	T22	SDHC1_DAT2	EVDD_VCC (1,8V / 3,3V)	PU: 34k
L5	SDHC1_DAT3	↔	T21	SDHC1_DAT3	EVDD_VCC (1,8V / 3,3V)	PU: 34k

Table 4-29 SDHC1 interface: pin assignments

Card detect and write protect pins are shared with other functions on the I2C2 primary functions pins. Please see Table 4-19 for details.

The SDHC1 is supplied with EVDD_VCC voltage which is software controlled by the SDHC_VSEL signal.

SDHC1 has several multiplexing options according to Table 4-30.

Nevertheless, MicroSys recommends providing an option for an SD card slot on the carrier board.

Pin	Primary function	Secondary function	Tertiary function	Quaternary function	GPIO
N7	SDHC1_CMD	SPI1_SOUT	SAI1_TX_BCLK	SAI1_RX_BCLK	GPIO1_DAT21
M6	SDHC1_CLK	SPI1_SCK	SAI2_TX_SYNC	SAI2_RX_SYNC	GPIO1_DAT16
N3	SDHC1_DAT0	SPI1_SIN	SAI2_TX_DATA	SAI2_RX_DATA	GPIO1_DAT17
P4	SDHC1_DAT1	SPI1_PCS2	SAI2_TX_BCLK	SAI2_RX_BCLK	GPIO1_DAT18
N1	SDHC1_DAT2	SPI1_PCS1	SAI1_TX_SYNC	SAI1_RX_SYNC	GPIO1_DAT19
L5	SDHC1_DAT3	SPI1_PCS0	SAI1_TX_DATA	SAI1_RX_DATA	GPIO1_DAT20

Table 4-30 SDHC1 pin multiplexing options

4.10.10.2 eSDHC2

The following table shows the internal connections for the 4-bit eSDHC2 interface (primary function):

CPU			Module Connector			
Ball	Signal		Pin	Signal	I/O Range	Signal conditioning
G21	SDHC2_CMD	↔	T9	SDHC2_CMD	1,8V	PU: 10k
F20	SDHC2_CLK	→	T11	SDHC2_CLK	1,8V	SR: 10R
B20	SDHC2_DS	→	T19	SDHC2_DS	1,8V	PD: 100k
N3	SDHC2_DAT0	↔	T17	SDHC2_DAT0	1,8V	PU: 49k9
P4	SDHC2_DAT1	↔	T16	SDHC2_DAT1	1,8V	PU: 49k9
N1	SDHC2_DAT2	↔	T15	SDHC2_DAT2	1,8V	PU: 49k9
L5	SDHC2_DAT3	↔	T14	SDHC2_DAT3	1,8V	PU: 49k9

Table 4-31 SDHC2 interface: pin assignments

Data bits 4 to 7 are shared with I2C7 and I2C8 according to Table 4-19.

Pin	Primary function	Secondary function	Tertiary function	Quaternary function	GPIO
G21	SDHC2_CMD	SPI2_SOUT		XSPI1_B_CS1_B	GPIO2_DAT19
F20	SDHC2_CLK	SPI2_SCK		XSPI1_B_SCK	GPIO2_DAT09
B20	SDHC2_DS	SPI2_PCS3		XSPI1_B_DQS	GPIO2_DAT10
N3	SDHC2_DAT0	SPI2_SIN	LPUART5_RTS_B	XSPI1_B_DATA0	GPIO2_DAT11
P4	SDHC2_DAT1	SPI2_PCS2	LPUART5_CTS_B	XSPI1_B_DATA1	GPIO2_DAT12
N1	SDHC2_DAT2	SPI2_PCS1	LPUART5_SIN	XSPI1_B_DATA2	GPIO2_DAT13
L5	SDHC2_DAT3	SPI2_PCS0	LPUART5_SOUT	XSPI1_B_DATA3	GPIO2_DAT14

Table 4-32 SDHC2 pin multiplexing options

4.10.11 RGMII

The LS1028A CPU contains an Ethernet controller with two ports and a TSN Switch with four MACs (MAC 0,1,2,3).

- Port 1 is an RGMII port with a dedicated MAC that does not support TSN.
- Port 0 can be used for SGMII / USXGMII. It does not support TSN either.
- MAC0, MAC1, MAC2, MAC3 support TSN.

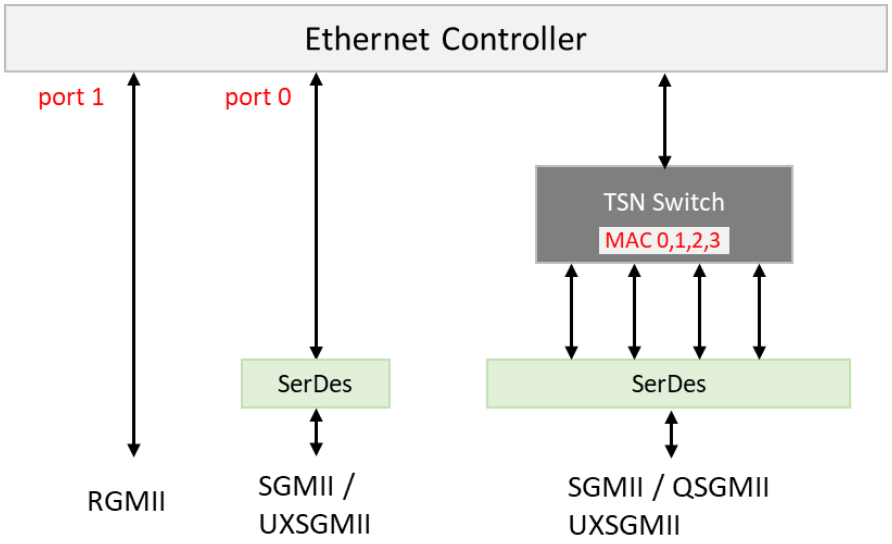

Table 4-33 Ethernet Controller / TSN Switch

The following table shows the internal connections of RGMII1:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
AD2	EC1_RX_CLK	←	B53	EC1_RX_CLK	1,8V	
AH2	EC1_RX_DV	←	B52	EC1_RX_DV	1,8V	
AK2	EC1_GTX_CLK125	←	B60	EC1_GTX_CLK 125	1,8V	
AG1	EC1_RXD0	←	B58	EC1_RXD0	1,8V	
AF2	EC1_RXD1	←	B57	EC1_RXD1	1,8V	
AE3	EC1_RXD2	←	B56	EC1_RXD2	1,8V	
AE1	EC1_RXD3	←	B55	EC1_RXD3	1,8V	
AH4	EC1_GTX_CLK	→	T71	EC1_GTX_CLK	1,8V	SR: 10R
AF6	EC1_TXD0	→	T69	EC1_TXD0	1,8V	SR: 10R

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
AF4	EC1_TXD1	→	T68	EC1_TXD1	1,8V	SR: 10R
AD4	EC1_TXD2	→	T67	EC1_TXD2	1,8V	SR: 10R
AG5	EC1_TXD3	→	T66	EC1_TXD3	1,8V	SR: 10R
AJ3	EC1_TX_EN	→	T64	EC1_TX_EN	1,8V	SR: 10R
AK4	EMI1_MDIO	↔	T60	EMI1_MDIO	1,8V	PU: 10k
AK6	EMI1_MDC	→	T62	EMI1_MDC	1,8V	PD: 4k7

Table 4-34 RGMII1: pin assignments

The RGMII interface has different multiplexing options. The most common functions are displayed in the following table. Please refer to the NXP datasheet for all possible combinations and potential group limitations:

Pin	**Primary function**	**Secondary function**	**Tertiary function**	**Quaternary function**	**GPIO**
AD2	EC1_RX_CLK	EC1_1588_CLK_IN	SAI3_TX_SYNC	SAI3_RX_SYNC	GPIO3_DAT01
AH2	EC1_RX_DV	EC1_1588_TRIG_IN	SAI6_TX_SYNC	SAI6_RX_SYNC	GPIO3_DAT00
AK2	EC1_GTX_CLK125	EC1_1722_DAT0			GPIO3_DAT06
AG1	EC1_RXD0		SAI6_TX_BCLK	SAI6_RX_BCLK	GPIO3_DAT02
AF2	EC1_RXD1		SAI3_TX_BCLK	SAI3_RX_BCLK	GPIO3_DAT03
AE3	EC1_RXD2		SAI4_TX_BCLK	SAI4_RX_BCLK	GPIO3_DAT04
AE1	EC1_RXD3	EC1_1722_DAT1	SAI5_TX_BCLK	SAI5_RX_BCLK	GPIO3_DAT05
AH4	EC1_GTX_CLK	SWITCH_1588_DAT0	SAI4_TX_SYNC	SAI4_RX_SYNC	GPIO3_DAT07
AF6	EC1_TXD0	EC1_1588_PULSE_OUT2	SAI6_TX_DATA	SAI6_RX_DATA	GPIO3_DAT09
AF4	EC1_TXD1		SAI3_TX_DATA	SAI3_RX_DATA	GPIO3_DAT10
AD4	EC1_TXD2		SAI4_TX_DATA	SAI4_RX_DATA	GPIO3_DAT11
AG5	EC1_TXD3		SAI5_TX_DATA	SAI5_RX_DATA	GPIO3_DAT12
AJ3	EC1_TX_EN	SWITCH_1588_DAT1	SAI5_TX_SYNC	SAI5_RX_SYNC	GPIO3_DAT08
AK4	EMI1_MDIO				---
AK6	EMI1_MDC				---

Table 4-35 RGMII pin multiplexing options

4.10.12 SerDes

The MPX-LS1028A module offers four SerDes lanes. These lanes can be configured according to the LS1028A reference manual provided by manufacturer NXP.

SerDes mapping is configurable via RCW.
For more information on possible configurations please contact MicroSys.

The four SerDes lanes can support different protocols. Some of the protocols are available on specific lanes only. The following table shows the distribution across those lanes. Not all combinations are valid:

Lane on module connector:	Lane 0	Lane 1	Lane 2	Lane 3
PCIe x1	✓		✓	✓
PCIe x2	✓		✓	
PCIe x4	✓			
SGMII	✓	✓	✓	
SGMII (TSN support)	✓	✓	✓	✓
10G SXGMII	✓			
QSGMII		✓		
10G QXGMII		✓		
SATA				✓

Table 4-36 SerDes interface: lane distribution

Note that the 10G SXGMII supports a maximum speed of 2.5Gbps.

The MPX-LS1028A module provides one clock pair to the carrier board which is displayed in Table 4-37. The frequency on those pins is 100MHz.

PI6C557			Module Connector			
Pin	Signal		Pin	Signal	I/O Range	Signal conditioning
10	CLK1#	→	T30	SD_CLK100_N	HCSL	SR: 33R PD: 49R9
11	CLK1	→	T31	SD_CLK100_P	HCSL	SR: 33R PD: 49R9

Table 4-37 SerDes interface: external clock

The following table shows the internal connections of the data pairs:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
AJ11	SD1_RX0_N	←	T57	SD1_RX0_N		
AK10	SD1_RX0_P	←	T58	SD1_RX0_P		
AG13	SD1_TX0_N	→	T54	SD1_TX0_N		AC-coupling: 220nF
AF12	SD1_TX0_P	→	T55	SD1_TX0_P		AC-coupling: 220nF
AJ13	SD1_RX1_N	←	T51	SD1_RX1_N		
AK12	SD1_RX1_P	←	T52	SD1_RX1_P		
AG15	SD1_TX1_N	→	T48	SD1_TX1_N		AC-coupling: 220nF
AF14	SD1_TX1_P	→	T49	SD1_TX1_P		AC-coupling: 220nF
AJ15	SD1_RX2_N	←	T45	SD1_RX2_N		
AK14	SD1_RX2_P	←	T46	SD1_RX2_P		
AG17	SD1_TX2_N	→	T42	SD1_TX2_N		AC-coupling: 220nF
AF16	SD1_TX2_P	→	T43	SD1_TX2_P		AC-coupling: 220nF
AJ17	SD1_RX3_N	←	T39	SD1_RX3_N		
AK16	SD1_RX3_P	←	T40	SD1_RX3_P		
AG19	SD1_TX3_N	→	T36	SD1_TX3_N		AC-coupling: 220nF
AF18	SD1_TX3_P	→	T37	SD1_TX3_P		AC-coupling: 220nF

Table 4-38 SerDes interface: pin assignments

The MPX-LS1028A module can also be configured as a PCIe Endpoint. In that case it is mandatory to provide an external 100MHz clock for REF_CLK1:

CPU			Module Connector			
Ball	**Signal**		**Pin**	**Signal**	**I/O Range**	**Signal conditioning**
AG9	SD1_REF_CLK1_N	←	T33	SD_CLKIN_N	HCSL	PD: 49R9
AF10	SD1_REF_CLK1_P	←	T34	SD_CLKIN_P	HCSL	PD: 49R9

Table 4-39 SerDes interface: clock for PCIe Endpoint

5 Mechanical Description

5.1 Edge Finger

The MPX-LS1028A module is connected with the carrier board via a 230-pin connector with 0.5mm pitch. Note that the mating connector on the carrier needs to accept edge cards with a thickness of 1.2mm.

The pin layout is symmetric, so the pins are equally distributed among top and bottom side edge fingers, 115 pins each.

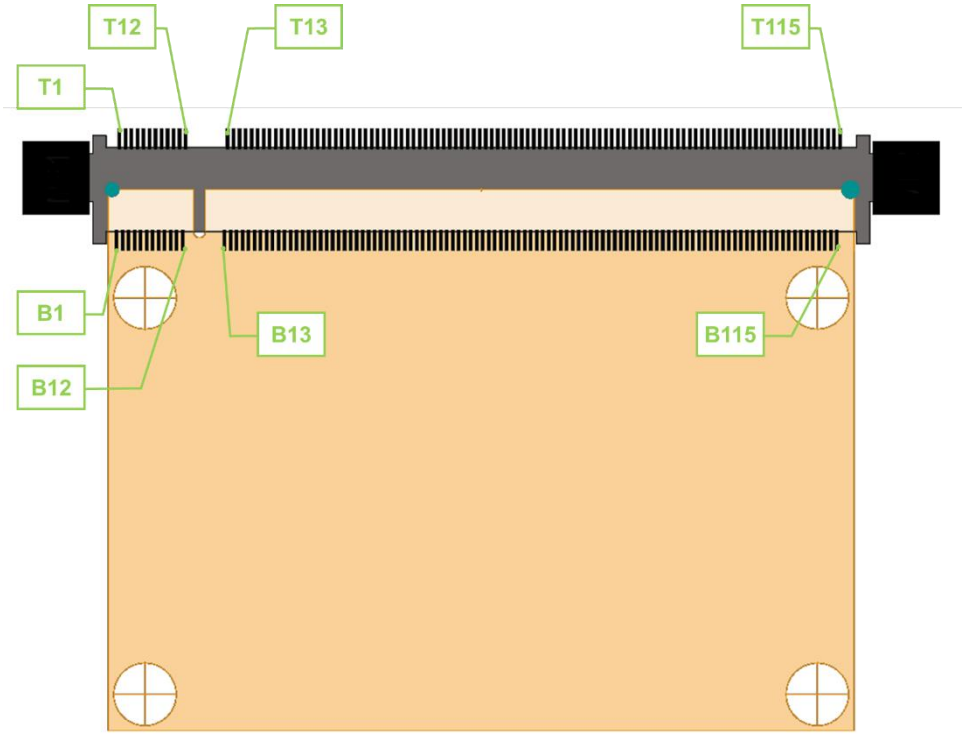

Figure 5-1 Plugged module (pin numbering scheme)

The recommended connector for the MPX-LS1028A is:

Manufacturer	Type	Board-to-board height	Total height
Iriso	IMSA-18010S-230A-GN1	5mm	7.75mm

Table 5-1 Connector Type: ordering information

5.2 Board Outline

NOTE

For 3D data files please contact MicroSys.

The following drawing shows the mechanical outline (62.11mm x 45mm) of the MPX-LS1028A module:

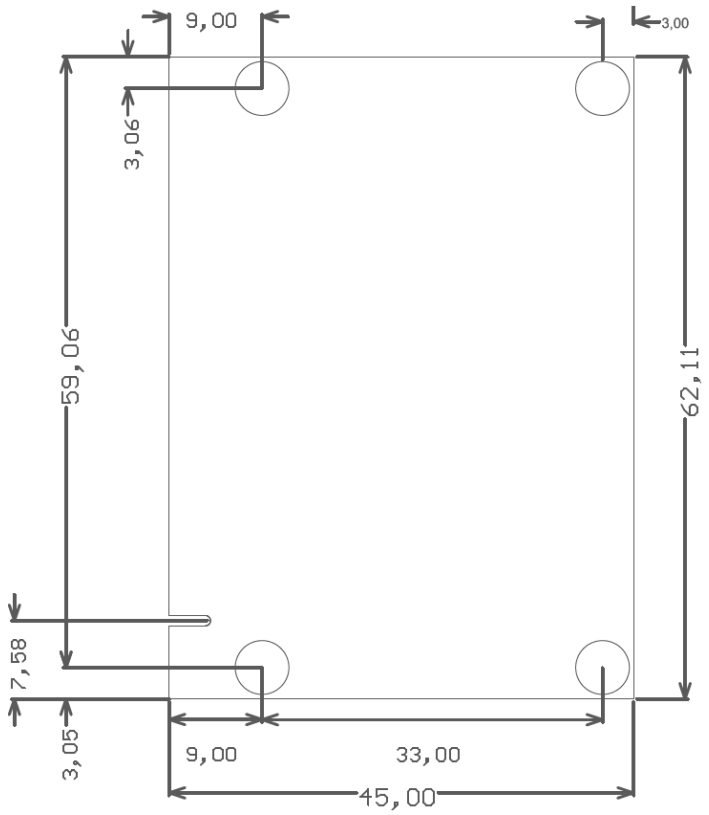

Figure 5-2 Module outline (62.11mm x 45.00mm)

The mounting holes can be used with M2.5 screws. Dimensions are designed as follows:

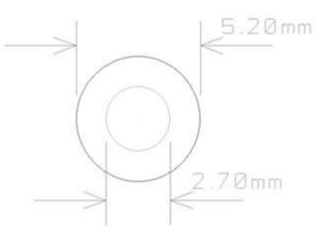

Figure 5-3 Mounting holes: dimensions

5.3 Height

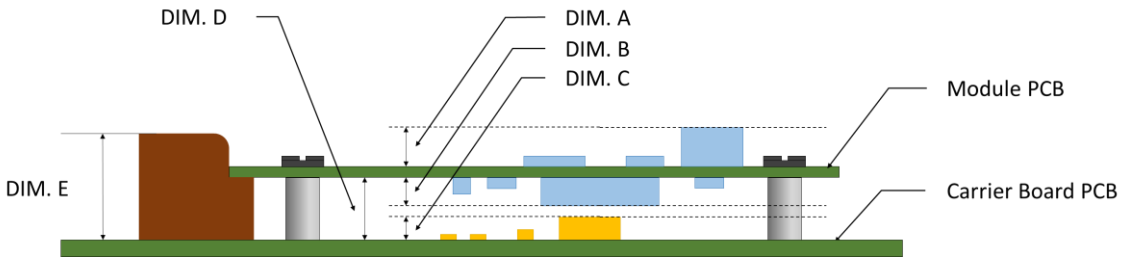

Figure 5-4 Construction height for parts

	Definition	Value
DIM. A	Module top side parts	3.00 mm
DIM. B	Module bottom side parts	1.20 mm
DIM. C	Carrier board parts under the module	DIM. D minus DIM. B
DIM. D	Board-to-board height	Depending on connector type
DIM. E	Connector product height	Depending on connector type

Table 5-2 Construction height overview

5.4 Thickness

PCB thickness of the MPX-LS1028A module is 1.2mm ± 10%.

5.5 Component Layout - Top Side

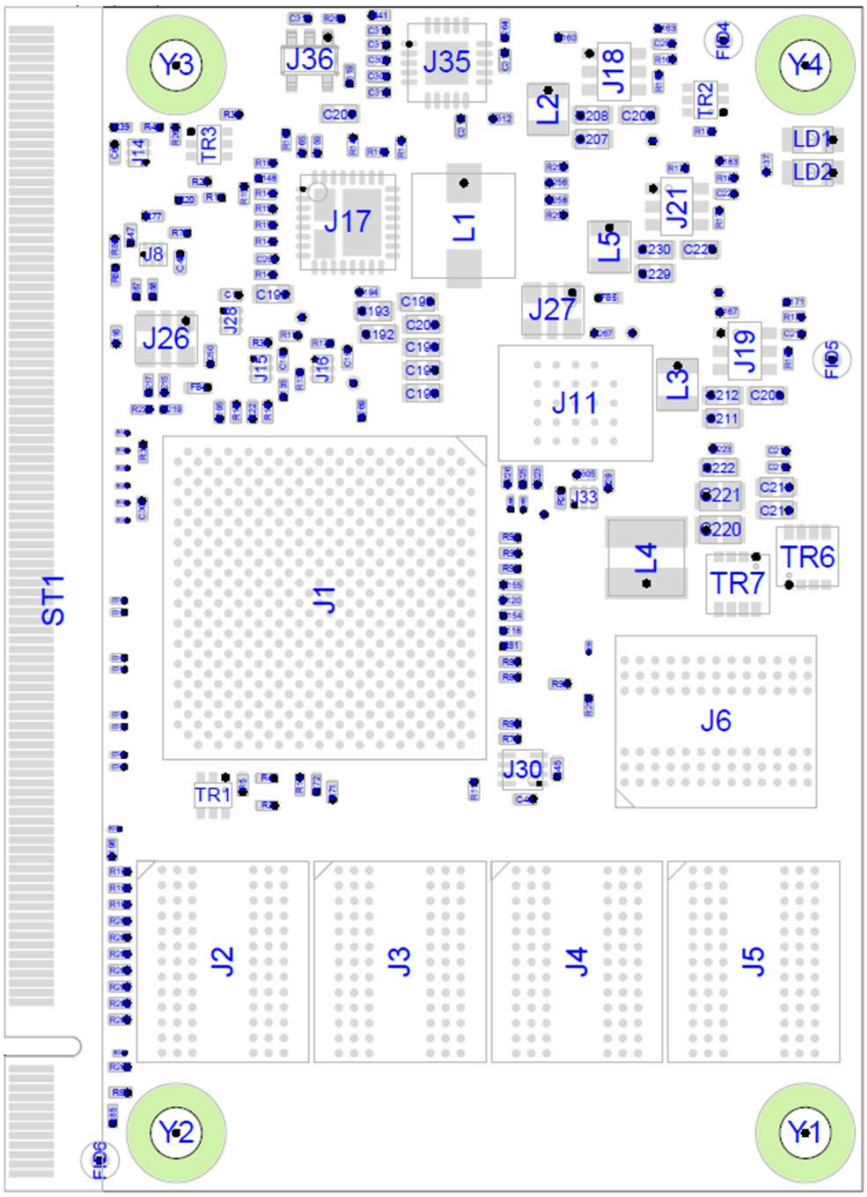

Figure 5-5 Top Components

Part Reference	Manufacturer	Type	Function
ST1	---	Edge Finger	connection to carrier board
J1	NXP	LS1028A	CPU
J2/J3/J4/J5/6	Micron	DDR4	memory
J11	Micron	QSPI Serial NOR Flash	memory
J30	Texas Instruments	TMP451	temperature sensor

Table 5-3 Top side components

5.6 Component Layout - Bottom Side

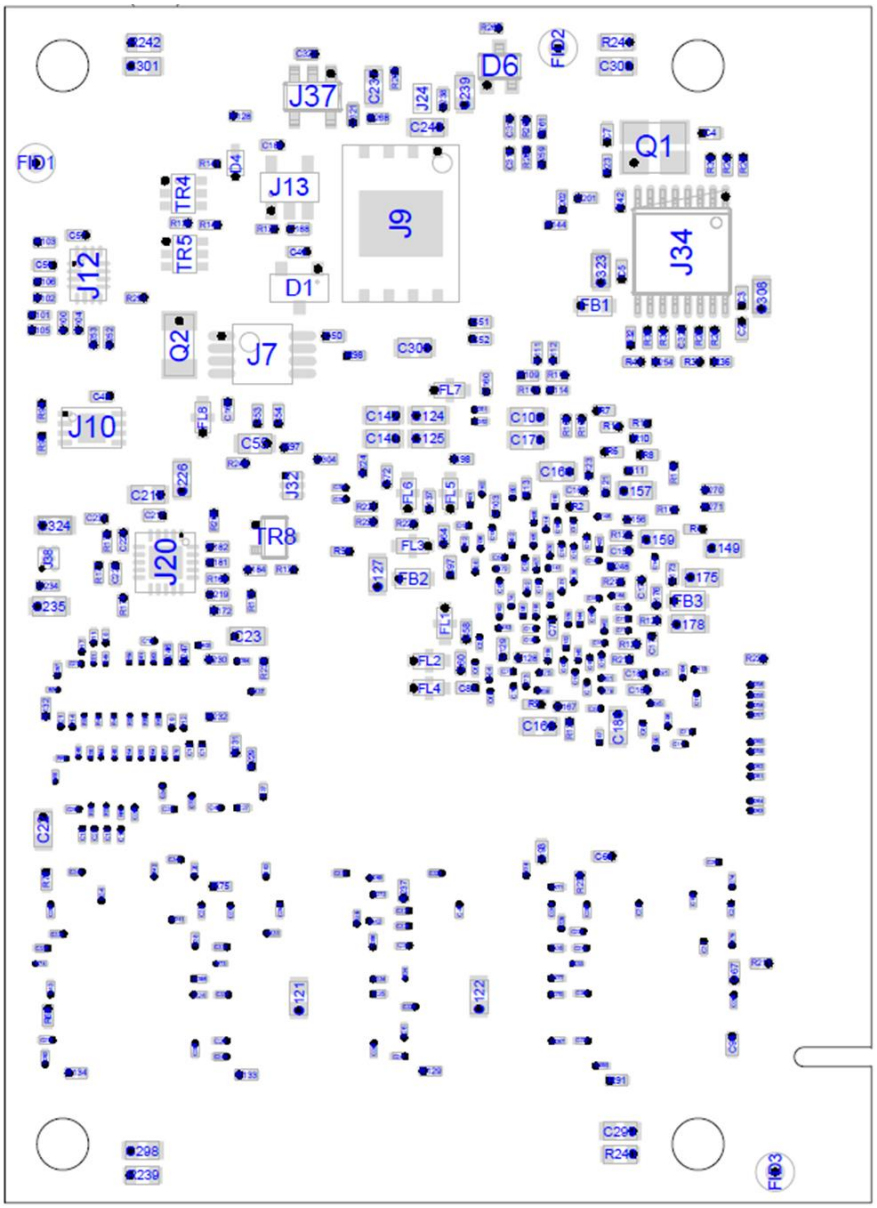

Figure 5-6 Bottom Components

Part Reference	Manufacturer	Type	Function
J7	NXP	PCF85063	RTC
J9	Toshiba	QSPI Serial NAND Flash	memory
J10	Rohm	BR24G	EEPROM
J12	On Semicondutor	FXL6408	GPIO Expander
J34	Diodes	PI6C557	clock generator

Table 5-4 Bottom side components

6 Software

6.1 U-Boot

The MPX-LS1028A uses U-Boot as the standard boot loader, which is always integrated in the boards QSPI Flash memories on delivery.

Additionally, there's a U-Boot version available to be placed on an SD card if that interface is implemented on the carrier board.

More information on selecting the boot source can be found in chapter 4.5.

The U-Boot carries out the following tasks:

- Pin configuration
- CPU configuration
- Clock configuration
- DDR4 configuration and timing

6.2 Operating System

MicroSys Electronics GmbH offers Linux and Microware OS-9 RTOS support for the module.

Other Operating Systems are available on request only.

7 Safety Requirements And Protective Regulations

7.1 EMC

The System on Module MPX-LS1028A is designed according to the requirements of electromagnetic compatibility. Nevertheless, there are several factors which in the target system may require measures against interference.

Active components, especially CPUs of the latest generation do not only operate with high frequencies but also drive very fast signal rise times.

At least the following measures shall be applied:

- Provide sufficient block capacitors in your supply voltages
- Keep short all clock lines in order to prevent interference with other signals
- Shield clock lines with ground planes or keep as much distance as possible to other signals
- Provide filtering for all external signals
- Provide an EMI proof housing for your electronics

7.2 ESD

For technical reasons there is no ESD protection on the MPX-LS1028A. Please provide sufficient protection on the baseboard and/or system level.

7.3 Reliability

The SOM MPX-LS1028A is available for operation in extended temperature range.

Please note that steady high temperature operation reduces lifetime of all electronic components. Make sure that no component on the module ever exceeds its maximum specified temperature during operation or storage. A reasonable cooling concept can dramatically increase the lifetime of your electronics.

The MPX-LS1028A is designed to withstand a high level of vibration and shock due to its light weight and no overhanging components on the module. If desired, MicroSys Electronics GmbH can support you with your shock and vibration concept. Please ask your sales representative or send an email inquiry to support@microsys.de.

Relevant components on the module are chosen with values for a high level of derating.

7.4 Climatic conditions

The relative humidity during operation or storage of the module may not exceed 10% to 90%, non-condensing.

7.5 RoHS

All components of the MPX-LS1028A are RoHS compliant, also a RoHS compliant soldering process is used for manufacturing.

8 General notes

Customers responsibility for chip errata.

It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of.

The manufacturer’s advice should be followed.

If desired, MicroSys Electronics GmbH can support you with your lifecycle management regarding chip errata. Please ask your sales representative or send an email inquiry to support@microsys.de.

9 Appendix

9.1 Acronyms

These acronyms are being used within the document; note that this list does not claim to be complete or exhaustive:

CAN ..... *Controller Area Network*
ESD ..... *Electrostatic Discharge*
eSDHC ..... *Enhanced Secured Digital Host Controller*
GPL ..... *General Public License*
I²C ..... *Inter-Integrated Circuit*
LED ..... *Light Emitting Diode*
MCU ..... *Microcontroller Unit*
PU ..... *Pull-Up Resistor*
QSPI ..... *Quad Serial Peripheral Interface*
RGMII ..... *Reduced Gigabit Media Independent Interface*
RTC ..... *Real-Time clock*
SAI ..... *Synchronous Audio Interface*
SATA ..... *Serial Advanced Technology Attachment*
SDHC ..... *Secure Digital High Capacity*
SerDes ..... *Serializer Deserializer*
SPI ..... *Serial Peripheral Interface*
USB ..... *Universal Serial Bus*

9.2 Table of Figures

9.3 Table of Tables

10 History

Date	Version	Change Description
2020-03-26	1.0	Initial Release Version

Table 10-1 Document history