Product category

miriac® MPX-LS1046A
miriac® MPX-LS1043A
miriac® MPX-LS1088A

Question

We are trying to bring up the SPI interface. Enabling SPI in the device tree results in the following error messages:

[3.155114] fsl-dspi 2100000.dspi: can‘t get bus-num

[3.160085] fsl-dspi: probe of 2100000.dspi failed with error -22

We have verified that RCW[SPI_EXT]=000 and RCW[SPI_BASE]=00.

What are we missing?

Answer

Basically you need an entry in your Device Tree so that the /dev/spidevB.C character device nodes are created and then you need to modify $KRN_SRC/drivers/spi/spidev.c.

Here is an example of a device tree entry on another of our carriers where we have two SJA1105 switches which can be controlled via SPI:

```
&dspi {
            num-cs = <2>;
            bus-num = <0>;
            status = „okay“;

            spidev@0×01 {
           compatible = „fsl,sja1105“;
      spi-max-frequency = <17000000>;
      spi-cpha;
      reg = <1>;
      fsl,spi-sck-cs-delay = <25>;
      fsl,spi-cs-sck-delay = <25>;
   };

            spidev@0×02 {
           compatible = „fsl,sja1105“;
      spi-max-frequency = <17000000>;
      spi-cpha;
      reg = <2>;
      fsl,spi-sck-cs-delay = <25>;
      fsl,spi-cs-sck-delay = <25>;
   };
};
```

Answer

In the datasheet of the SPI device you are connecting, you need to determine which delay is required and which clocking mode (rising or falling edge). This is the spi-cpha entry.

Also the compatible string must match that listed in $KRN_SRC/drivers/spi/spidev.c which basically means that you have to enter it in the spidev.c file. For example:

{ .compatible = “fsl,sja1105” },

Further info can be found here:

https://www.kernel.org/doc/Documentation/spi/spi-summary

What are these four SPI „clock modes“?

The four modes combine two mode bits:

- CPOL indicates the initial clock polarity. CPOL=0 means the clock starts low, so the first (leading) edge is rising, and the second (trailing) edge is falling. CPOL=1 means the clock starts high, so the first (leading) edge is falling.

- CPHA indicates the clock phase used to sample data; CPHA=0 says sample on the leading edge, CPHA=1 means the trailing edge.

Since the signal needs to stablize before it‘s sampled, CPHA=0 implies that its data is written half a clock before the first clock edge. The chipselect may have made it become available.

Chip specs won‘t always say „uses SPI mode X“ in as many words, but their timing diagrams will make the CPOL and CPHA modes clear.

In the SPI mode number, CPOL is the high order bit and CPHA is the low order bit. So when a chip‘s timing diagram shows the clock starting low (CPOL=0) and data stabilized for sampling during the trailing clock edge (CPHA=1), that‘s SPI mode 1.

Note that the clock mode is relevant as soon as the chipselect goes active. So the master must set the clock to inactive before selecting a slave, and the slave can tell the chosen polarity by sampling the clock level when its select line goes active. That‘s why many devices support for example both modes 0 and 3: they don‘t care about polarity, and always clock data in/out on rising clock edges.

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