

miriac MPX-S32G399A

User Manual (HW Revision 6)

V6.1

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1 General Notes

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1.5 Symbols, Conventions and Abbreviations

1.5.1 Symbols

Throughout this document, the following symbols will be used:



Information marked with this symbol **MUST** be obeyed to avoid the risk of severe injury, health danger, or major destruction of the unit and its environment



Information marked with this symbol **MUST** be obeyed to avoid the risk of possible injury, permanent damage or malfunction of the unit.



Information marked with this symbol gives important hints upon details of this manual, or in order to get the best use out of the product and its features.

Table 1 Symbols

1.5.2 Conventions

| Symbol | Explanation |
|--------------|--|
| # / xxx_B | denotes a low active signal |
| ← | denotes the signal flow in the direction shown |
| → | denotes the signal flow in the direction shown |
| ↔ | denotes the signal flow in both directions |
| → | denotes the signal flow in the direction shown with additional logic / additional ICs in the signal path |
| I/O / INOUT | denotes a bidirectional pin |
| Input | denotes an input pin |
| Output | denotes an output pin |
| matched | denotes the according signal to be routed impedance controlled and length matched |
| Pin 1 | refers to the numeric pin of a component package |
| Pin a1 | refers to the array position of a pin within a component package |
| xxx- / xxx_N | denotes the negative signal of a differential pair |
| xxx+ / xxx_P | denotes the positive signal of a differential pair |
| xxx | denotes an optional not mounted or fitted part |

Table 2 Conventions

1.6 Safety and Handling Precautions



DO NOT exceed the rated maximum values for the power supply! This may result in severe permanent damage to the unit, as well as possible serious injury.

ALWAYS keep the unit dry, clean, and free of foreign objects. Otherwise, irreparable damage may occur.



Parts of the unit may become hot during operation. Take care not to touch any parts of the circuitry during operation to avoid burns and operate the unit in a well-ventilated location. Provide an appropriate cooling solution as required.



Electrostatic discharge (ESD) can damage the unit. Always take the necessary ESD precautions.

Many pins on the module connector are directly connected to the SOC or other ESD sensitive devices. Make or break ANY connection **ONLY** while the unit is switched OFF.

Otherwise, permanent damage to the unit may occur, which is not covered by warranty.



There is no separate SHIELD connection.

The module's mounting holes are not connected to GND. Take this into account when handling and mounting the unit.

Table 3 Safety and Handling Precautions

2 Short Description

The miriac MPX-S32G399A is a member of the MPX module family based on NXP's S32G399A network processor (SoC).

MicroSys Electronics GmbH offers a Development Kit which uses the key features of the module. The customer can:

- ...test the operation of the MPX-S32G399A module
- ...evaluate the main interfaces of the S32G399A SoC
- ...test the provided software
- ...start developing

3 System Description

3.1 Block Diagram

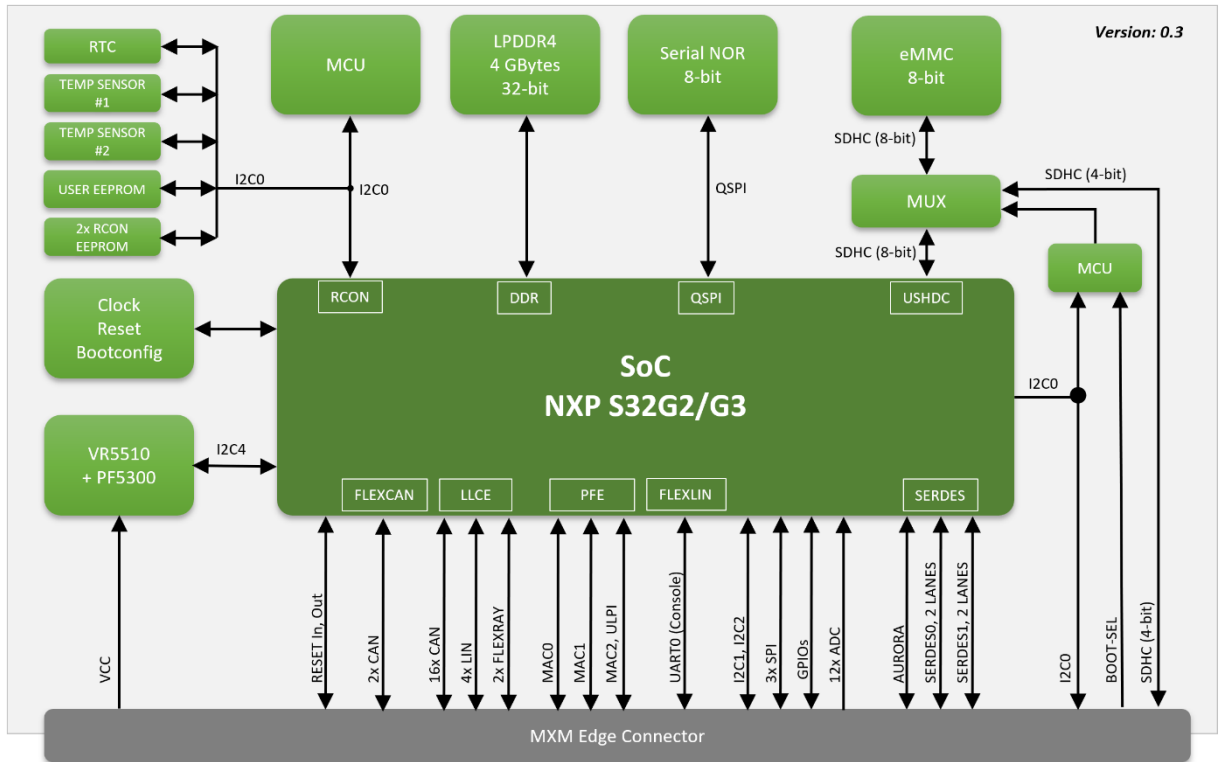


Figure 3-1 Block Diagram

3.2 System Components

- S32G399A SoC (8x Arm Cortex-A53 plus 4x Cortex-M7 lockstep cores)
- 4GB LPDDR4 SDRAM
- Serial NOR flash as boot or storage device
- eMMC flash as boot or storage device
- Clock generators for SOC and interface clocks
- I²C EEPROM
- I²C temperature sensor
- I²C RTC
- Voltage regulators for onboard voltages
- Supervisor MCU monitoring temperatures and supplies

3.3 Ordering Information

Ordering information can be found on the following website

[miriac MPX-S32G399A](https://www.miriac.com/MPX-S32G399A)

or contact your local sales representative.

3.4 Power Consumption

The MPX-S32G399A is supplied by a single input power rail.

The typical power consumption values for the module over junction temperature are determined on a CRX-S32G carrier running Linux based on BSP 36, input voltage 12V with 4 times RJ45 1G Ethernet connected as well as console over USB.

Linux Stress: stressapptest (<https://github.com/stressapptest/stressapptest>) (start parameters: -W -s 60, all cores)

Linux Idle: command prompt

| T _i [°C] from internal probe | Power dissipation idle [W] | Power dissipation stress [W] |
|---|----------------------------|------------------------------|
| -35 | 4,2 | 5,7 |
| -15 | 4,1 | 5,8 |
| 0 | 4,2 | 5,8 |
| 25 | 4,2 | 5,9 |
| 50 | 4,5 | 6,2 |
| 70 | 5,2 | 6,6 |

Table 4 Typical power consumption running module with Linux

3.5 Cooling

In chapter 3.4 the typical power consumption of the MPX-S32G399A module was specified. With this information a cooling method needs to be designed which considers the final use case. If desired, MicroSys Electronics GmbH can support you with your cooling concept. Please ask your sales representative or send an email inquiry to support@microsys.de.



Do not run the module without a heatsink or appropriate cooling concept

4 Technical Description

4.1 Pinouts



The signal direction is from the module's view. For example, PCIE0_TX0_N, pin T90, is an output from the module and an input to peripheral devices on the carrier.

The following table gives an overview of the 314 pins of the module's edge finger. For a detailed connector description see chapter 5.1. The pins will be described in chapter 4.10 and the following sections.

The signal names in the following two tables do not show all available options for each pin. Pin multiplexing can only be implemented in combination with the vendor's datasheet.

4.1.1 Module Connector – Top Pins

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|-----|--------------------------------|------------------------|-------|
| T1 | GND | --- | --- |
| T2 | SD_CLK | --- | ✓ |
| T3 | GND | --- | --- |
| T4 | SD_CMD | --- | ✓ |
| T5 | GND | --- | --- |
| T6 | SD_D0 | --- | ✓ |
| T7 | SD_D1 | --- | ✓ |
| T8 | SD_D2 | --- | ✓ |
| T9 | SD_D3 | --- | ✓ |
| TK1 | VCC_SDHC_1V8/3V3 | --- | --- |
| TK2 | PMIC_FCCU1_OUT | --- | --- |
| T10 | GND | --- | --- |
| T11 | GND | --- | --- |
| T12 | RGMII2_MDC/DSP10_CS7 | ✓ | ✓ |
| T13 | RGMII2_MDIO | ✓ | ✓ |
| T14 | GND | --- | --- |
| T15 | RGMII2_RXD3/USB_D7 | ✓ | ✓ |
| T16 | RGMII2_RXD2/USB_D6 | ✓ | ✓ |
| T17 | RGMII2_RXD1/USB_D5 | ✓ | ✓ |
| T18 | RGMII2_RXD0/USB_D4 | ✓ | ✓ |
| T19 | GND | --- | --- |
| T20 | RGMII2_RXDV/USB_D3 | ✓ | ✓ |

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|-----|--------------------------------|------------------------|-------|
| T21 | RGMII2_RX_CLK/USB_D2 | ✓ | ✓ |
| T22 | GND | --- | --- |
| T23 | RGMII2_TXD3/USB_D1 | ✓ | ✓ |
| T24 | RGMII2_TXD2/USB_D0 | ✓ | ✓ |
| T25 | RGMII2_TXD1/USB_NXT | ✓ | ✓ |
| T26 | RGMII2_TXD0/USB_STP | ✓ | ✓ |
| T27 | GND | --- | --- |
| T28 | RGMII2_TX_EN/USB_DIR | ✓ | ✓ |
| T29 | RGMII2_TX_CLK/USB_CLK | ✓ | ✓ |
| T30 | GND | --- | --- |
| T31 | RGMII1_MDC | ✓ | ✓ |
| T32 | RGMII1_MDIO | ✓ | ✓ |
| T33 | GND | --- | --- |
| T34 | RGMII1_RXD3 | ✓ | ✓ |
| T35 | RGMII1_RXD2 | ✓ | ✓ |
| T36 | RGMII1_RXD1 | ✓ | ✓ |
| T37 | RGMII1_RXD0 | ✓ | ✓ |
| T38 | GND | --- | --- |
| T39 | RGMII1_RXDV | ✓ | ✓ |
| T40 | RGMII1_RX_CLK | ✓ | ✓ |
| T41 | GND | --- | --- |
| T42 | RGMII1_TXD3 | ✓ | ✓ |
| T43 | RGMII1_TXD2 | ✓ | ✓ |
| T44 | RGMII1_TXD1 | ✓ | ✓ |
| T45 | RGMII1_TXD0 | ✓ | ✓ |
| T46 | GND | --- | --- |
| T47 | RGMII1_TX_EN | ✓ | ✓ |
| T48 | RGMII1_TX_CLK | ✓ | ✓ |
| T49 | GND | --- | --- |
| T50 | RGMII0_MDC | ✓ | ✓ |
| T51 | RGMII0_MDIO | ✓ | ✓ |
| T52 | GND | --- | --- |
| T53 | RGMII0_RXD3 | ✓ | ✓ |
| T54 | RGMII0_RXD2 | ✓ | ✓ |
| T55 | RGMII0_RXD1 | ✓ | ✓ |
| T56 | RGMII0_RXD0 | ✓ | ✓ |

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|-----|--------------------------------|------------------------|-------|
| T57 | GND | --- | --- |
| T58 | RGMII0_RXDV | ✓ | ✓ |
| T59 | RGMII0_RX_CLK | ✓ | ✓ |
| T60 | GND | --- | --- |
| T61 | RGMII0_TXD3 | ✓ | ✓ |
| T62 | RGMII0_TXD2 | ✓ | ✓ |
| T63 | RGMII0_TXD1 | ✓ | ✓ |
| T64 | RGMII0_TXD0 | ✓ | ✓ |
| T65 | GND | --- | --- |
| T66 | RGMII0_TX_EN | ✓ | ✓ |
| T67 | RGMII0_TX_CLK | ✓ | ✓ |
| T68 | GND | --- | --- |
| T69 | PCIE1_RX0_N | --- | --- |
| T70 | PCIE1_RX0_P | --- | --- |
| T71 | GND | --- | --- |
| T72 | PCIE1_RX1_N | --- | --- |
| T73 | PCIE1_RX1_P | --- | --- |
| T74 | GND | --- | --- |
| T75 | PCIE0_RX0_N | --- | --- |
| T76 | PCIE0_RX0_P | --- | --- |
| T77 | GND | --- | --- |
| T78 | PCIE0_RX1_N | --- | --- |
| T79 | PCIE0_RX1_P | --- | --- |
| T80 | GND | --- | --- |
| T81 | MCU_SWD_CLK/KILL | --- | --- |
| T82 | MCU_SWD_DIO/SAFEIO | --- | --- |
| T83 | GND | --- | --- |
| T84 | PCIE1_TX0_N | --- | --- |
| T85 | PCIE1_TX0_P | --- | --- |
| T86 | GND | --- | --- |
| T87 | PCIE1_TX1_N | --- | --- |
| T88 | PCIE1_TX1_P | --- | --- |
| T89 | GND | --- | --- |
| T90 | PCIE0_TX0_N | --- | --- |
| T91 | PCIE0_TX0_P | --- | --- |
| T92 | GND | --- | --- |

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|------|--------------------------------|------------------------|-------|
| T93 | PCIE0_TX1_N | --- | --- |
| T94 | PCIE0_TX1_P | --- | --- |
| T95 | GND | --- | --- |
| T96 | AUR_CLK_N | --- | --- |
| T97 | AUR_CLK_P | --- | --- |
| T98 | GND | --- | --- |
| T99 | AUR_TX2_N | --- | --- |
| T100 | AUR_TX2_P | --- | --- |
| T101 | GND | --- | --- |
| T102 | AUR_TX0_N | --- | --- |
| T103 | AUR_TX0_P | --- | --- |
| T104 | GND | --- | --- |
| T105 | AUR_TX1_N | --- | --- |
| T106 | AUR_TX1_P | --- | --- |
| T107 | GND | --- | --- |
| T108 | AUR_TX3_N | --- | --- |
| T109 | AUR_TX3_P | --- | --- |
| T110 | GND | --- | --- |
| T111 | PB02 | ✓ | ✓ |
| T112 | PB07 | ✓ | ✓ |
| T113 | PB08 | ✓ | ✓ |
| T114 | PB15 | ✓ | ✓ |
| T115 | PC00 | ✓ | ✓ |
| T116 | GND | --- | --- |
| T117 | +VREF1 | --- | --- |
| T118 | +VREF2 | --- | --- |
| T119 | +VREF3 | --- | --- |
| T120 | +VREF4 | --- | --- |
| T121 | GND | --- | --- |
| T122 | PCIE0_CLKIN_N | --- | --- |
| T123 | PCIE0_CLKIN_P | --- | --- |
| T124 | GND | --- | --- |
| T125 | NMI | --- | --- |
| T126 | PMIC_RST# | --- | --- |
| T127 | RSTIN# | --- | --- |
| T128 | RST# | --- | --- |

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|------|--------------------------------|------------------------|-------|
| T129 | GND | --- | --- |
| T130 | SEL_CLK_RC/EP# | --- | --- |
| T131 | RCW_SEL# | --- | --- |
| T132 | Reserved, do not connect | --- | --- |
| T133 | VCC_RTC | --- | --- |
| T134 | +3V3_EXT | --- | --- |
| T135 | I2C_SCL_PROG | --- | --- |
| T136 | I2C_SDA_PROG | --- | --- |
| T137 | GND | --- | --- |
| T138 | GND | --- | --- |
| T139 | GND | --- | --- |
| T140 | GND | --- | --- |
| T141 | GND | --- | --- |
| T142 | GND | --- | --- |
| T143 | GND | --- | --- |
| T144 | GND | --- | --- |
| T145 | GND | --- | --- |
| T146 | +VIN | --- | --- |
| T147 | +VIN | --- | --- |
| T148 | +VIN | --- | --- |
| T149 | +VIN | --- | --- |
| T150 | +VIN | --- | --- |
| T151 | +VIN | --- | --- |
| T152 | +VIN | --- | --- |
| T153 | +VIN | --- | --- |
| T154 | +VIN | --- | --- |

Table 5 Module connector: top pins

4.1.2 Module Connector – Bottom Pins

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|-----|--------------------------------|------------------------|-----------|
| B1 | ADC_CH_11 | --- | --- |
| B2 | ADC_CH_10 | --- | --- |
| B3 | GND | --- | --- |
| B4 | ADC_CH_09 | --- | --- |
| B5 | ADC_CH_08 | --- | --- |
| B6 | GND | --- | --- |
| B7 | ADC_CH_07 | --- | --- |
| B8 | ADC_CH_06 | --- | --- |
| B9 | GND | --- | --- |
| BK1 | PMIC_STBY# | --- | --- |
| BK2 | PMIC_VDD_OK | --- | --- |
| B10 | ADC_CH_05 | --- | --- |
| B11 | ADC_CH_04 | --- | --- |
| B12 | GND | --- | --- |
| B13 | ADC_CH_03 | --- | --- |
| B14 | ADC_CH_02 | --- | --- |
| B15 | GND | --- | --- |
| B16 | ADC_CH_01 | --- | --- |
| B17 | ADC_CH_00 | --- | --- |
| B18 | GND | --- | --- |
| B19 | CAN00_RX | --- | ✓ (INPUT) |
| B20 | CAN00_TX | --- | ✓ |
| B21 | GND | --- | --- |
| B22 | CAN01_RX | --- | ✓ (INPUT) |
| B23 | CAN01_TX | --- | ✓ |
| B24 | GND | --- | --- |
| B25 | CAN02_RX | --- | ✓ (INPUT) |
| B26 | CAN02_TX | --- | ✓ |
| B27 | GND | --- | --- |
| B28 | CAN03_RX | --- | ✓ (INPUT) |
| B29 | CAN03_TX | --- | ✓ |
| B30 | GND | --- | --- |
| B31 | CAN04_RX | ✓ | ✓ (INPUT) |
| B32 | CAN04_TX | ✓ | ✓ |

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|-----|--------------------------------|------------------------|-----------|
| B33 | GND | --- | --- |
| B34 | CAN05_RX | ✓ | ✓ (INPUT) |
| B35 | CAN05_TX | ✓ | ✓ |
| B36 | GND | --- | --- |
| B37 | CAN06_RX | ✓ | ✓ (INPUT) |
| B38 | CAN06_TX | ✓ | ✓ |
| B39 | GND | --- | --- |
| B40 | CAN07_RX | ✓ | ✓ (INPUT) |
| B41 | CAN07_TX | ✓ | ✓ |
| B42 | GND | --- | --- |
| B43 | CAN08_RX | ✓ | ✓ (INPUT) |
| B44 | CAN08_TX | ✓ | ✓ |
| B45 | GND | --- | --- |
| B46 | CAN09_RX | ✓ | ✓ (INPUT) |
| B47 | CAN09_TX | ✓ | ✓ |
| B48 | GND | --- | --- |
| B49 | CAN10_RX | ✓ | ✓ (INPUT) |
| B50 | CAN10_TX | ✓ | ✓ |
| B51 | GND | --- | --- |
| B52 | CAN11_RX | ✓ | ✓ (INPUT) |
| B53 | CAN11_TX | ✓ | ✓ |
| B54 | GND | --- | --- |
| B55 | CAN12_RX | ✓ | ✓ (INPUT) |
| B56 | CAN12_TX | ✓ | ✓ |
| B57 | GND | --- | --- |
| B58 | CAN13_RX | ✓ | ✓ (INPUT) |
| B59 | CAN13_TX | ✓ | ✓ |
| B60 | GND | --- | --- |
| B61 | CAN14_RX | ✓ | ✓ (INPUT) |
| B62 | CAN14_TX | ✓ | ✓ |
| B63 | GND | --- | --- |
| B64 | CAN15_RX | ✓ | ✓ (INPUT) |
| B65 | CAN15_TX | ✓ | ✓ |
| B66 | GND | --- | --- |
| B67 | PA15_DSPIO_SOUT | ✓ | ✓ |
| B68 | PA13_DSPIO_SCK | ✓ | ✓ |

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|------|--------------------------------|------------------------|-------|
| B69 | PA14_DSPI0_SIN | ✓ | ✓ |
| B70 | PB09_DSPI0_CS1 | ✓ | ✓ |
| B71 | PB10_DSPI0_CS2 | ✓ | ✓ |
| B72 | GND | --- | --- |
| B73 | PA06_DSPI1_SOUT | ✓ | ✓ |
| B74 | PA08_DSPI1_SCK | ✓ | ✓ |
| B75 | PF15_DSPI1_SIN | ✓ | ✓ |
| B76 | PA07_DSPI1_CS0 | ✓ | ✓ |
| B77 | GND | --- | --- |
| B78 | PA11_DSPI5_SOUT | ✓ | ✓ |
| B79 | PA09_DSPI5_SCK | ✓ | ✓ |
| B80 | PA10_DSPI5_SIN | ✓ | ✓ |
| B81 | PA12_DSPI5_CS0 | ✓ | ✓ |
| B82 | JTAG_TCK | --- | ✓ |
| B83 | JTAG_TDO | --- | ✓ |
| B84 | JTAG_TDI | --- | ✓ |
| B85 | JTAG_TMS | --- | ✓ |
| B86 | JCOMP | --- | --- |
| B87 | GND | --- | --- |
| B88 | PF03_CLKOUT0 | --- | ✓ |
| B89 | PF04_CLKOUT1 | --- | ✓ |
| B90 | GND | --- | --- |
| B91 | FLXR0A_RX_D | ✓ | ✓ |
| B92 | FLXR0A_TX_D | ✓ | ✓ |
| B93 | FLXR0A_TXEN# | ✓ | ✓ |
| B94 | GND | --- | --- |
| B95 | FLXR0B_RX_D | ✓ | ✓ |
| B96 | FLXR0B_TX_D | ✓ | ✓ |
| B97 | FLXR0B_TXEN# | ✓ | ✓ |
| B98 | GND | --- | --- |
| B99 | PB12_FXCAN2_RX | ✓ | ✓ |
| B100 | PB11_FXCAN2_TX | ✓ | ✓ |
| B101 | GND | --- | --- |
| B102 | PB14_FXCAN3_RX | ✓ | ✓ |
| B103 | PB13_FXCAN3_TX | ✓ | ✓ |
| B104 | GND | --- | --- |

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|------|--------------------------------|------------------------|-----------|
| B105 | LIN0_RX | --- | ✓ (INPUT) |
| B106 | LIN0_TX | ✓ | ✓ |
| B107 | GND | --- | --- |
| B108 | LIN1_RX | ✓ | ✓ (INPUT) |
| B109 | LIN1_TX | ✓ | ✓ |
| B110 | GND | --- | --- |
| B111 | LIN2_RX | ✓ | ✓ (INPUT) |
| B112 | LIN2_TX | ✓ | ✓ |
| B113 | GND | --- | --- |
| B114 | LIN3_RX | --- | ✓ (INPUT) |
| B115 | LIN3_TX | ✓ | ✓ |
| B116 | GND | --- | --- |
| B117 | PCIE1_CLKC_N | --- | --- |
| B118 | PCIE1_CLKC_P | --- | --- |
| B119 | GND | --- | --- |
| B120 | PCIE0_CLKC_N | --- | --- |
| B121 | PCIE0_CLKC_P | --- | --- |
| B122 | GND | --- | --- |
| B123 | PMIC_FSOUT# | --- | --- |
| B124 | PMIC_FIN/MCU_SWD_RST# | --- | --- |
| B125 | VDD_OTP | --- | --- |
| B126 | PMIC_PWROFF# | --- | --- |
| B127 | PMIC_PSYNC | --- | --- |
| B128 | PMIC_FOUT/AMUX | --- | --- |
| B129 | GND | --- | --- |
| B130 | PC09_UART0_TX | ✓ | ✓ |
| B131 | PC10_UART0_RX | ✓ | ✓ |
| B132 | GND | --- | --- |
| B133 | PB01_I2C0_SCL | ✓ | ✓ |
| B134 | PB00_I2C0_SDA | ✓ | ✓ |
| B135 | PB03_I2C1_SCL | ✓ | ✓ |
| B136 | PB04_I2C1_SDA | ✓ | ✓ |
| B137 | PB05_I2C2_SCL | ✓ | ✓ |
| B138 | PB06_I2C2_SDA | ✓ | ✓ |
| B139 | GND | --- | --- |
| B140 | GND | --- | --- |

| Pin | Pin Name / Primary Function | Alternate Functions | GPIO? |
|------|--------------------------------|------------------------|-------|
| B141 | GND | --- | --- |
| B142 | GND | --- | --- |
| B143 | GND | --- | --- |
| B144 | GND | --- | --- |
| B145 | GND | --- | --- |
| B146 | GND | --- | --- |
| B147 | GND | --- | --- |
| B148 | +VIN | --- | --- |
| B149 | +VIN | --- | --- |
| B150 | +VIN | --- | --- |
| B151 | +VIN | --- | --- |
| B152 | +VIN | --- | --- |
| B153 | +VIN | --- | --- |
| B154 | +VIN | --- | --- |
| B155 | +VIN | --- | --- |
| B156 | +VIN | --- | --- |

Table 6 Module connector: bottom pins

4.2 Power Structure

The MPX-S32G399A module is supplied by a single 6-36V supply. Onboard voltages are generated by the PMIC VR5510. The core voltage is generated from 3V3.

For RTC backup buffering an additional supply “VCC_RTC” is necessary from the carrier.

The module itself does not provide any supply voltage to the carrier but it has some reference voltages that show the voltage level of the respective interface on the module. If necessary, the carrier must track the reference voltages and generate a copy which can carry higher loads.

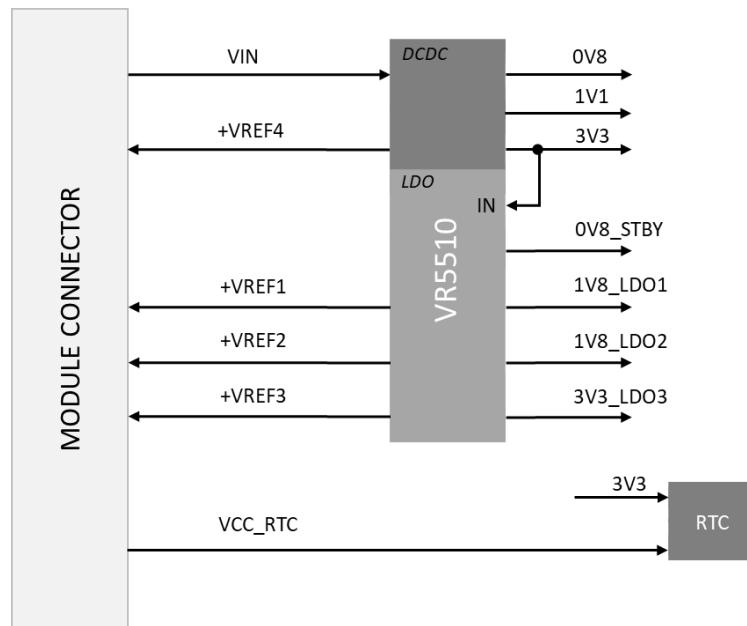


Figure 4-1 Power supplies: structure

The following table shows the available voltages on the module connector:

| Module Connector | | | |
|-----------------------|----------|---------------------------------|---|
| Pin | Signal | I/O Range | Description |
| T146-T154 / B148-B156 | VIN | 6-36V | Module supply input |
| T117 | +VREF1 | 1.8V | Reference voltage output |
| T118 | +VREF2 | 1.8V | Reference voltage output |
| T119 | +VREF3 | 3.3V | Reference voltage output |
| T120 | +VREF4 | 3.3V | Reference voltage output |
| T133 | VCC_RTC | 1.1V-5.5V | Optional backup supply |
| T134 | +3V3_EXT | 3.3V | Optional boot EEPROM programming supply input |
| B125 | VDD_OTP | typ. 7.5V see PMIC datasheet | Optional voltage for PMIC debug mode. May be left open if debugging is not required. Power sequence can be found in PMIC datasheet. |

Table 7 Module connector: power pin assignments

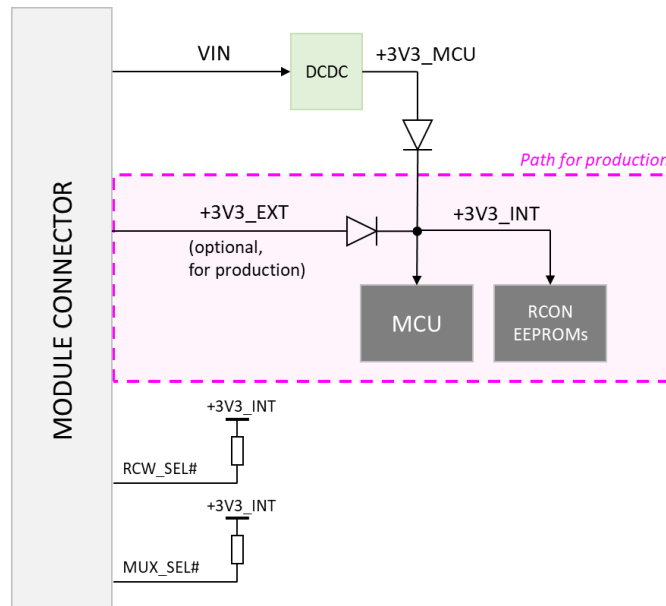


Figure 4-2 Power supplies: microcontroller

The onboard microcontroller is supplied by a 3.3V rail that is generated from a DCDC regulator fed by input supply. During the production test it is necessary to do some pre-programming which is achieved by connecting +3V3_EXT to an unpowered module.

+3V3_EXT is not necessary for standard customer baseboards and can be left unconnected.

There's no limitation with using RCW_SEL# for boot source selection when +3V3_EXT is omitted. This signal has an onboard pullup and only needs to be pulled low on the carrier if required.

The diode-ORing in Figure 4-2 is a simplified representation of the actual implementation, where +3V3_MCU (generated from input supply) takes precedence over +3V3_EXT.

4.3 Reset Structure

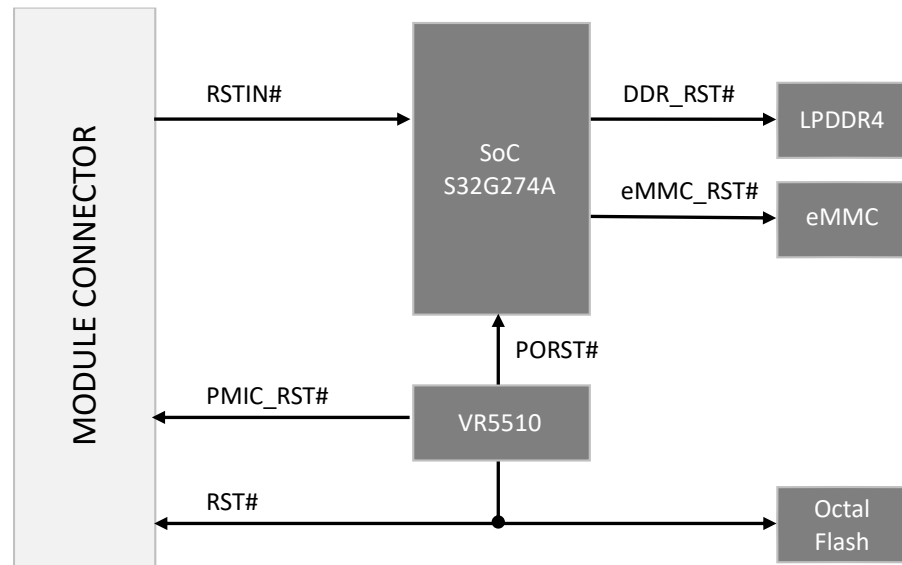


Figure 4-3 Reset Structure

The reset structure of the MPX-S32G399A module is shown in Figure 4-3. The board resets are controlled by the system power management chip (PMIC) VR5510.

When the onboard voltages of the module are within their limits, the power good signal in combination with the RSTIN# signal will release the PORST# of the SoC. PMIC_RST# controls both the SoC and peripheral devices. PMIC_RST# and RST# are identical signals. The only difference is that RST# could be disconnected by a zero-ohm resistor.

As RST# is bi-directional, it can also be used as JTAG reset.

The S32G399A provides dedicated reset signals for eMMC and LPDDR4 memories.

| Signal Name | Function | Type |
|-------------|----------------------------|--|
| RSTIN# | System Global Reset Input | 100R series resistance / 10nF / 4k7 Pullup |
| RST# | System Global Reset / JTAG | Open Drain |
| PMIC_RST# | System Global Reset | Open Drain |
| PORST# | Power-On Reset for SoC | |
| DDR_RST# | Reset for LPDDR Memory | |
| EMMC_RST# | Reset for eMMC Memory | |

Table 4-3 Reset signal overview

4.4 Clock Structure

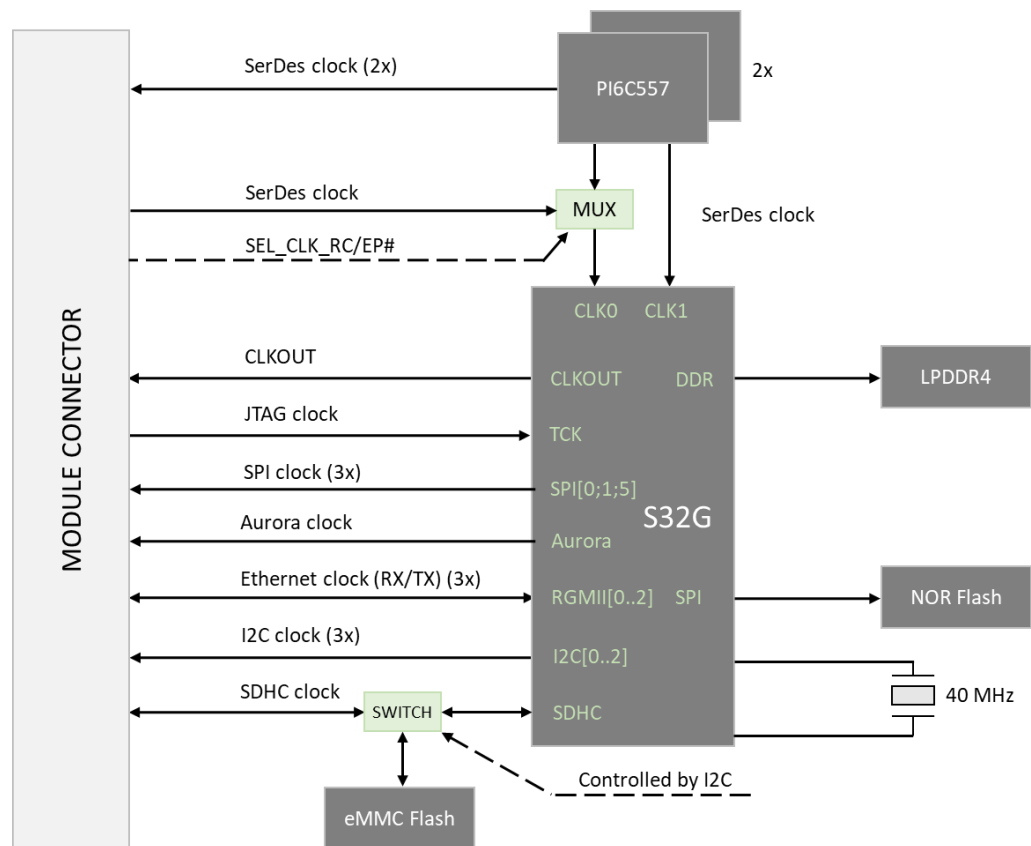


Figure 4-4 Clock Structure

The S32G399A offers two SerDes channels with four lanes in total which can be configured as PCIe or SGMII. To be compliant with the NXP documentation they are referred to as “PCIE0” and “PCIE1”.

Each SerDes channel requires a clock which can be configured as 100MHz or 125MHz clock depending on PCIe or SGMII use.

| J12 (PI6C557) | | | S32G399A “PCIE0” channel | | | | |
|---------------|--------|---|--------------------------|-------------|-----------|---------------------|-------------|
| Pin | Signal | | Pin | Signal | I/O Range | Signal conditioning | Frequency |
| 15 | CLK0+ | → | AB15 | PCIE0_CLK_P | HCSL | SR: 33R PD: 49R9 | 100/125 MHz |
| 14 | CLK0- | → | AC15 | PCIE0_CLK_N | HCSL | SR: 33R PD: 49R9 | 100/125 MHz |

| J12 (PI6C557) | | Module Connector | | | | | |
|---------------|--------|------------------|------|--------------|-----------|---------------------|-------------|
| Pin | Signal | | Pin | Signal | I/O Range | Signal conditioning | Frequency |
| 11 | CLK1+ | → | B121 | PCIE0_CLKC_P | HCSL | SR: 33R PD: 49R9 | 100/125 MHz |
| 10 | CLK1- | → | B120 | PCIE0_CLKC_N | HCSL | SR: 33R PD: 49R9 | 100/125 MHz |

Table 8 PCIe0 clock: pin assignments

Channel 0 can also be configured as a PCIe Endpoint. In this case the SoC can be fed with an external clock from the carrier:

| S32G399A | | Module Connector | | | | | |
|----------|-------------|------------------|------|---------------|-----------|---------------------|-----------|
| Ball | Signal | | Pin | Signal | I/O Range | Signal conditioning | Frequency |
| AB15 | PCIE0_CLK_P | ← | T123 | PCIE0_CLKIN_P | HCSL | | 100 MHz |
| AC15 | PCIE0_CLK_N | ← | T122 | PCIE0_CLKIN_N | HCSL | | 100 MHz |

Table 9 PCIe clock for endpoint configuration

Channel 1 is fed from J16:

| J16 (PI6C557) | | Module Connector | | | | | |
|---------------|--------|------------------|------|--------------|-----------|---------------------|-------------|
| Pin | Signal | | Pin | Signal | I/O Range | Signal conditioning | Frequency |
| 15 | CLK0+ | → | B121 | PCIE1_CLKC_P | HCSL | SR: 33R PD: 49R9 | 100/125 MHz |
| 14 | CLK0- | → | B120 | PCIE1_CLKC_N | HCSL | SR: 33R PD: 49R9 | 100/125 MHz |

| J16 (PI6C557) | | Module Connector | | | | | |
|---------------|--------|------------------|------|-------------|-----------|---------------------|-------------|
| Pin | Signal | | Pin | Signal | I/O Range | Signal conditioning | Frequency |
| 11 | CLK1+ | → | AB16 | PCIE1_CLK_P | HCSL | SR: 33R PD: 49R9 | 100/125 MHz |
| 10 | CLK1- | → | AC16 | PCIE1_CLK_N | HCSL | SR: 33R PD: 49R9 | 100/125 MHz |

Table 10 PCIe1 clock: pin assignments

The following table shows the available clocks configured as primary interface on the MPX-S32G399A:

| S32G399A | | | Module Connector | | | | |
|----------|---------------|---|------------------|----------------|-----------|---------------------|-----------|
| Ball | Signal | | Pin | Signal | I/O Range | Signal conditioning | Frequency |
| E19 | SD0_CLK | → | T2 | SD_CLK | +VREF3 | SR: 22R | t.b.d |
| U12 | DSPI0_SCK | → | B68 | PA13_DSPI0_SCK | +VREF3 | | t.b.d |
| U10 | DSPI1_SCK | → | B74 | PA08_DSPI1_SCK | +VREF3 | | t.b.d |
| B8 | DSPI5_SCK | → | B79 | PA09_DSPI5_SCK | +VREF3 | | t.b.d |
| E7 | I2C0_SCL | → | B133 | PB01_I2C0_SCL | +VREF3 | PU: 2k7 | 400 kHz |
| C6 | I2C1_SCL | → | B135 | PB03_I2C1_SCL | +VREF3 | PU: 4k7 | 400 kHz |
| A6 | I2C2_SCL | → | B137 | PB05_I2C2_SCL | +VREF3 | PU: 4k7 | 400 kHz |
| AC11 | AUR_CLK_P | ← | T97 | AUR_CLK_P | +VREF1 | | t.b.d. |
| AB11 | AUR_CLK_N | ← | T96 | AUR_CLK_N | +VREF1 | | t.b.d. |
| W9 | TCK | ← | B82 | JTAG_TCK | +VREF3 | PD: 10k | t.b.d. |
| V20 | RGMII0_TX_CLK | → | T67 | RGMII0_TX_CLK | +VREF1 | SR: 10R | 125 MHz |
| V21 | RGMII0_RX_CLK | ← | T59 | RGMII0_RX_CLK | +VREF1 | SR: 10R | 125 MHz |
| Y21 | RGMII0_MDC | → | T50 | RGMII0_MDC | +VREF1 | SR: 10R | < 10 MHz. |
| P20 | RGMII1_TX_CLK | → | T48 | RGMII1_TX_CLK | +VREF1 | SR: 10R | 125 MHz |
| R21 | RGMII1_RX_CLK | ← | T40 | RGMII1_RX_CLK | +VREF1 | SR: 10R | 125 MHz |
| V23 | RGMII1_MDC | → | T31 | RGMII1_MDC | +VREF1 | SR: 10R | < 10 MHz |
| N19 | RGMII2_TX_CLK | → | T29 | RGMII2_TX_CLK | +VREF2 | SR: 10R | 125 MHz |
| P21 | RGMII2_RX_CLK | ← | T21 | RGMII2_RX_CLK | +VREF2 | SR: 10R | 125 MHz |
| M19 | RGMII2_MDC | → | T12 | RGMII2_MDC | +VREF2 | SR: 10R | < 10 MHz |

Table 11 Clock: pin assignments

4.5 Boot Mode Configuration

The MPX-S32G399A module offers several different boot modes to choose from. The settings can be done via the MCU J27 on the module in case the FUSE_SEL fuse is not blown.

The S32G399A can retrieve the boot configuration (abbreviated: BOOT_CFG) either from fuses or from a serial EEPROM. This latter mode is called “RCON” mode.

FUSE_SEL = 0

| BOOTMOD0 (ball W10) | BOOTMOD1 (ball W11) | Ethernet boot config | Boot Mode |
|------------------------|------------------------|----------------------|-------------|
| 0 | 0 | No Ethernet | Serial Boot |
| 0 | 1 | SGMII | Serial Boot |
| 1 | 0 | | RCON |
| 1 | 1 | | Reserved |

Table 12 Boot mode settings (no fuse)

FUSE_SEL = 1

| BOOTMOD0 (ball W10) | BOOTMOD1 (ball W11) | Ethernet boot config | Boot Mode |
|------------------------|------------------------|----------------------|-------------|
| 0 | 0 | | Fuses |
| 0 | 1 | | |
| 1 | 0 | | Serial Boot |
| 1 | 1 | | Reserved |

Table 13 Boot mode settings (fuses)

In Serial RCON mode the BOOT_CFG bits are mapped to the EEPROM.

BOOT_CFG1[7:5] configures the boot devices:

| BOOT_CFG1[7:5] | Boot Source | Description | Boot Location |
|----------------|--------------|---|---------------|
| 000 | QuadSPI Boot | Quad/Hyper/Octal Flash (see BOOT_CFG[4:2]) | Module |
| 010 | SD Boot | SD Card | Carrier |
| 011 | eMMC Boot | eMMC | Module |

Table 14 Boot devices

4.6 LEDs

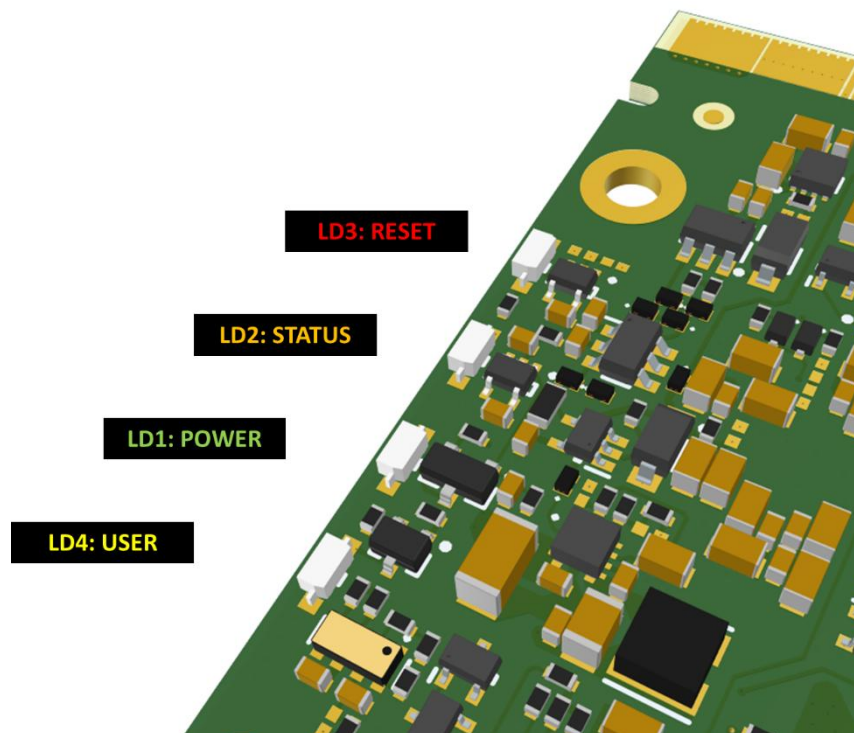


Figure 4-5 LEDs

There are four LEDs on the bottom side of the MPX-S32G399A module. The side-looker LEDs are placed near the edge of the PCB.

| Reference | Color | Function | |
|-----------|--------|----------|--|
| LD1 | Green | LED ON: | Power-up sequence of the module is finished, power is good |
| | | LED OFF: | Power fail |
| LD2 | Orange | LED ON: | SAFEIO error |
| | | LED OFF: | No error detected |
| LD3 | Red | LED ON: | Module / Peripheral reset is active |
| | | LED OFF: | Reset is inactive |
| LD4 | Yellow | LED ON: | User defined function (S32G, GPIO "PC_13" on ball Y7) |
| | | LED OFF: | User defined function (S32G, GPIO "PC_13" on ball Y7) |

Table 15 LED: pin description

4.7 RTC

The Real-Time Clock (RTC) is implemented with a Micro Crystal RV-3028-C7 chip:

- I²C clock frequency up to 400 kHz
- Operating temperature -40°C to 85°C
- Slave address according to Table 26
- 3.3V supply voltage

The RTC is supplied by 3.3V (reference voltage: +VREF4) and has an optional backup voltage that needs to be provided from the carrier if buffering is desired. The following table shows the internal connection:

| Module Connector | | | |
|------------------|---------|-------------|---|
| Pin | Signal | I/O Range | Description |
| T133 | VCC_RTC | 1.1V – 5.5V | Battery backup voltage provided by the carrier (optional) |

Table 16 RTC: backup voltage



NOTE

Automatic switchover is deactivated per default setting.

Do not use “Direct Switching Mode” in case VCC_RTC > 3.3V, as I²C access to the RTC is disabled when the module is powered again.

Use “Level Switching Mode” instead.

The RTC's interrupt output is connected to the CPU:

| CPU | | RV-3028-C7 | | | |
|------|-----------|------------|--------|-----------|---------------------|
| Ball | Signal | Pin | Signal | I/O Range | Signal conditioning |
| U9 | RTC_IRQA# | ← 2 | INT# | +VREF3 | PU: 4k7 |

Table 17 RTC: IRQ

4.8 Temperature sensors

The MPX-S32G399 module has two different temperature sensors.

4.8.1 TMP112

- I²C clock frequency up to 400 kHz
- Operating temperature -40°C to 125°C
- Slave addresses according to Table 26
- Local temperature monitoring
- Interrupt for thermal alert (configurable)
- ≤ 1% accuracy over temperature range

The temperature sensor provides an interrupt which is connected to the microcontroller.

| GPIO Expander | | TMP112 | | | |
|---------------|---------------|--------|--------|-----------|---------------------|
| Pin | Signal | Pin | Signal | I/O Range | Signal conditioning |
| 14 | THERM_ALERT1# | ← 3 | ALERT | VMCU | PU: MCU internal |

Table 18 Temperature sensor: IRQ1

4.8.2 MCP9802

- I²C clock frequency up to 400 kHz
- Operating temperature -55°C to 125°C
- Slave addresses according to Table 26
- Local temperature monitoring
- Interrupt for thermal alert (configurable)
- ≤ 3% accuracy over temperature range

The temperature sensor provides an interrupt which is connected to the microcontroller.

| GPIO Expander | | TMP112 | | | |
|---------------|---------------|--------|--------|-----------|---------------------|
| Pin | Signal | Pin | Signal | I/O Range | Signal conditioning |
| 22 | THERM_ALERT2# | ← 3 | ALERT | VMCU | PU: MCU internal |

Table 19 Temperature sensor: IRQ2

4.9 eFuse

S32G CPUs support fuse programming which requires an additional voltage “VDD_EFUSE” (1.8V typ.).

This voltage can be toggled on/off by GPIO “PD_11” on ball Y10 of the S32G.

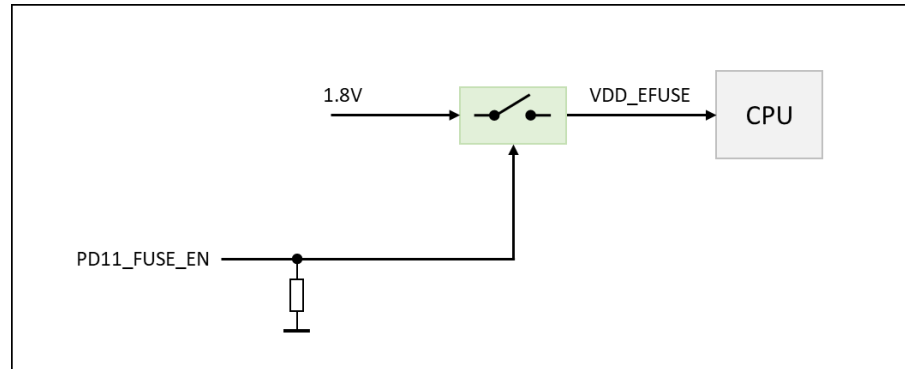


Figure 4-6 Fuse Programming

4.10 Serial Boot EEPROM (RCON)

In chapter 4.5 the boot modes were described. Two EEPROMs are installed on the module to store the settings for Serial RCON mode. Serial RCON mode always uses I2C0 on address 0x50 to load the board configuration.

The second EEPROM is accessible on address 0x56.

The addresses of the two EEPROMs can be swapped, thus each EEPROM can be used to load the board configuration. Swapping is achieved with the RCW_SEL# signal from the carrier.

According to Table 14 more than two boot devices are supported. J22 is classified as primary EEPROM to store the boot configuration for SD card boot. J14 is the secondary EEPROM used for any other boot configuration than SD card boot mode. The code can be loaded by the user, stored in the EEPROM, and selected via the carrier.



If the FUSE_SEL fuse is blown the SoC will always boot from fuses (FUSE_SEL = 1).

| FUSE_SEL | SD / eMMC MUX | RCW_SEL# | Description | |
|-------------------------------|---|----------|--|--|
| 0 (normal boot) | Microcontroller: • SD-Card • eMMC | 0 | Boot from J14 configuration | |
| | | 1 | Boot from J22 configuration | |
| 1 (boot from fuses) | Microcontroller: • SD-Card • eMMC | X | BOOT SOURCE DETERMINED BY FUSES | <ul style="list-style-type: none"> • SD-Card • eMMC • SPI NOR |

Table 20 Boot configuration

There are two options for booting, either from fuses or from pin configuration. In either way the hardware routing must be set correctly in EEPROM, MCU respectively. See chapter 4.11 for details.

The boot source for RCW boot is determined by the configuration in any EEPROM. RCW_SEL# selects which configuration is finally loaded.

4.11 Microcontroller

The microcontroller (MCU) has been assigned the task as monitoring, supervising and control unit. It replaces the electronic DIP switch previously used on older revisions, providing enhanced and flexible options.

The MCU can be accessed via I2C interface with slave address according to Table 26. The communication with the device has been implemented via a register interface. The settings of MCU are stored in the boot EEPROMs used for RCON storage. Thus, the settings can be changed by RCW_SEL# pin.

Initial settings are programmed during production test and can be overridden via I2C.

4.11.1 Mode of operation

After power up of MCU, the power to CPU is kept disabled and reset line is active. MCU starts monitoring the supplies and temperatures. The content of current active EEPROM is read into local memory, boot config pins and multiplexer select are set, SAFEIO gets signaled, and system power gets turned on. After PMIC has turned on all power supplies, the MCU releases the reset line and starts the CPU.

The CPU boots and needs to inform MCU about start of normal operation. This stop signaling SAFEIO and starts the optional challenge response watchdog timer.

For safety purposes the microcontroller provides two signals, SAFEIO and KILL. Both share their pins with the SWD programming interface on T81 and T82 of the module connector. Both signals can be masked in settings to disable the output of the frequency if not needed.

SAFEIO and KILL toggle high and low, whereas permanent high or low states signal an error. The nominal frequency is 100 Hz.

Supervisor MCU permanently monitors the power rails as well as temperature sensors on the module. In case of undervoltage or overtemperature the module is set into safe state. This asserts the reset line of CPU and signals the error by stopping to toggle SAFEIO pin. The carrier could monitor this signal and set all peripherals in a safe state as long as the signal is not toggling.

In case of an overvoltage on any supply the MCU stops toggling the KILL signal. The carrier could monitor this signal and turn the system permanently off, for example by burning a fuse or similar.

4.11.2 Challenge Response Watchdog Timer

The CPU is connected to the MCU via I2C. After informing the MCU to be in normal operation mode, the challenge response watchdog timer needs to be serviced. It is implemented as a windowed WDT with a minimum and maximum reset time. The resolution is 1ms with a range of 0-65535 ms. Any reset before the minimum time results in a transition to safe state. No reset up to maximum time also results in a transition to safe state.

The minimum time can be set to 0 to disable this check and the maximum time can be set to 65535ms to disable the timeout check. Default values are 0ms minimum and 10s maximum.

To reset the watchdog timer the content of WDT-Response register should be read, its value should be incremented by one and bit 7 should be cleared. This value should be written into the WDT-Challenge register. The MCU increases this value by one, sets bit 7 and writes this new value into the WDT-Response register.

A wrong content in WDT-Response register should cause the application to take appropriate actions to deal with this violation. A wrong value written to WDT-Challenge register will result in a transition to safe state.

4.11.3

Register Interface

| Register | Address | Description |
|-----------------|-----------|---|
| WDT-WindowMin | 0x00 | Minimum CR-WD reset time in ms |
| WDT-WindowMax | 0x02 | Maximum CR-WD reset time in ms |
| WDT-Counter | 0x04 | read only CR-WD counter register (incremented once per ms) |
| WDT-Challenge | 0x06 | The challenge byte to WD-Counter |
| WDT-Response | 0x07 | The response byte from reset WD-Counter |
| CTRL-Operating | 0x08 | Write A8 to start operation mode (safeio clear, start WDT) |
| CTRL-Shutdown | 0x09 | Write A9 to shutdown system |
| CTRL-Reset | 0x0A | Write AA to reset system |
| CTRL-Safeio | 0x0B | Write AB or 0B to enable/disable safio output signal |
| CTRL-Kill | 0x0C | Write AC or 0C to enable/disable safio output signal |
| CTRL-Pinconfig | 0c0D | Configuration Pins Bit 0-3 set CFG 0-3 pins, Bit 4 sets SEL_EMMC_SDHC# See Table 23 Microcontroller: Hardware config pins |
| REV-HW | 0x0E | read only Get HW revision |
| REV-FW-Major | 0x0F | read only Get FW revision major |
| REV-FW-Customer | 0x10 | read only Get FW revision customer |
| REV-FW-Minor | 0x11 | read only Get FW revision minor |
| SELECT-EMMC-SD | 0x12 | Switch multiplexer to SD (0) or eMMC (1) |
| EEPROM_ACCESS | 0x13 | Select alternatively EEPROM (write1) or boot EEPROM (write 0) for following read/write accesses |
| FW-Update | 0x20-0x4F | Description available on request |

Table 21 Microcontroller: Register Interface

Register 0, 2 and 4 are treated as word registers and should be accessed accordingly.

Following table lists some sample commands from Linux

| Register | Format | Example |
|---------------|----------------------------------|---|
| WDT-WindowMin | set 0x00 [VALUE] w get 0x00 w | i2cset -f -y 0 0x10 0x00 0xBBCC w i2cget -f -y 0 0x10 0x00 w |
| WDT-WindowMax | set 0x02 [VALUE] w get 0x02 w | i2cset -f -y 0 0x10 0x02 10000 w i2cget -f -y 0 0x10 0x02 w |
| WDT-Counter | get 0x04 w | i2cget -f -y 0 0x10 0x04 w |
| WDT-Challenge | set 0x06 value get 0x06 | i2cset -f -y 0 0x10 0x06 0x81 i2cget -f -y 0 0x10 0x06 |

| Register | Format | Example |
|-----------------|--------------------|-------------------------------|
| WDT-Response | get 0x07 | i2cget -f -y 0 0x10 0x07 |
| CTRL-Operating | set 0x08 0xA8 | i2cset -f -y 0 0x10 0x08 0xA8 |
| | get 0x08 | i2cget -f -y 0 0x10 0x08 |
| CTRL-Shutdown | set 0x09 0xA9 | i2cset -f -y 0 0x10 0x09 0xA9 |
| CTRL-Reset | set 0x0A 0xAA | i2cset -f -y 0 0x10 0x0A 0xAA |
| CTRL-Safeio | set 0x0B enable | i2cset -f -y 0 0x10 0x0B 0xAB |
| CTRL-Kill | set 0x0C enable | i2cset -f -y 0 0x10 0x0C 0xAC |
| CTRL-Pinconfig | set 0x0D [VALUE] | i2cset -f -y 0 0x10 0x0D 0x0B |
| | get 0x0D | i2cget -f -y 0 0x10 0x0D |
| REV-HW | get 0x0E | i2cget -f -y 0 0x10 0x0E |
| REV-FW-Major | get 0x0F | i2cget -f -y 0 0x10 0x0F |
| REV-FW-Customer | get 0x10 | i2cget -f -y 0 0x10 0x10 |
| REV-FW-Minor | get 0x11 | i2cget -f -y 0 0x10 0x11 |
| SELECT-EMMC-SD | set 0x12 emmc_sd | i2cset -f -y 0 0x10 0x12 0x01 |
| | get 0x12 | i2cget -f -y 0 0x10 0x12 |
| EEPROM-ACCESS | set 0x13 alternate | i2cset -f -y 0 0x10 0x13 0x01 |
| | get 0x13 | i2cget -f -y 0 0x10 0x13 |

Table 22 Microcontroller: Register sample access

4.11.4 Configuration storage

The configuration is stored in RCON EEPROMs. As two EEPROMs exist, it is possible to store two different settings and select one of these before boot by means of RCON_SEL pin. The configs are stored starting from address 0x10. It is not recommended to alter the content directly in EEPROM, but via the commands in MCU.

4.11.5 HW interfaces

At power-up the values for HW_CONFIGx pins are loaded from EEPROM as well as the SEL_EMMC_SDHC# multiplexer select.

| HW_CONFIG_x | Signal Name | Description |
|-------------|--------------------|--|
| 0 | CLKGEN2_100M/125M# | 1 PCIE1_CLK_P/N = 100 MHz (SoC PLL) PCIE1_CLKC_P/N = 100 MHz (ST1: B117 / B118) |
| | | 0 PCIE1_CLK_P/N = 125 MHz (SoC PLL) PCIE1_CLKC_P/N = 125 MHz (ST1: B117 / B118) |
| 1 | CLKGEN1_100M/125M# | 1 PCIE0_CLK_P/N = 100 MHz (SoC PLL) PCIE0_CLKC_P/N = 100 MHz (ST1: B120 / B121) |
| | | 0 PCIE0_CLK_P/N = 125 MHz (SoC PLL) PCIE0_CLKC_P/N = 125 MHz (ST1: B120 / B121) |
| 2 | PA03_BOOTMOD2 | 1 Bootmode Pin 2 (J1: W11) = 1 |
| | | 0 Bootmode Pin 2 (J1: W11) = 0 |
| 3 | PA02_BOOTMOD1 | 1 Bootmode Pin 1 (J1: W10) = 1 |

| HW_CONFIG_x | Signal Name | Description |
|-------------|-------------|--------------------------------|
| | | 0 Bootmode Pin 1 (J1: W10) = 0 |

Table 23 Microcontroller: Hardware config pins

In case SEL_EMMC_SDHC# is high, the eMMC is routed to the CPU. If it is low the SDHC is routed to the CPU.

The microcontroller is programmed via SWD interface:

| Connector Pin | SWD | SAFETY |
|---------------|--------------|--------|
| T81 | MCU_SWD_CLK | KILL |
| T82 | MCU_SWD_DIO | SAFEIO |
| B124 | MCU_SWD_RST# | --- |

Table 24 Microcontroller SWD / safety signals

The alarm output of the two temperature sensors is connected to the MCU. If any sensor detects an overtemperature, the module turns into safe state. The alarm temperature can be programmed into the two sensors. See datasheet of these devices for more details.

4.12 Interface Description

In the following chapters the interfaces of the MPX-S32G399A module are described.



Due to pin multiplexing, there may be limitations regarding the availability of certain interfaces. Nevertheless, different pinouts are possible.

4.12.1 Definition of “Primary Interfaces”

The terms “primary”, “secondary”, ... do not imply any priority. The connector's pin names are derived from the primary functions defined by MicroSys.

Primary interfaces can also be configured for other interfaces. Nevertheless, high speed interfaces are optimized in layout, signals are length and often group matched. Multiplexing information for each pin can be found in the manufacturer's datasheet, some signals are used onboard (see chapter 10.6).

4.12.2 JTAG

The JTAG chain of the MPX-S32G399A includes the S32G399A processor only. The JTAG port is directly connected to the MXM module connector. The JTAG interface can also be configured as GPIO.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

Some debuggers require a 10k pullup on TDI and TDO pins. These are not assembled on the module and may be provided externally for debugging.

4.12.3 AURORA

The Aurora port is a trace port consisting of 4 LVDS data pairs and a LVDS clock pair. The signals are available on the module connector as primary interface with no multiplexing options.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

4.12.4 ADC

The ADC converter contained in the S32G399A processor has 12 multiplexed single-ended channels. They can be accessed via the MXM module connector and do not share their pins with other interfaces.

The pins are listed in the Appendix in chapter 10.4 and 10.5.



There is no protection on any ADC line against over-voltage or wrong polarity. Refer to the S32G399A datasheet for maximum ratings.

4.12.5 CAN

The S32G399A has 4 FlexCANs and 16 LLCE CANs. Due to pin multiplexing, there are limitations.

The MPX-S32G399A module realizes 18 CAN ports as primary interfaces on the module connector, two FlexCANs and 16 LLCE CANs. The ports support CAN2.0 version B and CAN FD protocols at data rates up to 8Mb/s. CAN transceivers are not installed on the module.

The CAN interfaces can also be configured as GPIO.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

4.12.6 RGMII

The S32G399A provides MACs for three RGMII interfaces, each RGMII port has a dedicated MDIO interface.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

RGMII2 is also shared with an ULPI interface for USB PHYs:

| Module Connector | RGMII | ULPI |
|------------------|---------------|---------|
| T15 | RGMII2_RXD3 | USB_D7 |
| T16 | RGMII2_RXD2 | USB_D6 |
| T17 | RGMII2_RXD1 | USB_D5 |
| T18 | RGMII2_RXD0 | USB_D4 |
| T20 | RGMII2_RXDV | USB_D3 |
| T21 | RGMII2_RX_CLK | USB_D2 |
| T23 | RGMII2_TXD3 | USB_D1 |
| T24 | RGMII2_TXD2 | USB_D0 |
| T25 | RGMII2_TXD1 | USB_NXT |
| T26 | RGMII2_TXD0 | USB_STP |
| T28 | RGMII2_TX_EN | USB_DIR |
| T29 | RGMII2_TX_CLK | USB_CLK |

Table 25 RGMII2 / ULPI pin multiplexing options

4.12.7 ULPI (USB)

The MPX-S32G399A does not have a USB PHY but a ULPI interface. The ULPI signals are not available as primary interface on the module connector, but they are shared with RGMII signals. For more details, please see chapter 4.12.6.

The ULPI interface can also be configured as GPIO.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

4.12.8 I2C

The MPX-S32G399A module offers five I²C busses which run at up to 400kHz.

I2C3 is not available as primary interface.

I2C4 is explicitly used for the power management chip on the module.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

I2C0 map:

| Device | | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | Addr |
|-----------------------|---|----|----|----|----|----|----|----|-----|------|
| Microcon- troller | S32K1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1/0 | 0x10 |
| Temperature Sensor | MCP9802A0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1/0 | 0x48 |
| Temperature Sensor | TMP112 (slave address) | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1/0 | 0x49 |
| | TMP112 (General Call reset address) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | -/0 | 0x00 |
| EEPROM | AT24C01C | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1/0 | 0x50 |
| RTC | RV-3028-C7 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1/0 | 0x52 |
| EEPROM | M24C64-DRMF3 (slave address) | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1/0 | 0x54 |
| | M24C64-DRMF3 (identification page) | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1/0 | 0x5C |
| EEPROM | AT24C01C | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1/0 | 0x56 |
| Multiplexer | PCA9540 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1/0 | 0x70 |

Table 26 I2C0: bus map

I2C1 map:

| Device | | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | Addr |
|--------|-----|----|----|----|----|----|----|----|-----|------|
| --- | --- | - | - | - | - | - | - | - | - | - |

Table 27 I2C1: bus map

I2C2 map:

| Device | | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | Addr |
|--------|-----|----|----|----|----|----|----|----|-----|------|
| --- | --- | - | - | - | - | - | - | - | - | - |

Table 28 I2C2: bus map



I2C 3 is available by multiplexing functions. Primary interface is FlexCAN3.

I2C4 map:

| Device | | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | Addr |
|--------|------------------------|----|----|----|----|----|----|----|-----|------|
| PMIC | VR5510 Main logic | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1/0 | 0x20 |
| PMIC | VR5510 Fail-safe logic | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1/0 | 0x21 |
| PMIC | PF5300 debug mode | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1/0 | 0x28 |

Table 29 I2C4: bus map

4.12.9 QSPI (Flash)

The MPX-S32G399A uses the QSPI port A to connect a serial NOR flash (8-bit bus).

The following table shows the internal connections:

| S32G399A | | | SPI NOR Flash MT35XU512ABA1G12 | | |
|----------|---------------|---|-----------------------------------|--------|-----------|
| Ball | Signal | | Pin | Signal | I/O Range |
| G21 | QSPI1_A_CS0# | → | C2 | CS# | 1.8V |
| K20 | QSPI1_A_SCK | → | B2 | CLK | 1.8V |
| K23 | QSPI_A_DQS | ← | C3 | DQS | |
| | | | B3, E5, C1 | GND | |
| L18 | QSPI1_A_DATA0 | ↔ | D3 | D0 | 1.8V |
| L19 | QSPI1_A_DATA1 | ↔ | D2 | D1 | 1.8V |
| L20 | QSPI1_A_DATA2 | ↔ | C4 | D2 | 1.8V |
| K22 | QSPI1_A_DATA3 | ↔ | D4 | D3 | 1.8V |
| K19 | QSPI1_A_DATA4 | ↔ | D5 | D4 | 1.8V |
| J23 | QSPI1_A_DATA5 | ↔ | E3 | D5 | 1.8V |
| H23 | QSPI1_A_DATA6 | ↔ | E2 | D6 | 1.8V |
| K18 | QSPI1_A_DATA7 | ↔ | E1 | D7 | 1.8V |
| | | | B4, E4, D1 | +1.8V | |
| | | | A5 | ECS | PU 1.8V |

Table 30 QSPI NOR Flash: pin assignments

4.12.10 SPI

The MPX-S32G399A has 6 SPI and 4 LLCE SPI interfaces. Due to pin multiplexing, there are limitations.

Three SPI interfaces (and no LLCE SPIs) are available as primary interfaces on the module connector.

SPI1 and SPI5 provide one chip select each, whereas SPI0 has two chip selects.

The SPI interfaces can also be configured as GPIO.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

4.12.11 UART

The UART of the MPX-S32G399A module is used as debug console (LINFlex_0). It provides TTL levels and needs to be converted to RS-232 or USB on the carrier, for example.

As there is no dedicated UART controller, each UART requires one LINFlex controller configured for UART mode. The maximum number of available LINFLEX modules is three.

| Port | Function | Module | Ball | I/O Power Domain | PRIMARY Pin Usage | Connector Pin | |
|------------------|--------------------|----------------------|----------------|-------------------|----------------------|---------------|-------------------------------|
| PA_14 | LINO_RX | LINFlex_0 | AA12 | +VREF3 | DSPIO_SIN | B69 | Microsys UART console input |
| PC_10 | LINO_RX | LINFlex_0 | Y12 | +VREF3 | UART0_RX | B131 | |
| PL_00 | LINO_RX | LINFlex_0 | A12 | +VREF4 | LINO_RX | B105 | |
| PA_15 | LINO_TX | LINFlex_0 | W13 | +VREF3 | DSPIO_SOUT | B67 | Microsys UART console output |
| PC_09 | LINO_TX | LINFlex_0 | U11 | +VREF3 | UART0_TX | B130 | |
| PK_15 | LINO_TX | LINFlex_0 | F10 | +VREF3 | LINO_TX | B106 | |
| PB_00 | LIN1_RX | LINFlex_1 | W12 | +VREF3 | I2C0_SDA | B134 | not available for UART muxing |
| PB_10 | LIN1_RX | LINFlex_1 | V11 | +VREF3 | DSPIO_CS2 | B71 | |
| PC_04 | LIN1_RX | LINFlex_1 | C13 | +VREF4 | LIN1_RX | B108 | |
| PA_13 | LIN1_TX | LINFlex_1 | U12 | +VREF3 | DSPIO_SCK | B68 | |
| PB_09 | LIN1_TX | LINFlex_1 | AA10 | +VREF3 | DSPIO_CS1 | B70 | |
| PC_08 | LIN1_TX | LINFlex_1 | B6 | +VREF3 | LIN1_TX | B109 | |
| PB_12 | LIN2_RX | LINFlex_2 | F8 | +VREF3 | FXCAN2_TX | B99 | |
| PE_01 | LIN2_RX | LINFlex_2 | M23 | +VREF1 | RGMII2_RXDV/USB_D3 | T20 | |
| PK_12 | LIN2_RX | LINFlex_2 | C14 | +VREF4 | CAN14_RX | B61 | |
| PB_11 | LIN2_TX | LINFlex_2 | G8 | +VREF3 | FXCAN2_RX | B100 | |
| PE_00 | LIN2_TX | LINFlex_2 | P21 | +VREF1 | RGMII2_RX CLK/USB_D2 | T21 | |
| PK_11 | LIN2_TX | LINFlex_2 | A9 | +VREF3 | CAN14_TX | B62 | |

Table 31 UART multiplexing options

For example:

Additional UARTs could be multiplexed to PC_04 & PC_08 (LINFlex_1) and PB_11 & PB12 (LINFlex_2), respectively.

4.12.12 LIN

The MPX-S32G399A has 3 LINFlex controllers which can be either configured for LIN or UART mode. Moreover, there are 4 LLCE LIN interfaces routed as primary interfaces to the module connector.

The LINFlexD controllers' pins are not available as primary interfaces on the connector but shared with other interfaces due to pin multiplexing.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

4.12.13 FlexRay

The MPX-S32G399A has 1 LLCE FlexRay interface with dual channels as primary interface and another shared FlexRay interface due to pin multiplexing.

The pins are listed in the Appendix in chapter 10.4 and 10.5.

4.12.14 SDHC

The MPX-S32G399A module has an SDHC interface with 8 data bits. It is either routed to an onboard eMMC memory (8-bit) or to the module connector (4-bit). The multiplexing is controlled by I2C via the MCU (see chapter 4.11.3 Register Interface).

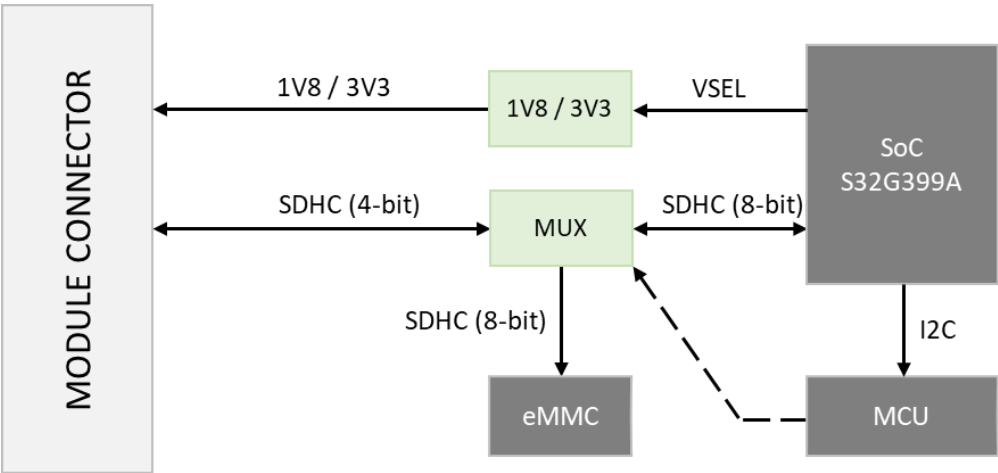


Figure 4-7 SDHC routing

Voltage is controlled by SD0_VSELECT from the SoC:

| S32G399A Ball | Signal | Signal Conditioning | Function | |
|---------------|-------------|---------------------|----------|------|
| G19 | SD0_VSELECT | PD: 10k | 0 | 3.3V |
| | | | 1 | 1.8V |

Table 32 SDHC voltage select

“VCC_SDHC_1V8/3V3” is a reference voltage which indicates the level of the supply voltage of the SDHC interface:

| J23 | | Module Connector | | | |
|------|------------------|------------------|------------------|-------------|---------------------|
| Ball | Signal | Pin | Signal | I/O Range | Signal conditioning |
| B2 | VCC_SDHC_1V8/3V3 | → TK1 | VCC_SDHC_1V8/3V3 | 1.8V / 3.3V | |

4.12.15 SerDes

The S32G399A offers two SerDes channels with four lanes in total which can be configured as PCIe or SGMII. To be consistent with the NXP documentation they are referred to as “PCIE0” and “PCIE1”.

Each SerDes channel requires a clock which can be configured as 100MHz or 125MHz clock depending on PCIe or SGMII use. More information on SerDes clocks can be obtained from chapter 4.4.

SerDes 0 (“PCIE0”):

| Lane 0 | Lane 1 | Clock |
|-----------------|-----------------|-------------------|
| PCIe x2 | | 100 MHz |
| PCIe x1 | SGMII 1.25 Gbps | 100 MHz |
| SGMII 1.25 Gbps | SGMII 1.25 Gbps | 125 MHz (100 MHz) |

Table 33 SerDes 0: working modes

SerDes 1 (“PCIE1”):

| Lane 0 | Lane 1 | Clock |
|------------------|------------------|-------------------|
| PCIe x2 | | 100 MHz |
| PCIe x1 | SGMII 1.25 Gbps | 100 MHz |
| SGMII 1.25 Gbps | SGMII 1.25 Gbps | 125 MHz (100 MHz) |
| SGMII 3.125 Gbps | SGMII 1.25 Gbps | 125 MHz |
| SGMII 1.25 Gbps | SGMII 3.125 Gbps | 125 MHz |
| SGMII 3.125 Gbps | SGMII 3.125 Gbps | 125 MHz |
| PCIe x1 (Gen2) | SGMII 3.125 Gbps | 100 MHz |

Table 34 SerDes 1: working modes

The MPX-S32G399A generates four clock pairs. Two of them are routed to the carrier (“CLKC”) and the other two to the SerDes PLLs of the SoC (“CLKM”). For each SerDes “CLKC” and “CLKM” have the same frequency and can be controlled via microcontroller interface.

The S32G399A can also be used as a PCIe endpoint. In this case, SerDes 0 (“PCIE0”) receives its clock pair from the carrier. To control the multiplexer on the module, “SEL_CLK_RC/EP#” needs to be driven low.

However, root complex (RC) or endpoint (EP) mode is determined via software.

| Pin | Signal | Signal Conditioning | Function | |
|------|----------------|---------------------|----------|---|
| T130 | SEL_CLK_RC/EP# | PU: 10k | 0 | S32G399A is endpoint (clock from carrier) |
| | | | 1 | S32G399A is root complex (clock from module) |

Table 35 SerDes: root complex / endpoint

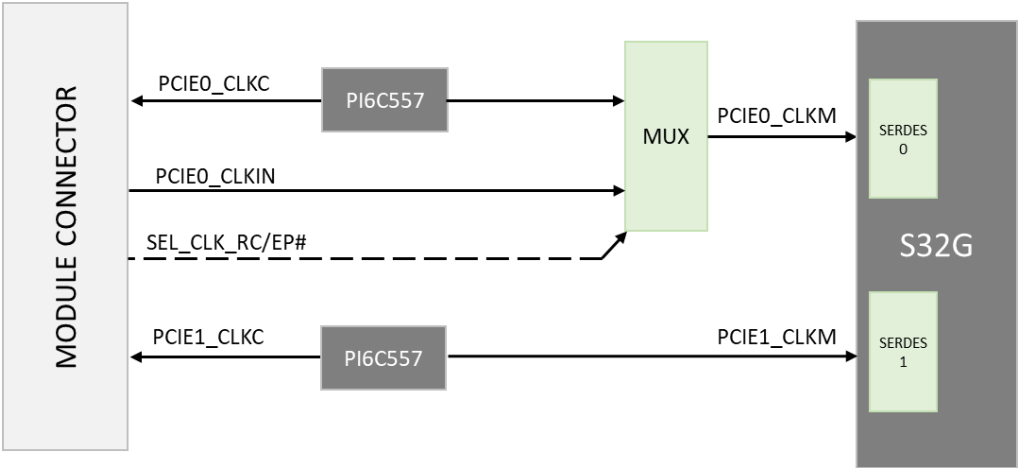


Figure 4-8 SerDes: clock routing

4.13 Differences between MPX-S32G274 and MPX-S32G399A

MPX-S32G274A and MPX-S32G399A have two typical differences related to hardware design.

First, S32G3 processor have more cores and higher performance. Therefore, they require more power. This must be considered for carrier board design when power supply is designed.

Second, S32G3 processors offer more SerDes configurations compared to S32G2 processors. That means, if a carrier board must support both processors, the design must implement an intersecting set of all SerDes modes.

NXP provides tables for “SerDes_0 working modes” and “SerDes_1 working modes” in the reference manual of the respective CPU.

4.14 Debug mode

When debugging the MPX-S32G module, users are recommended to set the VR5510 PMIC into debug mode. This is necessary to deactivate the watchdog in the PMIC that otherwise would power cycle the system if the CPU is halted by the debugger.

To set the PMIC into debug mode, follow the steps described below:

1. Apply a voltage of 5.0 V to the VDD_OTP pin of the module while applying power to the +VIN at the same time. Ensure that the PMIC_PWRON1 pin is LOW.
2. Release the PMIC_PWRON1 pin.
3. After a minimum of 8 ms, remove the voltage from the VDD_OTP pin. There is no maximum limit on the duration you can keep the VDD_OTP pin supplied. As long as the supply is kept on the VDD_OTP pin, the PMIC regulators are turned off.
4. The PMIC starts in debug mode after removing the supply to the VDD_OTP pin. According to the VR5510 datasheet:

In Debug mode, the Watchdog window is fully opened, the Deep Fail-safe request from the Fail-safe state machine (DFS = 1) is masked, the 8-second timer monitoring the RSTB pin is disabled and the Failsafe output pin FS0B cannot be released. Entering Standby mode is not possible while the device is in Debug mode.

5 Mechanical Description

5.1 Edge Connector

The MPX-S32G399A module has 314 edge finger contacts. Appropriate sockets on the carrier provide 314 pins with 0.5mm pitch and accept edge cards with a thickness of 1.2mm.

5.2 Previous Numbering Scheme

The numbering scheme is adopted from other MPX modules which used to have 310 edge fingers only. The reason for this was that you could previously choose from a broad variety of connectors on the market including 310-pin and 314-pin types.



310-pin connectors are obsolete now, the numbering scheme has remained the same.

5.3 Current Numbering Scheme

The differences between 310-pin and 314-pin connectors are four key “pins” that do not carry signals on 310-pin connectors. They are physically not present.

These key pins are, however, available on 314-pin connectors and on the MPX-S32G399A module carry signals. See Figure 5-1 for details:

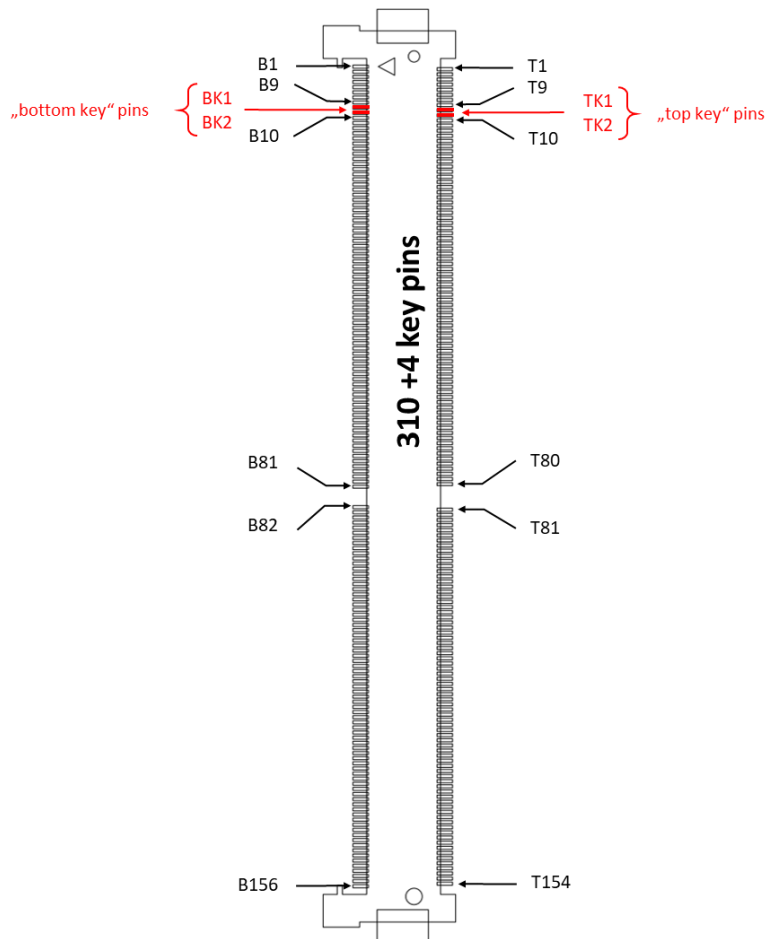


Figure 5-1 MXM Connector: pin definition



The original connector pinout definition was based on MM70-314-310B1-1-R300 which is now OBSOLETE.

314-pin connectors have pins between B9/B10 and T9/T10 which are now connected on the module! They are called “top key” and “bottom key” pins TK1, TK2, BK1, BK2.

5.4 Pin-Layout

The module has 314 pins, 310 pins and 4 pins previously used as key “pins” (see chapter 5.2).

The pin layout is asymmetric, so the pins are unequally distributed among top and bottom side edge fingers.

| Side | Pin Count | Pin Labels |
|--------|-----------|---|
| Bottom | 158 | “B1”, ... “B9”, “BK1” , “BK2” , “B10”, ... “B155”, “B156” |
| Top | 156 | “T1”, ... “T9”, “TK1” , “TK2” , “T10”, ... “T153”, “T154” |

Table 36 Connector pin naming scheme

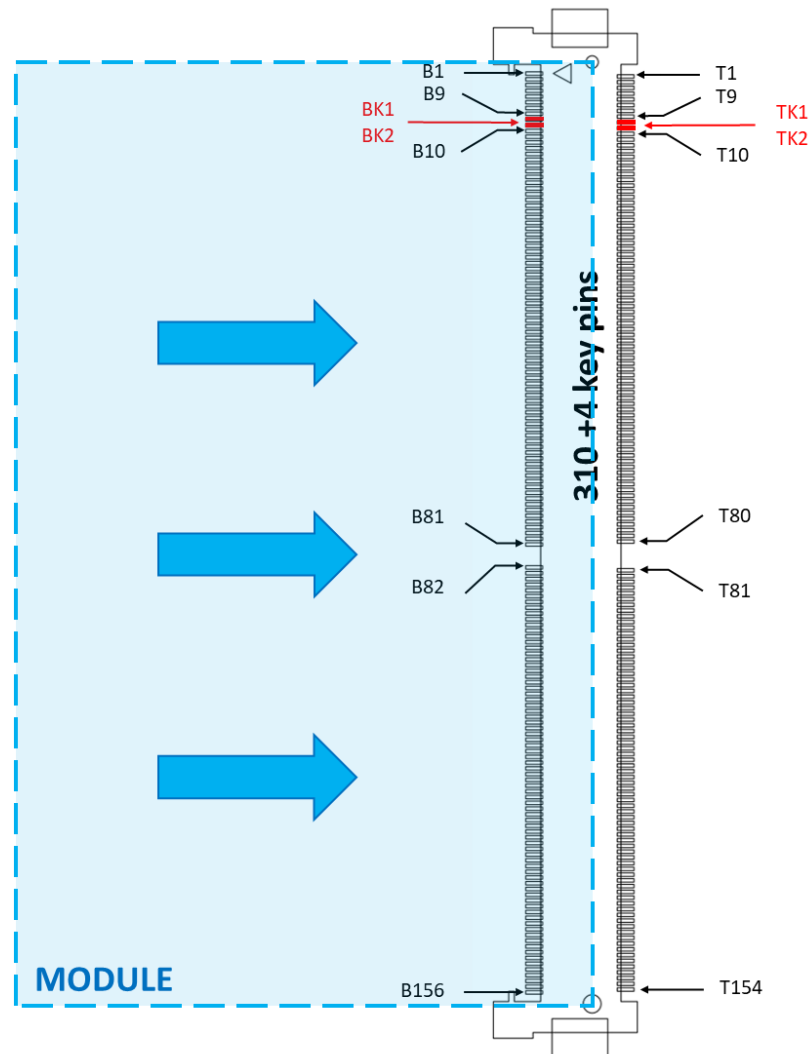


Figure 5-2 Connector orientation

The module connector is usually used for MXM3 graphic cards commonly found in notebooks. MicroSys changed the pin layout so that all 314 physically available pins can be used.

Alternatives - there are several connectors on the market that can be used if there are no conflicts with the mechanical dimensions of the module. The connectors usually have deviating mechanical pads thus drop-in replacements may require a combined PCB footprint. Please check the manufacturers' datasheets for details.

The recommended connectors for the MPX-S32G399A are:

| Manufacturer | Ordercode | Board-to-board height | Plating | Comment |
|--------------|--------------------|-----------------------|---------------------------------|----------|
| JAE | MM70-314B1-2-R300 | 3mm | 0.3µm min. gold plating over Ni | 314 pins |
| Foxconn | AS0B826-S55B-7H | 2,7mm | 10µm gold plating | |
| Foxconn | AS0B826-S78B-7H | 5mm | 10µm gold plating | |
| Aces | 91782-3140M-001 | 5mm | 3µm gold plating | |
| Yamaichi | CNU113-314-2201-VE | 5mm | 0.3µ" AU | |

Table 37 Connector Types: Ordering Information

5.5 Mounting/ Unmounting

The mounting or unmounting of the module should only be made in a static free area with full ESD precautions, i.e. as a minimum, a grounded dissipative work surface of sufficient size and a grounded skin contact wrist strap are necessary. Make sure that all parts, the carrier, the module and the heatsink are placed on the same static free area to avoid any discharges between them during assembly.

To mount the MPX-S32G399A module, make sure that the carrier is disconnected from any power or other IO interfaces. Both connector surfaces of the module must be clean as well as the carrier connector should be checked for bent or dirty contacts. Check the module and the carrier for foreign or loose parts, which do not belong to the boards. The screws should have clean threads and be tightened with a maximum torque of 30Ncm.

Insert or remove the MPX-S32G399A module at an angle of about 25° as shown in the following figure.

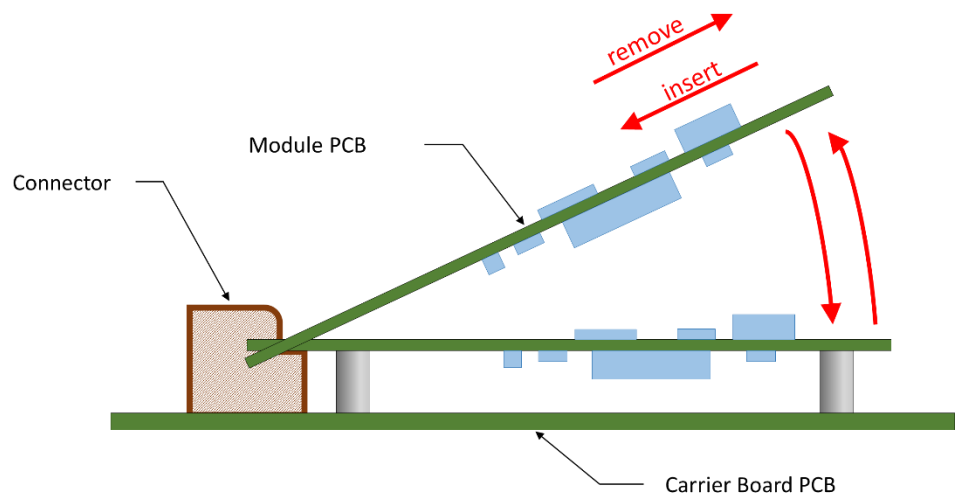


Figure 5-3 Module (un)mounting

The thermal conduction between heatsink and SoC is achieved using a thermal pad. Make sure that this thermal pad has the correct thickness and is placed over the SoC package before mounting the heatsink.

For the removal of the module, first unplug all connections to the system. Remove the inner screws, then the outer ones. The thermal pad may cause the heatsink to stick to the module, so take care when pulling them apart to avoid damaging any part of the module. Lift the module to about 25° and remove it from the connector. Store the parts on a static free area.

5.6 Board Outline

The following drawing shows the mechanical outline (82x50mm) of the MPX-S32G399A module:

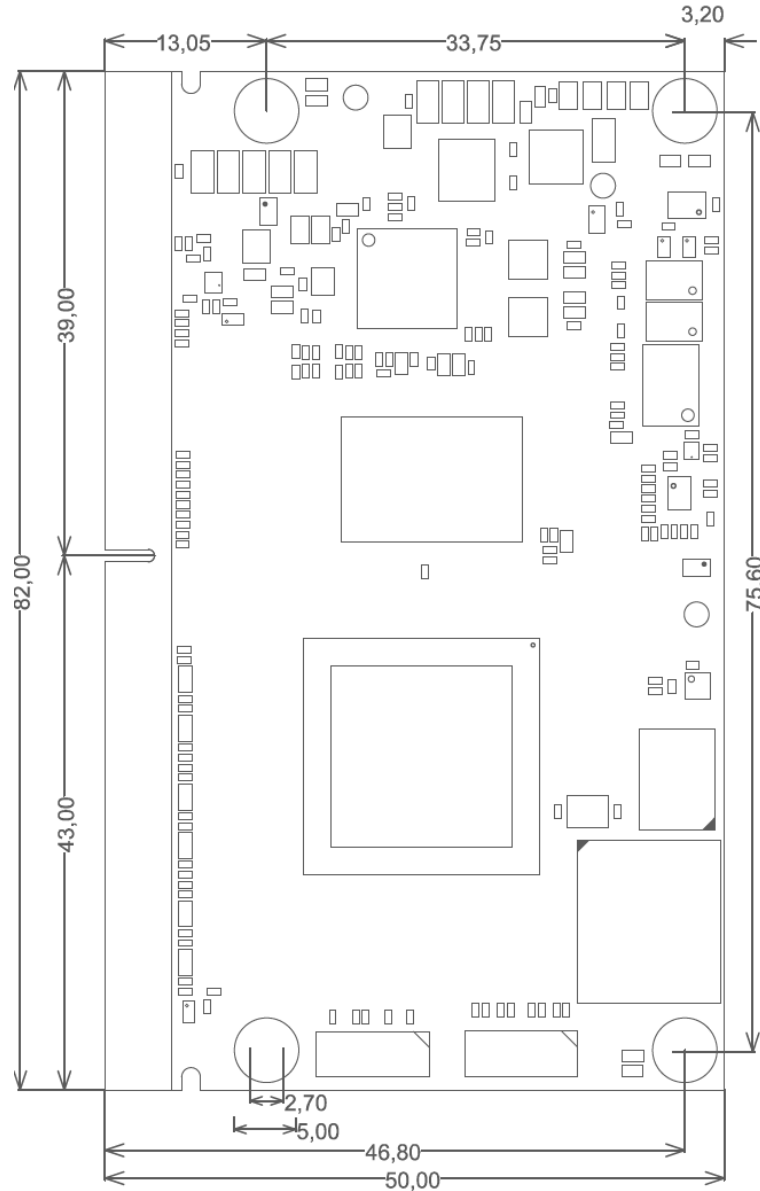


Figure 5-4 Board dimensions

The mounting holes require M2.5 screws.



For 3D data files please contact MicroSys.

5.7 Height

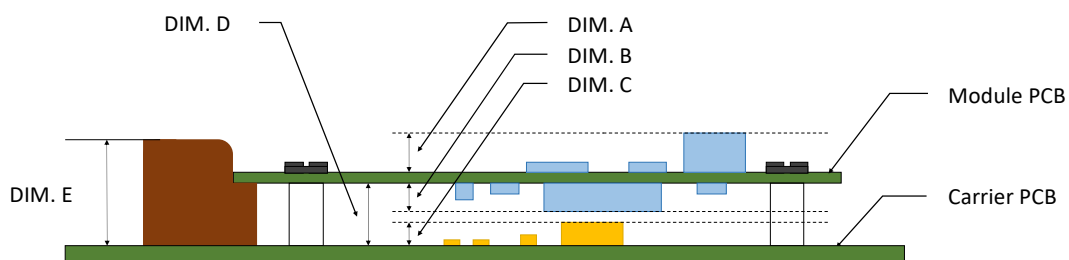


Figure 5-5 Construction height for parts

| | Definition | Value |
|--------|--------------------------------|---------------------------|
| DIM. A | Module top side parts | 3.00 mm |
| DIM. B | Module bottom side parts | 1.80 mm |
| DIM. C | Carrier parts under the module | DIM. D minus DIM. B |
| DIM. D | Board-to-board height | Depends on connector type |
| DIM. E | Connector product height | Depends on connector type |

Table 38 Construction height overview

5.8 Thickness

The PCB thickness of the MPX-S32G399A module is 1.2mm ± 10%.

5.9 Component Layout - Top Side

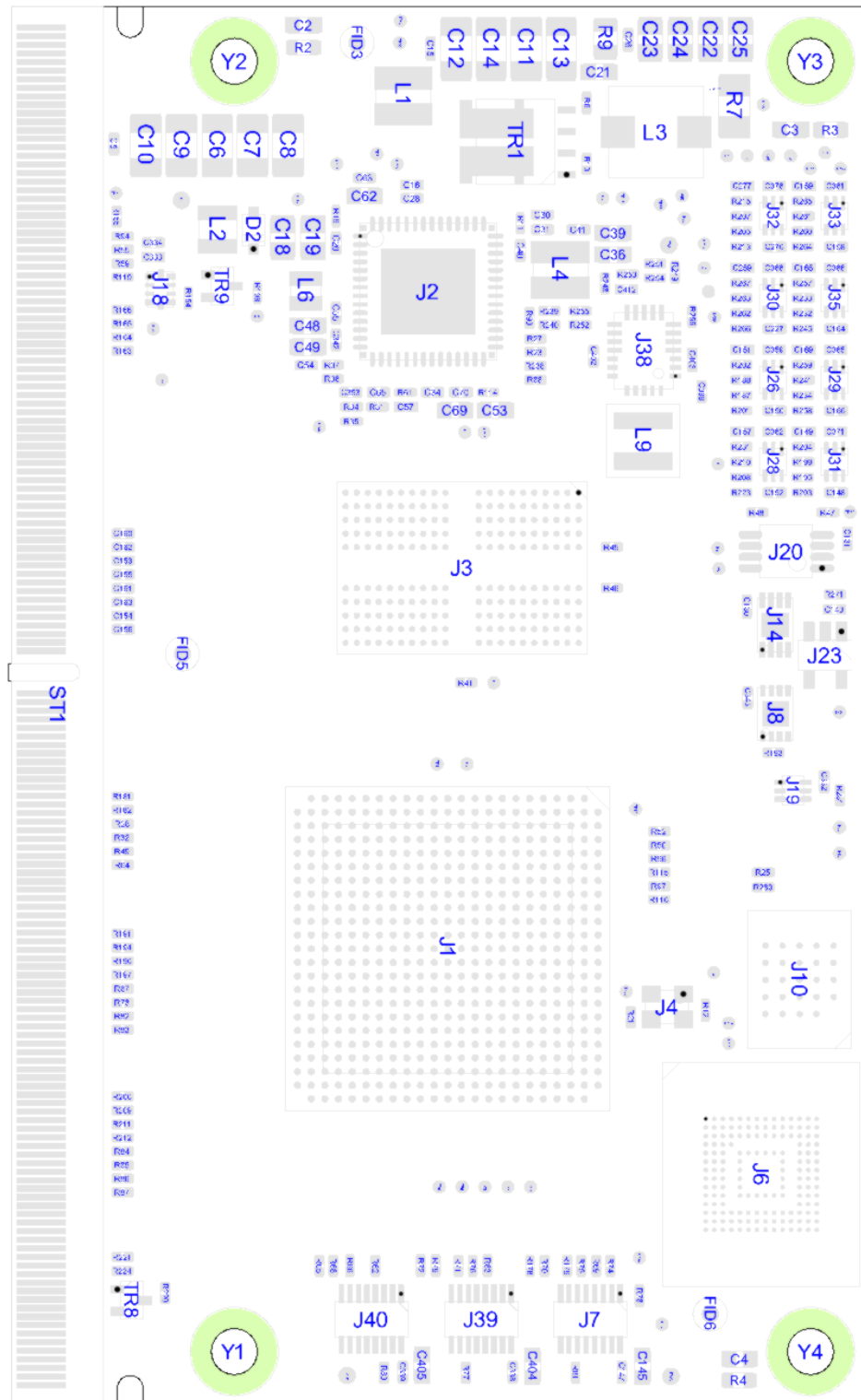


Figure 5-6 Top Components

The following table defines the main components on the top side:

| Part Reference | Type | Function |
|----------------|-----------------------|-----------------------------|
| ST1 | Edge Connector | Connection to carrier |
| J1 | S32G399A | SoC |
| J2 | PMIC | Regulator, power management |
| J3 | LPDDR4 | Memory |
| J6 | eMMC | Memory |
| J8 | M24C64 | EEPROM |
| J10 | Serial NOR Flash | Memory |
| J14 | Secondary Serial RCON | EEPROM |
| J19 | TMP112 | Temperature sensor |
| J23 | MCP9802 | Temperature Sensor |
| J38 | PF53 | Regulator |

Table 39 Top side components

5.10 Component Layout – Bottom Side

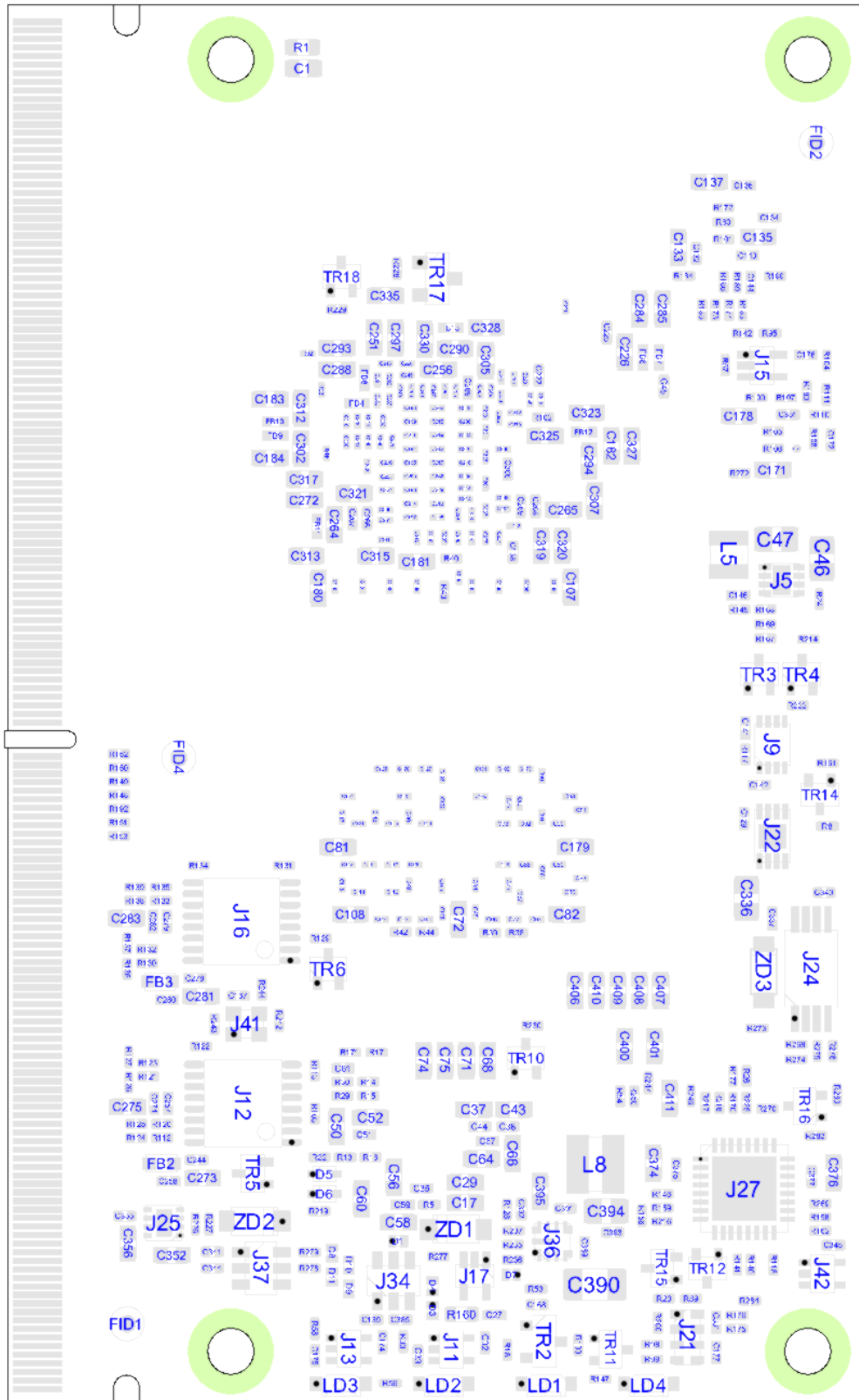


Figure 5-7 Bottom components

| Part Reference | Type | Function |
|--------------------|---------------------|------------------------|
| J12 | PI6C557 | Clock Generator |
| J16 | PI6C557 | Clock Generator |
| J21 | RV-3028-C7 | RTC |
| J22 | Primary Serial RCON | EEPROM |
| J27 | S32K1 | Microcontroller |
| LD1, LD2, LD3, LD4 | Side Looker LED | Reset, Power, User LED |

Table 40 Components on bottom

6 Software

6.1 U-Boot

The MPX-S32G399A uses U-Boot as the standard bootloader. The current version of U-Boot is pre-programmed in the boards QSPI Flash memory.

Additionally, there is a U-Boot version available for the SD card if that interface is implemented on the carrier. The standard MicroSys carrier (CRX-S32G) has an SD card interface.

Basically, the bootloader carries out the following tasks:

- Pin configuration
- SoC configuration
- Clock configuration
- LPDDR4 configuration and timing

6.2 Operating System

MicroSys Electronics GmbH offers Linux support for the module. Please refer to the MicroSys Software Enablement Guide for more details.

Other Operating Systems are available on request only.

7 Safety Requirements and Protective Regulations

7.1 EMC

The System on Module MPX-S32G399A is designed to meet requirements for electromagnetic compatibility. Nevertheless, there are several factors which in the target system may require measures against interference.

Active components, especially SoCs of the latest generation not only operate with high frequencies but also drive very fast signal rise times.

At least the following measures shall be applied:

- Provide sufficient block capacitors in the supply voltages
- Keep all clock lines short in order to prevent interference with other signals
- Shield clock lines with ground planes or keep as much distance as possible to other signals
- Provide filtering for all external signals
- Provide an EMI proof housing for final system

7.2 ESD

For technical reasons there is no ESD protection on the MPX-S32G399A. Please provide sufficient protection on the carrier and/or system level.

7.3 Reliability

The SoM MPX-S32G399A is available for operation in extended temperature range.

Please note that steady high temperature operation reduces lifetime of all electronic components. Make sure that no component on the module ever exceeds its maximum specified temperature during operation or storage. A reasonable cooling concept can dramatically increase the lifetime of the system.

The MPX-S32G399A is designed to withstand a high level of vibration and shock since there are no heavy and no overhanging components on the module. If desired, MicroSys Electronics GmbH can support you with your shock and vibration concept. Please ask your sales representative or send an email inquiry to support@microsys.de.

Relevant components on the module are chosen with values for a high level of derating.

7.4 Climatic conditions

The relative humidity during operation or storage of the module may not exceed 10% to 90%, non-condensing.

7.5 RoHS

All components on the MPX-S32G399A are RoHS compliant, also a RoHS compliant soldering process is used for manufacturing.

7.6 Storage Temperature

The storage temperature of the module is -55°C - +100°C.

8 General notes

Customers responsibility for chip errata:

It is the user's responsibility to make sure all errata published by the manufacturer of each component are taken note of.

The manufacturer's advice should be followed.

If desired, MicroSys Electronics GmbH can support you with your lifecycle management regarding chip errata. Please ask your sales representative or send an email inquiry to support@microsys.de.

9 History

| Date | Version | Change Description |
|------------|---------|---|
| 2024-09-27 | 6.0 | First Version Revision 6 for MPX-S32G399A |
| 2024-10-28 | 6.0 | Changed Figure 4-7 |
| 2025-03-17 | 6.1 | Added chapter 4.14 (Debug Mode) |

Table 41 Document history

10 Appendix

10.1 Acronyms

These acronyms are being used within the document; note that this list does not claim to be complete or exhaustive:

| | |
|-----------------------|---|
| ADC..... | Analog-to-Digital Converter |
| CAN..... | Controller Area Network |
| ESD..... | Electrostatic Discharge |
| GPL..... | General Public License |
| I ² C..... | Inter-Integrated Circuit |
| JTAG..... | Joint Test Action Group |
| LED..... | Light Emitting Diode |
| LIN..... | Local Interconnect Network |
| LPDDR..... | Low Power Double Data Rate memory |
| MCU..... | Microcontroller Unit |
| PD..... | Pull-Down Resistor |
| PU..... | Pull-Up Resistor, Pull-Up Resistor |
| RGMII..... | Reduced Gigabit Media Independent Interface |
| RTC..... | Real-Time clock |
| SDHC..... | Secure Digital Host Controller |
| SerDes..... | Serializer Deserializer |
| SPI..... | Serial Peripheral Interface |
| UART..... | Universal Asynchronous Receiver Transmitter |
| ULPI..... | UTMI+ Low Pin Interface |
| USB..... | Universal Serial Bus |

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10.4 Pin Definitions – Top

OUT = Output from module

IN = Input to module

| Pin | Name | CPU Ball | GPIO | Group | Direction | Supply Voltage | PU/PD | PU/PD Value | Series R/C |
|-----|---------------------------|----------|------|--------------|------------|------------------|-------|-------------|------------|
| T1 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T2 | PC14_SD_CLK | E19 | PC14 | SDHC | OUT | VCC_SDHC_1V8/3V3 | --- | --- | 22R |
| T3 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T4 | PD15_SD_CMD | F21 | PC15 | SDHC | INOUT | VCC_SDHC_1V8/3V3 | --- | --- | 22R |
| T5 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T6 | PD00_SD_D0 | G22 | PD00 | SDHC | INOUT | VCC_SDHC_1V8/3V3 | --- | --- | 0R |
| T7 | PD01_SD_D1 | E20 | PD01 | SDHC | INOUT | VCC_SDHC_1V8/3V3 | --- | --- | 0R |
| T8 | PD02_SD_D2 | H19 | PD02 | SDHC | INOUT | VCC_SDHC_1V8/3V3 | --- | --- | 0R |
| T9 | PD03_SD_D3 | H20 | PD03 | SDHC | INOUT | VCC_SDHC_1V8/3V3 | --- | --- | 0R |
| TK1 | VCC_SDHC_1V8/3V3 | --- | --- | Power / SDHC | | --- | --- | --- | --- |
| TK2 | PMIC_FCCU1_OUT | --- | --- | CTRL | OUT | +VREF4 (3V3) | PU | 5k1 | --- |
| T10 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T11 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T12 | PF00_RGMII2_MDC/DSPI0_CS7 | M19 | PF00 | RGMII | OUT | +VREF1 (1V8) | --- | --- | 10R |
| T13 | PF01_RGMII2_MDIO | L22 | PF01 | RGMII | INOUT | +VREF1 (1V8) | PU | 10k | --- |
| T14 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T15 | PH00_RGMII2_RXD3/USB_D7 | N23 | PH00 | RGMII / ULPI | IN / INOUT | +VREF1 (1V8) | --- | --- | --- |
| T16 | PL14_RGMII2_RXD2/USB_D6 | M21 | PL14 | RGMII / ULPI | IN / INOUT | +VREF1 (1V8) | --- | --- | --- |
| T17 | PL13_RGMII2_RXD1/USB_D5 | N21 | PL13 | RGMII / ULPI | IN / INOUT | +VREF1 (1V8) | --- | --- | --- |

| | | | | | | | | | |
|-----|----------------------------|-----|------|--------------|-------------|--------------|-----|-----|-----|
| T18 | PL12_RGMII2_RXD0/USB_D4 | N20 | PL12 | RGMII / ULPI | IN / INOUT | +VREF1 (1V8) | --- | --- | --- |
| T19 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T20 | PE01_RGMII2_RXDV/USB_D3 | M23 | PE01 | RGMII / ULPI | IN / INOUT | +VREF1 (1V8) | --- | --- | --- |
| T21 | PE00_RGMII2_RX_CLK/USB_D2 | P21 | PE00 | RGMII / ULPI | IN / INOUT | +VREF1 (1V8) | --- | --- | --- |
| T22 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T23 | PD15_RGMII2_TXD3/USB_D1 | L21 | PD15 | RGMII / ULPI | OUT / INOUT | +VREF1 (1V8) | --- | --- | 10R |
| T24 | PD14_RGMII2_TXD2/USB_D0 | P23 | PD14 | RGMII / ULPI | OUT / INOUT | +VREF1 (1V8) | --- | --- | 10R |
| T25 | PL11_RGMII2_TXD1/USB_NXT | N22 | PL11 | RGMII / ULPI | OUT / IN | +VREF1 (1V8) | --- | --- | 10R |
| T26 | PL10_RGMII2_TXD0/USB_STP | P22 | PL10 | RGMII / ULPI | OUT / OUT | +VREF1 (1V8) | --- | --- | 10R |
| T27 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T28 | PL09_RGMII2_TX_EN/USB_DIR | L23 | PL09 | RGMII / ULPI | OUT / IN | +VREF1 (1V8) | --- | --- | 10R |
| T29 | PL08_RGMII2_TX_CLK/USB_CLK | N19 | PL08 | RGMII / ULPI | OUT / IN | +VREF1 (1V8) | --- | --- | 10R |
| T30 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T31 | PD12_RGMII1_MDC | V23 | PD12 | RGMII | OUT | +VREF1 (1V8) | --- | --- | 10R |
| T32 | PD13_RGMII1_MDIO | R19 | PD13 | RGMII | INOUT | +VREF1 (1V8) | PU | 10k | --- |
| T33 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T34 | PE13_RGMII1_RXD3 | U21 | PE13 | RGMII | IN | +VREF1 (1V8) | --- | --- | --- |
| T35 | PE12_RGMII1_RXD2 | N18 | PE12 | RGMII | IN | +VREF1 (1V8) | --- | --- | --- |
| T36 | PE11_RGMII1_RXD1 | P18 | PE11 | RGMII | IN | +VREF1 (1V8) | --- | --- | --- |
| T37 | PE10_RGMII1_RXD0 | P19 | PE10 | RGMII | IN | +VREF1 (1V8) | --- | --- | --- |
| T38 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T39 | PE09_RGMII1_RXDV | R23 | PE09 | RGMII | IN | +VREF1 (1V8) | --- | --- | --- |
| T40 | PE08_RGMII1_RX_CLK | R21 | PE08 | RGMII | IN | +VREF1 (1V8) | --- | --- | --- |
| T41 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T42 | PE07_RGMII1_TXD3 | T21 | PE07 | RGMII | OUT | +VREF1 (1V8) | --- | --- | 10R |
| T43 | PE06_RGMII1_TXD2 | U22 | PE06 | RGMII | OUT | +VREF1 (1V8) | --- | --- | 10R |
| T44 | PE05_RGMII1_TXD1 | T22 | PE05 | RGMII | OUT | +VREF1 (1V8) | --- | --- | 10R |

| | | | | | | | | | |
|-----|--------------------|------|------|--------|-------|--------------|-----|-----|-----|
| T45 | PE04_RGMII1_TXD0 | T23 | PE04 | RGMII | OUT | +VREF1 (1V8) | --- | --- | 10R |
| T46 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T47 | PE03_RGMII1_TX_EN | U23 | PE03 | RGMII | OUT | +VREF1 (1V8) | --- | --- | 10R |
| T48 | PE02_RGMII1_TX_CLK | P20 | PE02 | RGMII | OUT | +VREF1 (1V8) | --- | --- | 10R |
| T49 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T50 | PF02_RGMII0_MDC | Y21 | PF02 | RGMII | OUT | +VREF1 (1V8) | --- | --- | 10R |
| T51 | PE15_RGMII0_MDIO | V17 | PE15 | RGMII | INOUT | +VREF1 (1V8) | PU | 10k | --- |
| T52 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T53 | PH09_RGMII0_RXD3 | W22 | PH09 | RGMII | IN | +VREF1 (1V8) | --- | --- | --- |
| T54 | PH08_RGMII0_RXD2 | W21 | PH08 | RGMII | IN | +VREF1 (1V8) | --- | --- | --- |
| T55 | PH07_RGMII0_RXD1 | Y23 | PH07 | RGMII | IN | +VREF1 (1V8) | --- | --- | --- |
| T56 | PH06_RGMII0_RXD0 | T20 | PH06 | RGMII | IN | +VREF1 (1V8) | --- | --- | --- |
| T57 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T58 | PH05_RGMII0_RXDV | W23 | PH05 | RGMII | IN | +VREF1 (1V8) | --- | --- | --- |
| T59 | PH04_RGMII0_RX_CLK | V21 | PH04 | RGMII | IN | +VREF1 (1V8) | --- | --- | --- |
| T60 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T61 | PH03_RGMII0_TXD3 | U20 | PH03 | RGMII | OUT | +VREF1 (1V8) | --- | --- | 10R |
| T62 | PH02_RGMII0_TXD2 | U18 | PH02 | RGMII | OUT | +VREF1 (1V8) | --- | --- | 10R |
| T63 | PH01_RGMII0_TXD1 | T19 | PH01 | RGMII | OUT | +VREF1 (1V8) | --- | --- | 10R |
| T64 | PJ00_RGMII0_TXD0 | U19 | PJ00 | RGMII | OUT | +VREF1 (1V8) | --- | --- | 10R |
| T65 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T66 | PE14_RGMII0_TX_EN | T18 | PE14 | RGMII | OUT | +VREF1 (1V8) | --- | --- | 10R |
| T67 | PH10_RGMII0_TX_CLK | V20 | PH10 | RGMII | OUT | +VREF1 (1V8) | --- | --- | 10R |
| T68 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T69 | PCIE1_RX0_N | AB22 | --- | SERDES | IN | +VREF1 (1V8) | --- | --- | --- |
| T70 | PCIE1_RX0_P | AA22 | --- | SERDES | IN | +VREF1 (1V8) | --- | --- | --- |
| T71 | GND | --- | --- | GND | | --- | --- | --- | --- |

| | | | | | | | | | |
|-----|--------------------|------|-----|-----------------|-----|------------------|-----|-----|-------|
| T72 | PCIE1_RX1_N | AC21 | --- | SERDES | IN | +VREF1 (1V8) | --- | --- | --- |
| T73 | PCIE1_RX1_P | AB21 | --- | SERDES | IN | +VREF1 (1V8) | --- | --- | --- |
| T74 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T75 | PCIE0_RX0_N | AC19 | --- | SERDES | IN | +VREF1 (1V8) | --- | --- | --- |
| T76 | PCIE0_RX0_P | AB19 | --- | SERDES | IN | +VREF1 (1V8) | --- | --- | --- |
| T77 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T78 | PCIE0_RX1_N | AC18 | --- | SERDES | IN | +VREF1 (1V8) | --- | --- | --- |
| T79 | PCIE0_RX1_P | AB18 | --- | SERDES | IN | +VREF1 (1V8) | --- | --- | --- |
| T80 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T81 | KILL/MCU_SWD_CLK | --- | --- | MICROCONTROLLER | IN | '+3V3_EXT / _INT | PD | 10K | --- |
| T82 | SAFEIO/MCU_SWD_DIO | --- | --- | MICROCONTROLLER | OUT | '+3V3_EXT / _INT | PU | 10K | --- |
| T83 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T84 | PCIE1_TX0_N | Y19 | --- | SERDES | OUT | +VREF1 (1V8) | --- | --- | 220nF |
| T85 | PCIE1_TX0_P | W19 | --- | SERDES | OUT | +VREF1 (1V8) | --- | --- | 220nF |
| T86 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T87 | PCIE1_TX1_N | Y18 | --- | SERDES | OUT | +VREF1 (1V8) | --- | --- | 220nF |
| T88 | PCIE1_TX1_P | W18 | --- | SERDES | OUT | +VREF1 (1V8) | --- | --- | 220nF |
| T89 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T90 | PCIE0_TX0_N | Y16 | --- | SERDES | OUT | +VREF1 (1V8) | --- | --- | 220nF |
| T91 | PCIE0_TX0_P | W16 | --- | SERDES | OUT | +VREF1 (1V8) | --- | --- | 220nF |
| T92 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T93 | PCIE0_TX1_N | Y15 | --- | SERDES | OUT | +VREF1 (1V8) | --- | --- | 220nF |
| T94 | PCIE0_TX1_P | W15 | --- | SERDES | OUT | +VREF1 (1V8) | --- | --- | 220nF |
| T95 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T96 | AUR_CLK_N | AB11 | --- | AURORA | IN | +VREF1 (1V8) | --- | --- | --- |
| T97 | AUR_CLK_P | AC11 | --- | AURORA | IN | +VREF1 (1V8) | --- | --- | --- |

| | | | | | | | | |
|------|---------------|------|------|--------|-------|----------------------|-----|-----|
| T98 | GND | --- | --- | GND | | --- | --- | --- |
| T99 | AUR_TX2_N | AB9 | --- | AURORA | OUT | +VREF1 (1V8) | --- | --- |
| T100 | AUR_TX2_P | AC9 | --- | AURORA | OUT | +VREF1 (1V8) | --- | --- |
| T101 | GND | --- | --- | GND | | --- | --- | --- |
| T102 | AUR_TX0_N | AB8 | --- | AURORA | OUT | +VREF1 (1V8) | --- | --- |
| T103 | AUR_TX0_P | AC8 | --- | AURORA | OUT | +VREF1 (1V8) | --- | --- |
| T104 | GND | --- | --- | GND | | --- | --- | --- |
| T105 | AUR_TX1_N | AC6 | --- | AURORA | OUT | +VREF1 (1V8) | --- | --- |
| T106 | AUR_TX1_P | AB6 | --- | AURORA | OUT | +VREF1 (1V8) | --- | --- |
| T107 | GND | --- | --- | GND | | --- | --- | --- |
| T108 | AUR_TX3_N | AC5 | --- | AURORA | OUT | +VREF1 (1V8) | --- | --- |
| T109 | AUR_TX3_P | AB5 | --- | AURORA | OUT | +VREF1 (1V8) | --- | --- |
| T110 | GND | --- | --- | GND | | --- | --- | --- |
| T111 | PB02 | D7 | PB02 | GPIO | INOUT | +VREF3 (3V3) | --- | --- |
| T112 | PB07 | A5 | PB07 | GPIO | INOUT | +VREF3 (3V3) | --- | --- |
| T113 | PB08 | F7 | PB08 | GPIO | INOUT | +VREF3 (3V3) | --- | --- |
| T114 | PB15 | B5 | PB15 | GPIO | INOUT | +VREF3 (3V3) | --- | --- |
| T115 | PC00 | V9 | PC00 | GPIO | INOUT | +VREF3 (3V3) | --- | --- |
| T116 | GND | --- | --- | GND | | --- | --- | --- |
| T117 | +VREF1 | --- | --- | POWER | | 1V8 Reference Output | --- | --- |
| T118 | +VREF2 | --- | --- | POWER | | 1V8 Reference Output | --- | --- |
| T119 | +VREF3 | --- | --- | POWER | | 3V3 Reference Output | --- | --- |
| T120 | +VREF4 | --- | --- | POWER | | 3V3 Reference Output | --- | --- |
| T121 | GND | --- | --- | GND | | --- | --- | --- |
| T122 | PCIE0_CLKIN_N | AC15 | --- | SERDES | IN | +VREF1 (1V8) | --- | --- |

| | | | | | | | | | |
|------|----------------|------|-----|------------|-------|--|-----|-----|------|
| T123 | PCIE0_CLKIN_P | AB15 | --- | SERDES | IN | +VREF1 (1V8) | --- | --- | --- |
| T124 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T125 | NMI | G6 | --- | CTRL | IN | +VREF3 (3V3) | PU | 4k7 | --- |
| T126 | PMIC_RST# | --- | --- | CTRL | OUT | +VREF4 (3V3) | PU | 2k2 | --- |
| T127 | RSTIN# | --- | --- | CTRL | IN | +VREF4 (3V3) | PU | 4k7 | 100R |
| T128 | RST# | --- | --- | CTRL | OUT | +VREF4 (3V3) | PU | 2k2 | --- |
| T129 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T130 | SEL_CLK_RC/EP# | --- | --- | CTRL | IN | +VREF4 (3V3) | PU | 10k | --- |
| T131 | RCW_SEL# | --- | --- | CTRL | IN | +3V3_INT | PU | 4k7 | --- |
| T132 | RESERVED | --- | --- | CTRL | IN | +3V3_INT | PU | 10k | --- |
| T133 | VCC_RTC | --- | --- | POWER | | RTC Backup Supply: Module Input (0.9V - 5.5V) | --- | --- | --- |
| T134 | +3V3_EXT | --- | --- | PRODUCTION | | Programming Voltage: Module Input (3.3V ± 5%) | --- | --- | --- |
| T135 | I2C_SCL_PROG | --- | --- | PRODUCTION | OUT | +3V3_EXT / _INT | PU | 2k7 | --- |
| T136 | I2C_SDA_PROG | --- | --- | PRODUCTION | INOUT | +3V3_EXT / _INT | PU | 2k7 | --- |
| T137 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T138 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T139 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T140 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T141 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T142 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T143 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T144 | GND | --- | --- | GND | | --- | --- | --- | --- |
| T145 | GND | --- | --- | GND | | --- | --- | --- | --- |

| | | | | | | | | |
|------|------|-----|-----|-------|-------|-----|-----|-----|
| T146 | +VIN | --- | --- | POWER | 6-36V | --- | --- | --- |
| T147 | +VIN | --- | --- | POWER | 6-36V | --- | --- | --- |
| T148 | +VIN | --- | --- | POWER | 6-36V | --- | --- | --- |
| T149 | +VIN | --- | --- | POWER | 6-36V | --- | --- | --- |
| T150 | +VIN | --- | --- | POWER | 6-36V | --- | --- | --- |
| T151 | +VIN | --- | --- | POWER | 6-36V | --- | --- | --- |
| T152 | +VIN | --- | --- | POWER | 6-36V | --- | --- | --- |
| T153 | +VIN | --- | --- | POWER | 6-36V | --- | --- | --- |
| T154 | +VIN | --- | --- | POWER | 6-36V | --- | --- | --- |

10.5 Pin Definitions – Bottom

OUT = Output from module

IN = Input to module

| Pin | Name | CPU Ball | Target | Group | Direction | Supply Voltage | PU/PD | PU/PD Value | Series R/C |
|-----|-----------------|----------|--------|-------|-----------|----------------|-------|-------------|------------|
| B1 | ADC_CH_11 | C21 | --- | ADC | IN | +VREF1 (1V8) | --- | --- | --- |
| B2 | ADC_CH_10 | A20 | --- | ADC | IN | +VREF1 (1V8) | --- | --- | --- |
| B3 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B4 | ADC_CH_09 | B20 | --- | ADC | IN | +VREF1 (1V8) | --- | --- | --- |
| B5 | ADC_CH_08 | A19 | --- | ADC | IN | +VREF1 (1V8) | --- | --- | --- |
| B6 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B7 | ADC_CH_07 | C22 | --- | ADC | IN | +VREF1 (1V8) | --- | --- | --- |
| B8 | ADC_CH_06 | D23 | --- | ADC | IN | +VREF1 (1V8) | --- | --- | --- |
| B9 | GND | --- | --- | GND | | --- | --- | --- | --- |
| BK1 | PMIC_STBY# | --- | | CTRL | OUT | +VREF4 (3V3) | PU | 10k | --- |
| BK2 | PMIC_STBY_PGOOD | --- | | CTRL | OUT | +VREF4 (3V3) | --- | --- | --- |
| B10 | ADC_CH_05 | B22 | --- | ADC | IN | +VREF1 (1V8) | --- | --- | --- |
| B11 | ADC_CH_04 | B21 | --- | ADC | IN | +VREF1 (1V8) | --- | --- | --- |
| B12 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B13 | ADC_CH_03 | D22 | --- | ADC | IN | +VREF1 (1V8) | --- | --- | --- |
| B14 | ADC_CH_02 | E23 | --- | ADC | IN | +VREF1 (1V8) | --- | --- | --- |
| B15 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B16 | ADC_CH_01 | E22 | --- | ADC | IN | +VREF1 (1V8) | --- | --- | --- |
| B17 | ADC_CH_00 | F23 | --- | ADC | IN | +VREF1 (1V8) | --- | --- | --- |

| | | | | | | | | |
|-----|---------------|-----|------|-----|-----|--------------|-----|-----|
| B18 | GND | --- | --- | GND | | --- | --- | --- |
| B19 | PC11_CAN00_RX | F15 | PC11 | CAN | IN | +VREF4 (3V3) | --- | --- |
| B20 | PC12_CAN00_TX | G11 | PC12 | CAN | OUT | +VREF3 (3V3) | --- | --- |
| B21 | GND | --- | --- | GND | | --- | --- | --- |
| B22 | PJ02_CAN01_RX | D17 | PJ02 | CAN | IN | +VREF4 (3V3) | --- | --- |
| B23 | PJ01_CAN01_TX | B11 | PJ01 | CAN | OUT | +VREF3 (3V3) | --- | --- |
| B24 | GND | --- | --- | GND | | --- | --- | --- |
| B25 | PJ04_CAN02_RX | C15 | PJ04 | CAN | IN | +VREF4 (3V3) | --- | --- |
| B26 | PJ03_CAN02_TX | D10 | PJ03 | CAN | OUT | +VREF3 (3V3) | --- | --- |
| B27 | GND | --- | --- | GND | | --- | --- | --- |
| B28 | PJ06_CAN03_RX | D15 | PJ06 | CAN | IN | +VREF4 (3V3) | --- | --- |
| B29 | PJ05_CAN03_TX | C11 | PJ05 | CAN | OUT | +VREF3 (3V3) | --- | --- |
| B30 | GND | --- | --- | GND | | --- | --- | --- |
| B31 | PJ08_CAN04_RX | F16 | PJ08 | CAN | IN | +VREF4 (3V3) | --- | --- |
| B32 | PJ07_CAN04_TX | D12 | PJ07 | CAN | OUT | +VREF3 (3V3) | --- | --- |
| B33 | GND | --- | --- | GND | | --- | --- | --- |
| B34 | PJ10_CAN05_RX | D16 | PJ10 | CAN | IN | +VREF4 (3V3) | --- | --- |
| B35 | PJ09_CAN05_TX | B12 | PJ09 | CAN | OUT | +VREF3 (3V3) | --- | --- |
| B36 | GND | --- | --- | GND | | --- | --- | --- |
| B37 | PJ12_CAN06_RX | E16 | PJ12 | CAN | IN | +VREF4 (3V3) | --- | --- |
| B38 | PJ11_CAN06_TX | E12 | PJ11 | CAN | OUT | +VREF3 (3V3) | --- | --- |
| B39 | GND | --- | --- | GND | | --- | --- | --- |
| B40 | PJ14_CAN07_RX | C16 | PJ14 | CAN | IN | +VREF4 (3V3) | --- | --- |
| B41 | PJ13_CAN07_TX | A11 | PJ13 | CAN | OUT | +VREF3 (3V3) | --- | --- |
| B42 | GND | --- | --- | GND | | --- | --- | --- |

| | | | | | | | | | |
|-----|-----------------|-----|------|-----|-----|--------------|-----|-----|-----|
| B43 | PK00_CAN08_RX | A15 | PK00 | CAN | IN | +VREF4 (3V3) | --- | --- | --- |
| B44 | PJ15_CAN08_TX | A10 | PJ15 | CAN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B45 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B46 | PK02_CAN09_RX | D14 | PK02 | CAN | IN | +VREF4 (3V3) | --- | --- | --- |
| B47 | PK01_CAN09_TX | F11 | PK01 | CAN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B48 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B49 | PK04_CAN10_RX | F14 | PK04 | CAN | IN | +VREF4 (3V3) | --- | --- | --- |
| B50 | PK03_CAN10_TX | E11 | PK03 | CAN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B51 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B52 | PK06_CAN11_RX | B15 | PK06 | CAN | IN | +VREF4 (3V3) | --- | --- | --- |
| B53 | PK05_CAN11_TX | D11 | PK05 | CAN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B54 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B55 | PK08_CAN12_RX | F13 | PK08 | CAN | IN | +VREF4 (3V3) | --- | --- | --- |
| B56 | PK07_CAN12_TX | C10 | PK07 | CAN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B57 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B58 | PK10_CAN13_RX | E14 | PK10 | CAN | IN | +VREF4 (3V3) | --- | --- | --- |
| B59 | PK09_CAN13_TX | E10 | PK09 | CAN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B60 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B61 | PK12_CAN14_RX | C14 | PK12 | CAN | IN | +VREF4 (3V3) | --- | --- | --- |
| B62 | PK11_CAN14_TX | A9 | PK11 | CAN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B63 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B64 | PK14_CAN15_RX | B13 | PK14 | CAN | IN | +VREF4 (3V3) | --- | --- | --- |
| B65 | PK13_CAN15_TX | C9 | PK13 | CAN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B66 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B67 | PA15_DSPIO_SOUT | W13 | PA15 | SPI | OUT | +VREF3 (3V3) | --- | --- | --- |

| | | | | | | | | | |
|-----|------------------|------|------|---------|-----|--------------|-----|-----|-----|
| B68 | PA13_DSPIO_SCK | U12 | PA13 | SPI | OUT | +VREF3 (3V3) | --- | --- | --- |
| B69 | PA14_DSPIO_SIN | AA12 | PA14 | SPI | IN | +VREF3 (3V3) | --- | --- | --- |
| B70 | PB09_DSPIO_CS1 | AA10 | PB09 | SPI | OUT | +VREF3 (3V3) | --- | --- | --- |
| B71 | PB10_DSPIO_CS2 | V11 | PB10 | SPI | OUT | +VREF3 (3V3) | --- | --- | --- |
| B72 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B73 | PA06_DSPI1_SOUT | Y9 | PA06 | SPI | OUT | +VREF3 (3V3) | --- | --- | --- |
| B74 | PA08_DSPI1_SCK | U10 | PA08 | SPI | OUT | +VREF3 (3V3) | --- | --- | --- |
| B75 | PF15_DSPI1_SIN | U8 | PF15 | SPI | IN | +VREF3 (3V3) | --- | --- | --- |
| B76 | PA07_DSPI1_CS0 | Y11 | PA07 | SPI | IN | +VREF3 (3V3) | --- | --- | --- |
| B77 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B78 | PA11_DSPI5_SOUT | D8 | PA11 | SPI | OUT | +VREF3 (3V3) | --- | --- | --- |
| B79 | PA09_DSPI5_SCK | B8 | PA09 | SPI | OUT | +VREF3 (3V3) | --- | --- | --- |
| B80 | PA10_DSPI5_SIN | E13 | PA10 | SPI | IN | +VREF4 (3V3) | --- | --- | --- |
| B81 | PA12_DSPI5_CS0 | C7 | PA12 | SPI | IN | +VREF3 (3V3) | --- | --- | --- |
| B82 | PA04_JTAG_TCK | W9 | PA04 | JTAG | IN | +VREF3 (3V3) | PD | 10k | --- |
| B83 | PA01_JTAG_TDO | AA7 | PA01 | JTAG | OUT | +VREF3 (3V3) | --- | --- | --- |
| B84 | PA00_JTAG_TDI | V7 | PA00 | JTAG | IN | +VREF3 (3V3) | --- | --- | --- |
| B85 | PA05_JTAG_TMS | U7 | PA05 | JTAG | IN | +VREF3 (3V3) | PU | 10k | --- |
| B86 | JCOMP | W7 | --- | JTAG | IN | +VREF3 (3V3) | PD | 10k | --- |
| B87 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B88 | PF03_CLKOUT0 | V14 | PF03 | CLOCK | OUT | +VREF1 (1V8) | --- | --- | --- |
| B89 | PF04_CLKOUT1 | V13 | PF04 | CLOCK | OUT | +VREF1 (1V8) | --- | --- | --- |
| B90 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B91 | PL03_FLXR0A_RX_D | A13 | PL03 | FLEXRAY | IN | +VREF4 (3V3) | --- | --- | --- |
| B92 | PL02_FLXR0A_TX_D | A8 | PL02 | FLEXRAY | OUT | +VREF3 (3V3) | --- | --- | --- |

| | | | | | | | | | |
|------|-------------------|-----|------|---------|-----|--------------|-----|------|-----|
| B93 | PL01_FLXR0A_TXEN# | E9 | PL01 | FLEXRAY | OUT | +VREF3 (3V3) | --- | --- | --- |
| B94 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B95 | PL06_FLXR0B_RX_D | D13 | PL06 | FLEXRAY | IN | +VREF4 (3V3) | --- | --- | --- |
| B96 | PL05_FLXR0B_TX_D | C8 | PL05 | FLEXRAY | OUT | +VREF3 (3V3) | --- | --- | --- |
| B97 | PL04_FLXR0B_TXEN# | A7 | PL04 | FLEXRAY | OUT | +VREF3 (3V3) | --- | --- | --- |
| B98 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B99 | PB12_FXCAN2_RX | F8 | PB12 | CAN | IN | +VREF3 (3V3) | --- | --- | --- |
| B100 | PB11_FXCAN2_TX | G8 | PB11 | CAN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B101 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B102 | PB14_FXCAN3_RX | E6 | PB14 | CAN | IN | +VREF3 (3V3) | --- | --- | --- |
| B103 | PB13_FXCAN3_TX | G7 | PB13 | CAN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B104 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B105 | PL00_LIN0_RX | A12 | PL00 | LIN | IN | +VREF4 (3V3) | --- | --- | --- |
| B106 | PK15_LIN0_TX | F10 | PK15 | LIN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B107 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B108 | PC04_LIN1_RX | C13 | PC04 | LIN | IN | +VREF4 (3V3) | --- | --- | --- |
| B109 | PC08_LIN1_TX | B6 | PC08 | LIN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B110 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B111 | PC06_LIN2_RX | A14 | PC06 | LIN | IN | +VREF4 (3V3) | --- | --- | --- |
| B112 | PC05_LIN2_TX | G10 | PC05 | LIN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B113 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B114 | PL07_LIN3_RX | G13 | PL07 | LIN | IN | +VREF4 (3V3) | --- | --- | --- |
| B115 | PC07_LIN3_TX | B9 | PC07 | LIN | OUT | +VREF3 (3V3) | --- | --- | --- |
| B116 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B117 | PCIE1_CLKC_N | --- | --- | SERDES | OUT | +VREF4 (3V3) | PD | 49R9 | 33R |

| | | | | | | | | | |
|------|-----------------------|-----|------|-----------------|-------|--|-----|------|-----|
| B118 | PCIE1_CLKC_P | --- | --- | SERDES | OUT | +VREF4 (3V3) | PD | 49R9 | 33R |
| B119 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B120 | PCIE0_CLKC_N | --- | --- | SERDES | OUT | +VREF4 (3V3) | PD | 49R9 | 33R |
| B121 | PCIE0_CLKC_P | --- | --- | SERDES | OUT | +VREF4 (3V3) | PD | 49R9 | 33R |
| B122 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B123 | PMIC_FSOUT# | --- | --- | CTRL | OUT | +VREF3 (3V3) | PU | 4k7 | 0R |
| B124 | PMIC_FIN/MCU_SWD_RST# | --- | --- | CTRL | IN | +VREF4 (3V3) | PD | 10k | 0R |
| | | --- | --- | MICROCONTROLLER | IN | '+3V3_EXT / +3V3_INT | PU | 10k | 0R |
| B125 | VDD_OTP | --- | --- | DEBUG | | Optional debug voltage for PMIC Typ. 7.5V | PD | 470k | --- |
| B126 | PMIC_PWRON1 | --- | --- | CTRL | IN | +VIN | PU | 5k11 | --- |
| B127 | PMIC_PSYNC | --- | --- | CTRL | IN | +VREF4 (3V3) | PD | 0R | --- |
| B128 | PMIC_FOUT/AMUX | --- | --- | CTRL | OUT | +VREF4 (3V3) | --- | --- | --- |
| B129 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B130 | PC09_UART0_TX | U11 | PC09 | UART | OUT | +VREF3 (3V3) | --- | --- | --- |
| B131 | PC10_UART0_RX | Y12 | PC10 | UART | IN | +VREF3 (3V3) | --- | --- | --- |
| B132 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B133 | PB01_I2C0_SCL | E7 | PB01 | I2C | OUT | +VREF3 (3V3) | PU | 4k7 | --- |
| B134 | PB00_I2C0_SDA | W12 | PB00 | I2C | INOUT | +VREF3 (3V3) | PU | 4k7 | --- |
| B135 | PB03_I2C1_SCL | C6 | PB03 | I2C | OUT | +VREF3 (3V3) | PU | 4k7 | --- |
| B136 | PB04_I2C1_SDA | E8 | PB04 | I2C | INOUT | +VREF3 (3V3) | PU | 4k7 | --- |
| B137 | PB05_I2C2_SCL | A6 | PB05 | I2C | OUT | +VREF3 (3V3) | PU | 4k7 | --- |
| B138 | PB06_I2C2_SDA | G9 | PB06 | I2C | INOUT | +VREF3 (3V3) | PU | 4k7 | --- |
| B139 | GND | --- | --- | GND | | --- | --- | --- | --- |
| B140 | GND | --- | --- | GND | | --- | --- | --- | --- |

| | | | | | | | | |
|------|------------|-----|-----|-------|-------|-----|-----|-----|
| B141 | GND | --- | --- | GND | --- | --- | --- | --- |
| B142 | GND | --- | --- | GND | --- | --- | --- | --- |
| B143 | GND | --- | --- | GND | --- | --- | --- | --- |
| B144 | GND | --- | --- | GND | --- | --- | --- | --- |
| B145 | GND | --- | --- | GND | --- | --- | --- | --- |
| B146 | GND | --- | --- | GND | --- | --- | --- | --- |
| B147 | GND | --- | --- | GND | --- | --- | --- | --- |
| B148 | +VIN | --- | --- | Power | 6-36V | --- | --- | --- |
| B149 | +VIN | --- | --- | Power | 6-36V | --- | --- | --- |
| B150 | +VIN | --- | --- | Power | 6-36V | --- | --- | --- |
| B151 | +VIN | --- | --- | Power | 6-36V | --- | --- | --- |
| B152 | +VIN | --- | --- | Power | 6-36V | --- | --- | --- |
| B153 | +VIN | --- | --- | Power | 6-36V | --- | --- | --- |
| B154 | +VIN | --- | --- | Power | 6-36V | --- | --- | --- |
| B155 | +VIN | --- | --- | Power | 6-36V | --- | --- | --- |
| B156 | +VIN | --- | --- | Power | 6-36V | --- | --- | --- |

10.6 Pins not available for pin multiplexing

| Ball | Name | Usage | Comment |
|------|------|------------|--|
| PC14 | | SDC / eMMC | GPIO possible in case SEL_EMMC_SDHC# is always low (eMMC cannot be used) |
| PC15 | | SDC / eMMC | GPIO possible in case SEL_EMMC_SDHC# is always low (eMMC cannot be used) |
| PD00 | | SDC / eMMC | GPIO possible in case SEL_EMMC_SDHC# is always low (eMMC cannot be used) |
| PD01 | | SDC / eMMC | GPIO possible in case SEL_EMMC_SDHC# is always low (eMMC cannot be used) |
| PD02 | | SDC / eMMC | GPIO possible in case SEL_EMMC_SDHC# is always low (eMMC cannot be used) |
| PD03 | | SDC / eMMC | GPIO possible in case SEL_EMMC_SDHC# is always low (eMMC cannot be used) |
| PD04 | | SDC / eMMC | GPIO possible in case SEL_EMMC_SDHC# is always low (eMMC cannot be used) |
| PD05 | | SDC / eMMC | N/A |
| PD06 | | SDC / eMMC | N/A |
| PD07 | | SDC / eMMC | N/A |
| PD08 | | SDC / eMMC | N/A |
| PD09 | | SDC / eMMC | N/A |
| PD10 | | SDC / eMMC | N/A |
| | | | |
| PG00 | | QSPI | N/A |
| PG01 | | QSPI | N/A |
| PG02 | | QSPI | N/A |
| PG03 | | QSPI | N/A |
| PG04 | | QSPI | N/A |
| PG05 | | QSPI | N/A |
| PF05 | | QSPI | N/A |
| PF06 | | QSPI | N/A |
| PF07 | | QSPI | N/A |

| | | | |
|------|--------------------|--------|-----|
| PF08 | | QSPI | N/A |
| PF09 | | QSPI | N/A |
| PF10 | | QSPI | N/A |
| PF11 | | QSPI | N/A |
| PF12 | | QSPI | N/A |
| PF13 | | QSPI | N/A |
| PF14 | | QSPI | N/A |
| | | | |
| PA02 | PA02_BOOTMOD1 | CONFIG | N/A |
| PA03 | PA03_BOOTMOD2 | CONFIG | N/A |
| | | | |
| PB00 | PB00_I2C0_SDA | I2C | N/A |
| PB01 | PB01_I2C0_SCL | I2C | N/A |
| | | | |
| PC01 | PC01_I2C4_SDA_PMIC | I2C | N/A |
| PC02 | PC02_I2C4_SCL_PMIC | I2C | N/A |
| | | | |
| PC03 | PMIC_IRQ# | CONFIG | N/A |
| PC13 | PC13 | N/A | N/A |
| | | | |
| PD11 | PMIC_FS0# | CONFIG | N/A |